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dsPIC33FJXXXMCX06A/X08A/X10A

16-bit Digital Signal Controllers (up to 256 KB Flash and 30 KB SRAM) with Motor Control and Advanced Analog

Operating Conditions

- 3.0V to 3.6V, -40ºC to +150ºC, DC to 20 MIPS
- 3.0V to 3.6V, -40ºC to +125ºC, DC to 40 MIPS

Core: 16-bit dsPIC33F CPU

- Code-efficient (C and Assembly) architecture
- Two 40-bit wide accumulators
- Single-cycle (MAC/MPY) with dual data fetch
- Single-cycle mixed-sign MUL plus hardware divide

Clock Management

- ±2% internal oscillator
- Programmable PLLs and oscillator clock sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer (WDT)
- Fast wake-up and start-up

Power Management

- Low-power management modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset
- 1.35 mA/MHz dynamic current (typical)
- 55 μA I_{PD} current (typical)

Motor Control PWM

- Up to four PWM generators with eight outputs
- Dead Time for rising and falling edges
- 12.5 ns PWM resolution
- PWM support for Motor Control: BLDC, PMSM, ACIM, and SRM
- Programmable Fault inputs
- Flexible trigger for ADC conversions and configurations

Advanced Analog Features

- Two ADC modules:
  - Configurable as 10-bit, 1.1 Msps with four S&H or 12-bit, 500 ksps with one S&H
  - 18 analog inputs on 64-pin devices and up to 32 analog inputs on 100-pin devices
- Flexible and independent ADC trigger sources

Timers/Output Compare/Input Capture

- Up to nine 16-bit timers/counters. Can pair up to make four 32-bit timers.
- Eight Output Compare modules configurable as timers/counters
- Eight Input Capture modules

Communication Interfaces

- Two UART modules (10 Mbps)
  - With support for LIN 2.0 protocols and IrDA®
- Two 4-wire SPI modules (15 Mbps)
- Up to two I^2C™ modules (up to 1 Mbaud) with SMBus support
- Up to two Enhanced CAN (ECAN) modules (1 Mbaud) with 2.0B support
- Quadrature Encoder Interface (QEI) module
- Data Converter Interface (DCI) module with I^2S codec support

Input/Output

- Sink/Source up to 10 mA (pin specific) for standard V_{OH}/V_{OL}, up to 16 mA (pin specific) for non-standard V_{OH1}
- 5V-tolerant pins
- Selectable open drain, pull-ups, and pull-downs
- Up to 5 mA overvoltage clamp current
- External interrupts on all I/O pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1 -40ºC to +125ºC)
- AEC-Q100 REVG (Grade 0 -40ºC to +150ºC)
- Class B Safety Library, IEC 60730

Debugger Development Support

- In-circuit and in-application programming
- Two program and two complex data breakpoints
- IEEE 1149.2-compatible (JTAG) boundary scan
- Trace and run-time watch

Packages

Type	QFN	TQFP	TQFP	TQFP
Pin Count	64	64	80	100
Contact Lead/Pitch	0.50	0.50	0.50	0.40
I/O Pins	53	53	69	85
Dimensions	9x9x0.9	10x10x1	12x12x1	14x14x1

Note: All dimensions are in millimeters (mm) unless specified.

dsPIC33F PRODUCT FAMILIES

The dsPIC33FJXXXMCX06A/X08A/X10A family of devices supports a variety of motor control applications, such as brushless DC motors, single and 3-phase induction motors and switched reluctance motors. The dsPIC33F Motor Control products are also well-suited for Uninterrupted Power Supply (UPS), inverters, Switched mode power supplies, power factor correction and also for controlling the power management module in servers, telecommunication equipment and other industrial equipment.

The device names, pin counts, memory sizes and peripheral availability of each device are listed below. The following pages show their pinout diagrams.

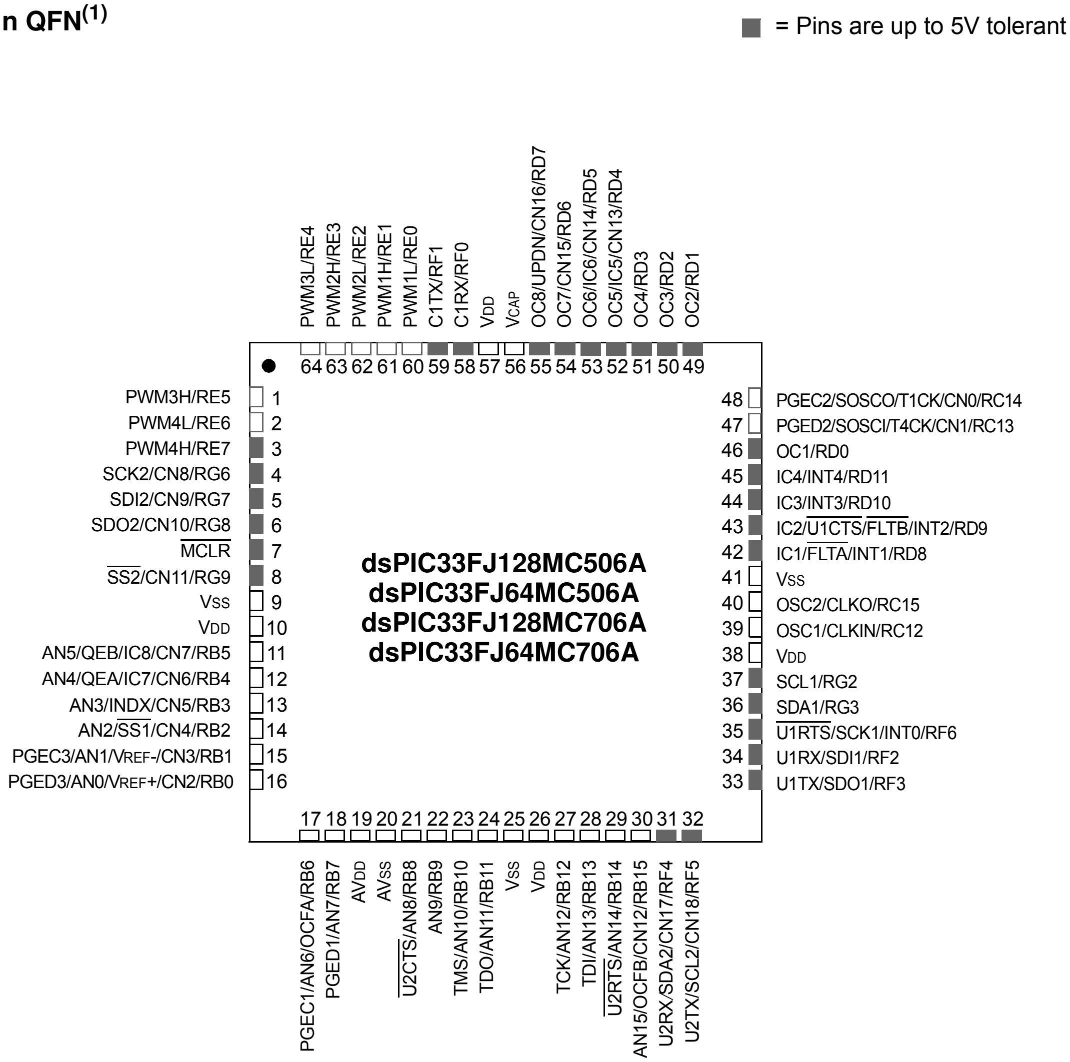
dsPIC33FJXXXMCX06A/X08A/X10A Controller Families

Device	Pins	Program Flash Memory (Kbyte)	RAM (Kbyte)(1)	Timer 16-bit	Input Capture	Output Compare Std. PWM	Motor Control PWM	Quadrature Encoder Interface	Codec Interface	ADC	UART	SPI	I^2C™	Enhanced CAN	I/O Pins (Max)(2)	Packages
dsPIC33FJ64MC506A	64	64	8	9	8	8	8 ch	1	0	1 ADC, 16 ch	2	2	2	1	53	PT, MR
dsPIC33FJ64MC508A	80	64	8	9	8	8	8 ch	1	0	1 ADC, 18 ch	2	2	2	1	69	PT
dsPIC33FJ64MC510A	100	64	8	9	8	8	8 ch	1	0	1 ADC, 24 ch	2	2	2	1	85	PF, PT
dsPIC33FJ64MC706A	64	64	16	9	8	8	8 ch	1	0	2 ADC, 16 ch	2	2	2	1	53	PT, MR
dsPIC33FJ64MC710A	100	64	16	9	8	8	8 ch	1	0	2 ADC, 24 ch	2	2	2	2	85	PF, PT
dsPIC33FJ128MC506A	64	128	8	9	8	8	8 ch	1	0	1 ADC, 16 ch	2	2	2	1	53	PT, MR
dsPIC33FJ128MC510A	100	128	8	9	8	8	8 ch	1	0	1 ADC, 24 ch	2	2	2	1	85	PF, PT
dsPIC33FJ128MC706A	64	128	16	9	8	8	8 ch	1	0	2 ADC, 16 ch	2	2	2	1	53	PT, MR
dsPIC33FJ128MC708A	80	128	16	9	8	8	8 ch	1	0	2 ADC, 18 ch	2	2	2	2	69	PT
dsPIC33FJ128MC710A	100	128	16	9	8	8	8 ch	1	0	2 ADC, 24 ch	2	2	2	2	85	PF, PT
dsPIC33FJ256MC510A	100	256	16	9	8	8	8 ch	1	0	1 ADC, 24 ch	2	2	2	1	85	PF, PT
dsPIC33FJ256MC710A	100	256	30	9	8	8	8 ch	1	0	2 ADC, 24 ch	2	2	2	2	85	PF, PT

Note 1: RAM size is inclusive of 2 Kbytes DMA RAM.
2: Maximum I/O pin count includes pins shared by the peripheral functions.

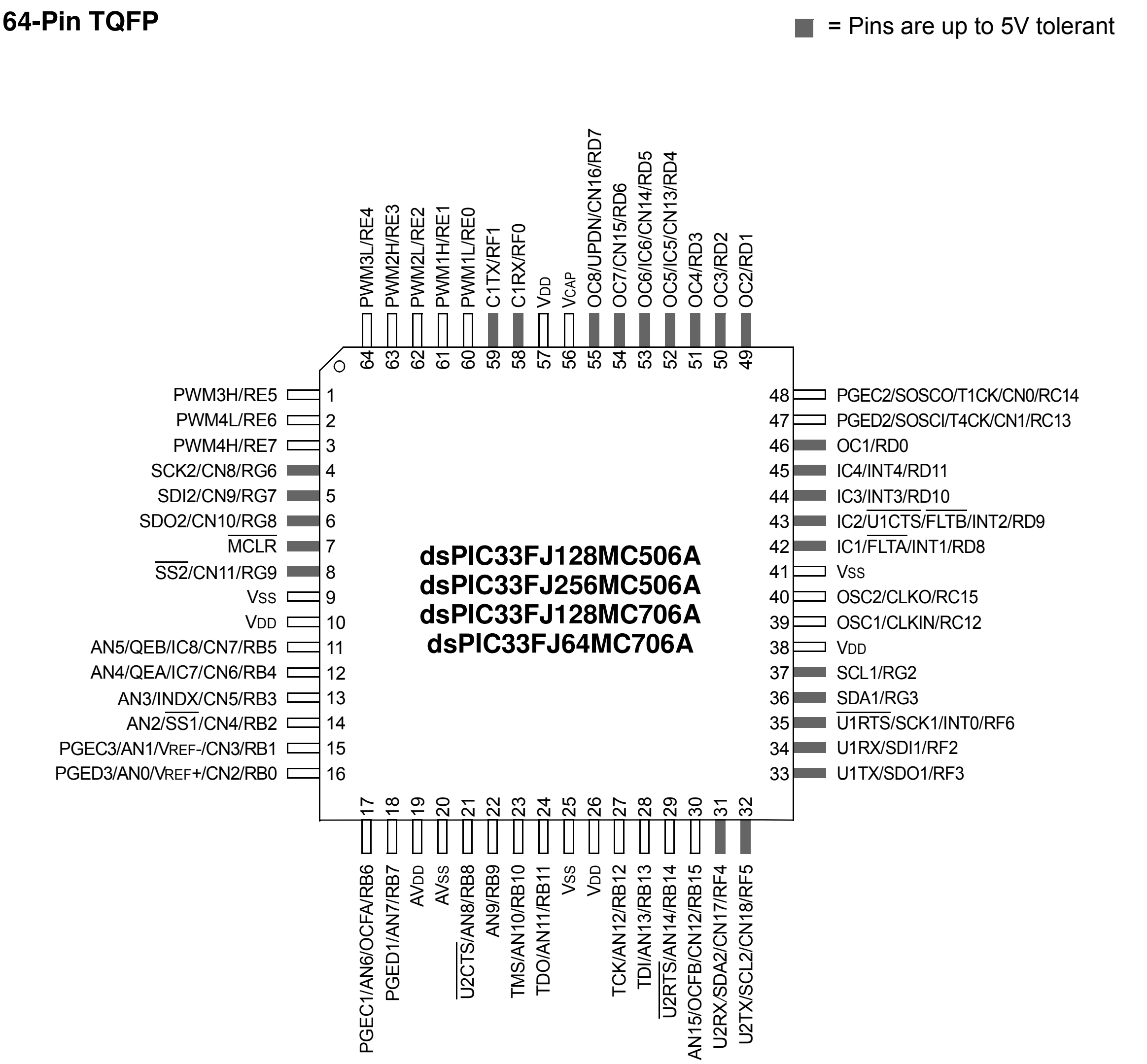
Pin Diagrams

64-Pin QFN(1)

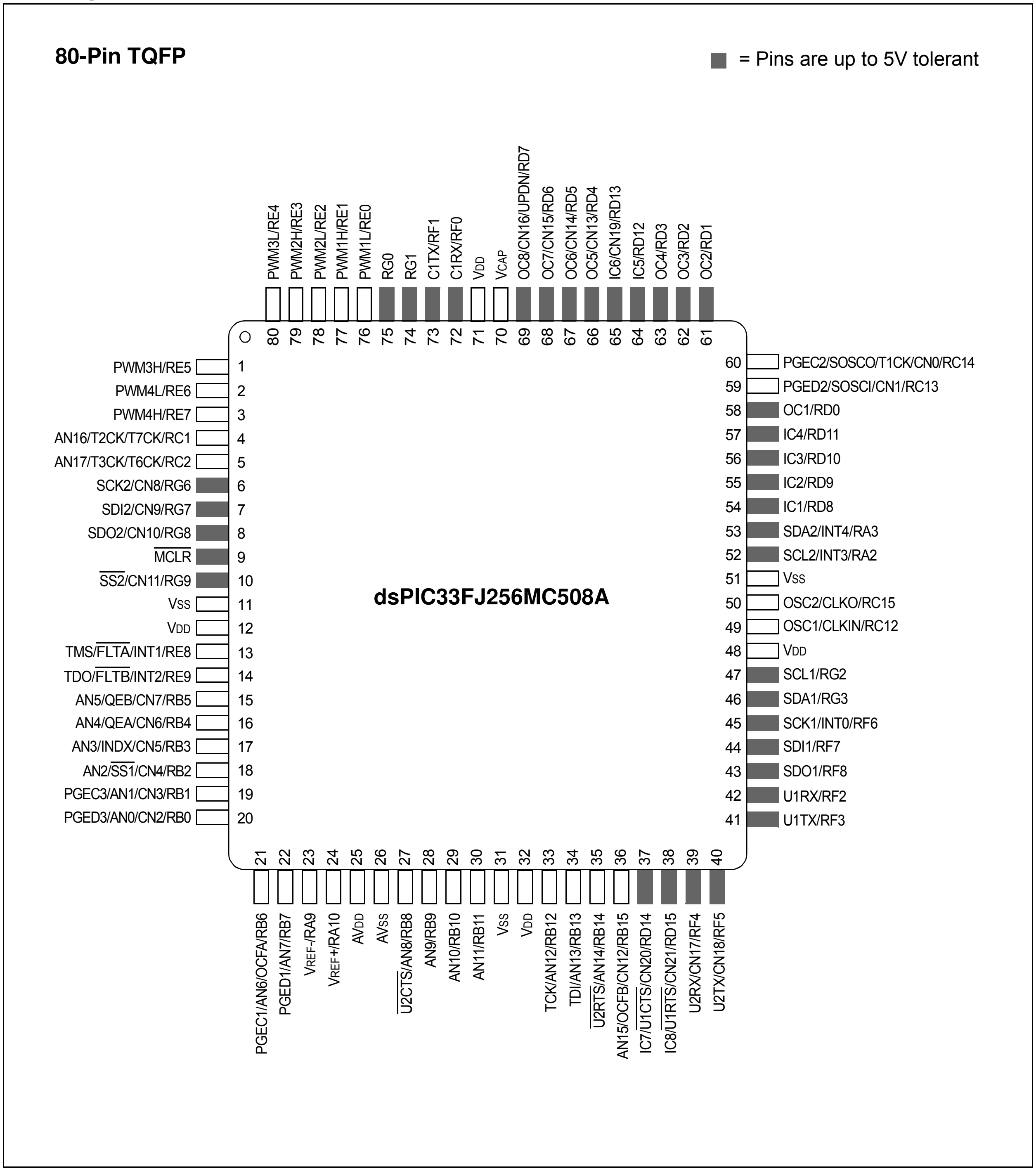


Note 1: The metal plane at the bottom of the device is not connected to any pins and should be connected to VSS externally.

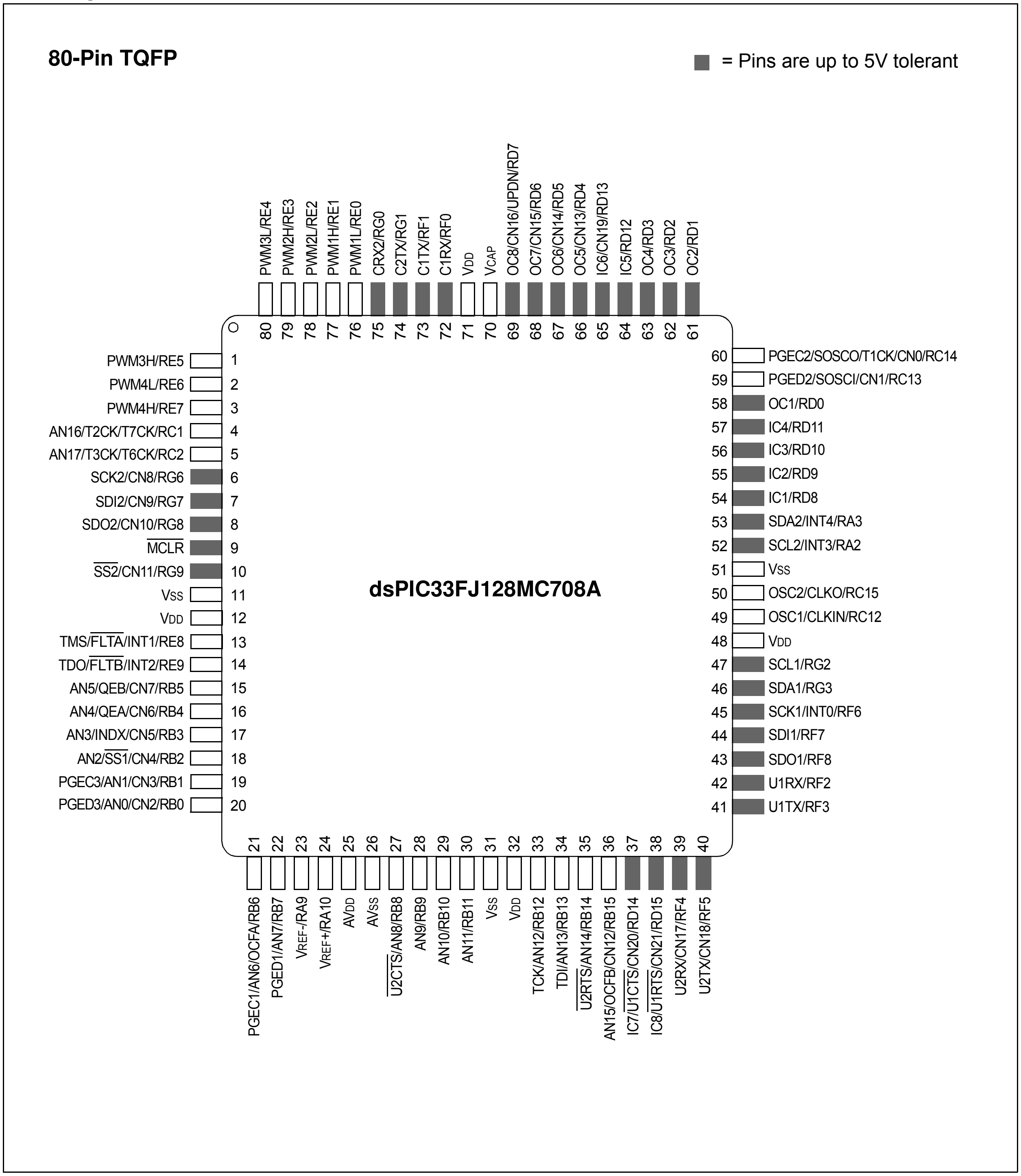
Pin Diagrams (Continued)



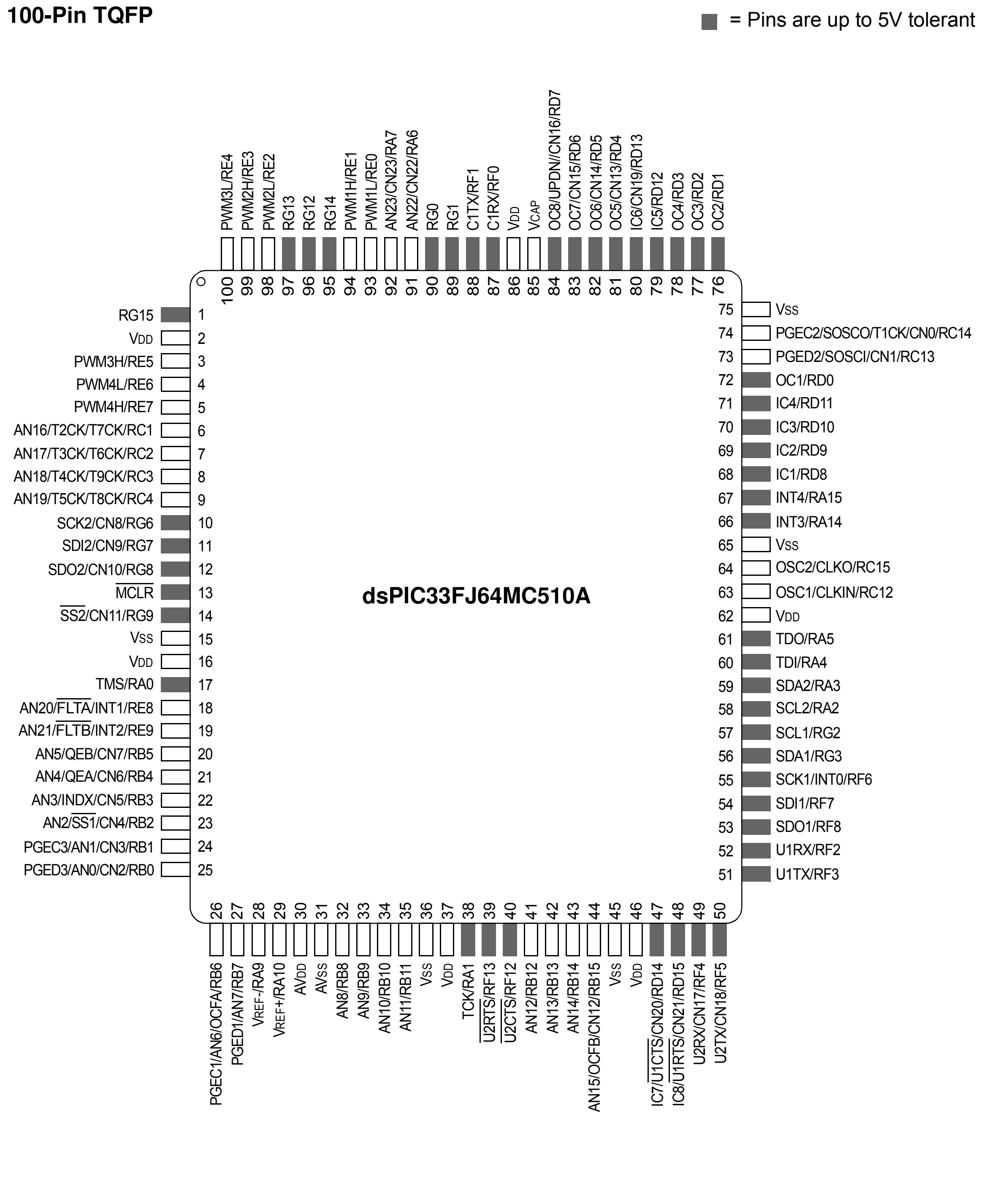
Pin Diagrams (Continued)



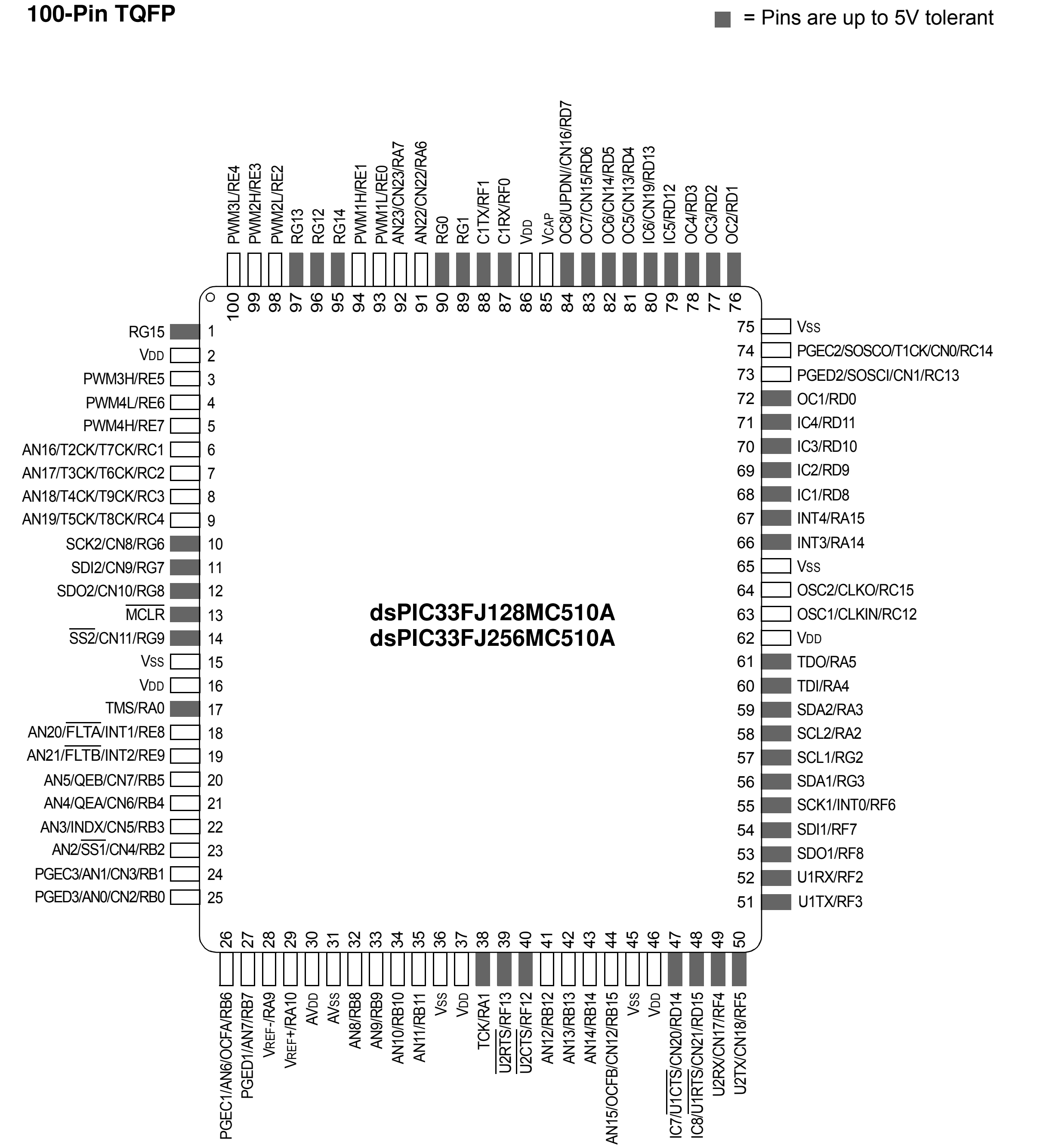
Pin Diagrams (Continued)



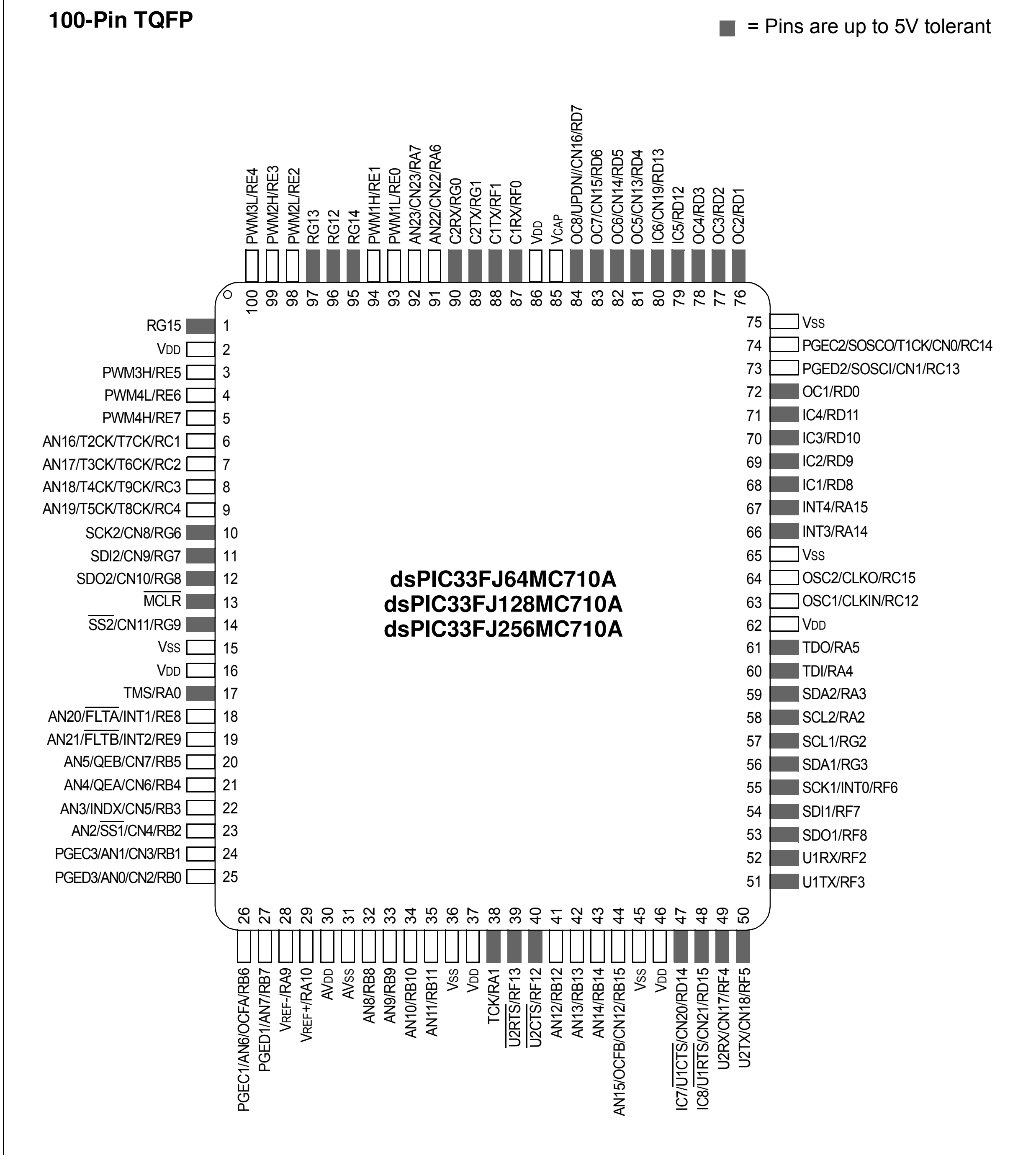
Pin Diagrams (Continued)



Pin Diagrams (Continued)



Pin Diagrams (Continued)



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Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33F/PIC24H Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note:	To access the documents listed below, browse to the documentation section of the dsPIC33FJ256MC710A product page on the Microchip web site (www.microchip.com) or select a family reference manual section from the following list. In addition to parameters, features, and other documentation, the resulting page provides links to the related family reference manual sections.

- **Section 1. "Introduction"** (DS70197)
- **Section 2. "CPU"** (DS70204)
- **Section 3. "Data Memory"** (DS70202)
- **Section 4. "Program Memory"** (DS70203)
- **Section 5. "Flash Programming"** (DS70191)
- **Section 6. "Interrupts"** (DS70184)
- **Section 7. "Oscillator"** (DS70186)
- **Section 8. "Reset"** (DS70192)
- **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70196)
- **Section 10. "I/O Ports"** (DS70193)
- **Section 11. "Timers"** (DS70205)
- **Section 12. "Input Capture"** (DS70198)
- **Section 13. "Output Compare"** (DS70209)
- **Section 14. "Motor Control PWM"** (DS70187)
- **Section 15. "Quadrature Encoder Interface (QEI)"** (DS70208)
- **Section 16. "Analog-to-Digital Converter (ADC)"** (DS70183)
- **Section 17. "UART"** (DS70188)
- **Section 18. "Serial Peripheral Interface (SPI)"** (DS70206)
- **Section 19. "Inter-Integrated Circuit™ (I2C™)"** (DS70195)
- **Section 20. "Data Converter Interface (DCI)"** (DS70288)
- **Section 21. "Enhanced Controller Area Network (ECAN™)"** (DS70185)
- **Section 22. "Direct Memory Access (DMA)"** (DS70182)
- **Section 23. "CodeGuard™ Security"** (DS70199)
- **Section 24. "Programming and Diagnostics"** (DS70207)
- **Section 25. "Device Configuration"** (DS70194)

1.0 DEVICE OVERVIEW

> **Note 1:** This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F/PIC24H Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the following devices:

- dsPIC33FJ64MC506A
- dsPIC33FJ64MC508A
- dsPIC33FJ64MC510A
- dsPIC33FJ64MC706A
- dsPIC33FJ64MC710A
- dsPIC33FJ128MC506A
- dsPIC33FJ128MC510A
- dsPIC33FJ128MC706A
- dsPIC33FJ128MC708A
- dsPIC33FJ128MC710A
- dsPIC33FJ256MC510A
- dsPIC33FJ256MC710A

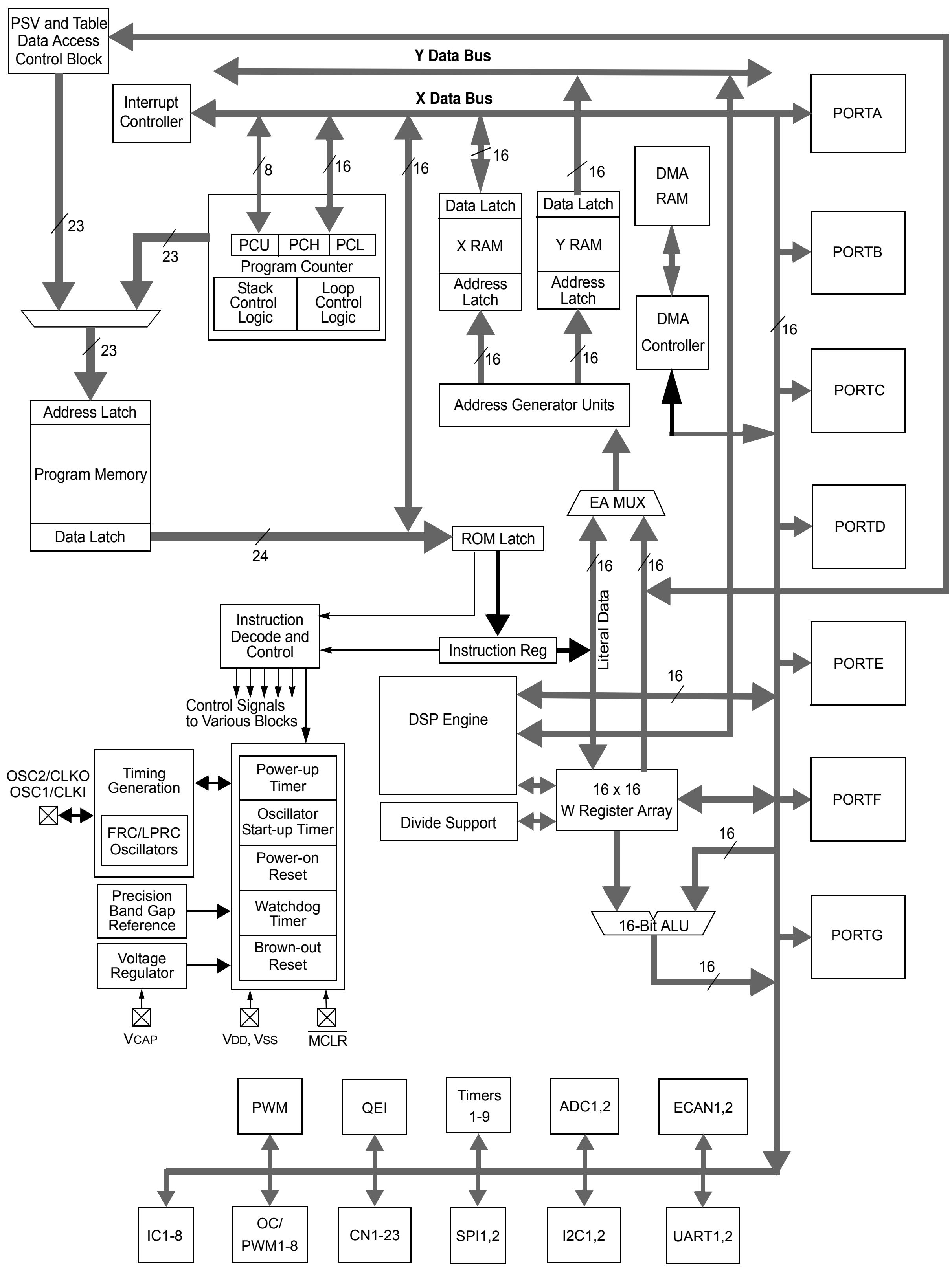
The dsPIC33FJXXXMCX06A/X08A/X10A includes devices with a wide range of pin counts (64, 80 and 100), different program memory sizes (64 Kbytes, 128 Kbytes and 256 Kbytes) and different RAM sizes (8 Kbytes, 16 Kbytes and 30 Kbytes).

These features make this family suitable for a wide variety of high-performance, digital signal control applications. The devices are pin compatible with the PIC24H family of devices, and also share a very high degree of compatibility with the dsPIC30F family devices. This allows easy migration between device families as may be necessitated by the specific functionality, computational resource and system cost requirements of the application.

The dsPIC33FJXXXMCX06A/X08A/X10A family of devices employs a powerful 16-bit architecture that seamlessly integrates the control features of a Microcontroller (MCU) with the computational capabilities of a Digital Signal Processor (DSP). The resulting functionality is ideal for applications that rely on high-speed, repetitive computations, as well as control.

The DSP engine, dual 40-bit accumulators, hardware support for division operations, barrel shifter, 17 x 17 multiplier, a large array of 16-bit working registers and a wide variety of data addressing modes, together, provide the dsPIC33FJXXXMCX06A/X08A/X10A Central Processing Unit (CPU) with extensive mathematical processing capability. Flexible and deterministic interrupt handling, coupled with a powerful array of peripherals, renders the dsPIC33FJXXXMCX06A/X08A/X10A devices suitable for control applications. Further, Direct Memory Access (DMA) enables overhead-free transfer of data between several peripherals and a dedicated DMA RAM. Reliable, field programmable Flash program memory ensures scalability of applications that use dsPIC33FJXXXMCX06A/X08A/X10A devices.

FIGURE 1-1: dsPIC33FJXXXMCX06A/X08A/X10A GENERAL BLOCK DIAGRAM



Note: Not all pins or features are implemented on all device pinout configurations. See pinout diagrams for the specific pins and features present on each device.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	Description
AN0-AN31	I	Analog	Analog input channels.
AVDD	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	Ground reference for analog modules.
CLKI CLKO	I O	ST/CMOS —	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
CN0-CN23	I	ST	Input change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
C1RX C1TX C2RX C2TX	I O I O	ST — ST —	ECAN1 bus receive pin. ECAN1 bus transmit pin. ECAN2 bus receive pin. ECAN2 bus transmit pin.
PGED1 PGEC1 PGED2 PGEC2 PGED3 PGEC3	I/O I I/O I I/O I	ST ST ST ST ST ST	Data I/O pin for Programming/Debugging Communication Channel 1. Clock input pin for Programming/Debugging Communication Channel 1. Data I/O pin for Programming/Debugging Communication Channel 2. Clock input pin for Programming/Debugging Communication Channel 2. Data I/O pin for Programming/Debugging Communication Channel 3. Clock input pin for Programming/Debugging Communication Channel 3.
IC1-IC8	I	ST	Capture Inputs 1 through 8.
INDX QEA QEB UPDN	I I I O	ST ST ST CMOS	Quadrature Encoder Index Pulse input. Quadrature Encoder Phase A input in QEI mode. Auxiliary timer external clock/gate input in Timer mode. Quadrature Encoder Phase A input in QEI mode. Auxiliary timer external clock/gate input in Timer mode. Position up/down counter direction state.
INT0 INT1 INT2 INT3 INT4	I I I I I	ST ST ST ST ST	External Interrupt 0. External Interrupt 1. External Interrupt 2. External Interrupt 3. External Interrupt 4.
$\overline{\text{FLTA}}$ $\overline{\text{FLTB}}$ PWM1L PWM1H PWM2L PWM2H PWM3L PWM3H PWM4L PWM4H	I I O O O O O O O O	ST ST — — — — — — — —	PWM Fault A input. PWM Fault B input. PWM1 low output. PWM1 high output. PWM2 low output. PWM2 high output. PWM3 low output. PWM3 high output. PWM4 low output. PWM4 high output.
$\overline{\text{MCLR}}$	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
OCFA OCFB OC1-OC8	I I O	ST ST —	Compare Fault A input (for Compare Channels 1, 2, 3 and 4). Compare Fault B input (for Compare Channels 5, 6, 7 and 8). Compare outputs 1 through 8.
OSC1 OSC2	I I/O	ST/CMOS —	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.

Legend: CMOS = CMOS compatible input or output   Analog = Analog input   P = Power
ST = Schmitt Trigger input with CMOS levels   O = Output   I = Input

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
RA0-RA7 RA9-RA10 RA12-RA15	I/O I/O I/O	ST ST ST	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.
RC1-RC4 RC12-RC15	I/O I/O	ST ST	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE9	I/O	ST	PORTE is a bidirectional I/O port.
RF0-RF8 RF12-RF13	I/O	ST	PORTF is a bidirectional I/O port.
RG0-RG3 RG6-RG9 RG12-RG15	I/O I/O I/O	ST ST ST	PORTG is a bidirectional I/O port.
SCK1 SDI1 SDO1 $\overline{\text{SS1}}$ SCK2 SDI2 SDO2 $\overline{\text{SS2}}$	I/O I O I/O I/O I O I/O	ST ST — ST ST ST — ST	Synchronous serial clock input/output for SPI1. SPI1 data in. SPI1 data out. SPI1 slave synchronization or frame pulse I/O. Synchronous serial clock input/output for SPI2. SPI2 data in. SPI2 data out. SPI2 slave synchronization or frame pulse I/O.
SCL1 SDA1 SCL2 SDA2	I/O I/O I/O I/O	ST ST ST ST	Synchronous serial clock input/output for I2C1. Synchronous serial data input/output for I2C1. Synchronous serial clock input/output for I2C2. Synchronous serial data input/output for I2C2.
SOSCI SOSCO	I O	ST/CMOS —	32.768 kHz low-power oscillator crystal input; CMOS otherwise. 32.768 kHz low-power oscillator crystal output.
TMS TCK TDI TDO	I I I O	ST ST ST —	JTAG Test mode select pin. JTAG test clock input pin. JTAG test data input pin. JTAG test data output pin.
T1CK T2CK T3CK T4CK T5CK T6CK T7CK T8CK T9CK	I I I I I I I I I	ST ST ST ST ST ST ST ST ST	Timer1 external clock input. Timer2 external clock input. Timer3 external clock input. Timer4 external clock input. Timer5 external clock input. Timer6 external clock input. Timer7 external clock input. Timer8 external clock input. Timer9 external clock input.
$\overline{\text{U1CTS}}$ $\overline{\text{U1RTS}}$ U1RX U1TX $\overline{\text{U2CTS}}$ $\overline{\text{U2RTS}}$ U2RX U2TX	I O I O I O I O	ST — ST — ST — ST —	UART1 clear to send. UART1 ready to send. UART1 receive. UART1 transmit. UART2 clear to send. UART2 ready to send. UART2 receive. UART2 transmit.
VDD	P	—	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	CPU logic filter capacitor connection.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power; ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
VSS	P	—	Ground reference for logic and I/O pins.
VREF+	I	Analog	Analog voltage reference (high) input.
VREF-	I	Analog	Analog voltage reference (low) input.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input

NOTES:

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/X10A family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33FJXXXMCX06A/X08A/X10A family of 16-bit Digital Signal Controllers (DSC) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used) (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used (see **Section 2.6 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins used when external voltage reference for ADC module is implemented

Note: The AVDD and AVSS pins must be connected independent of the ADC voltage reference source.

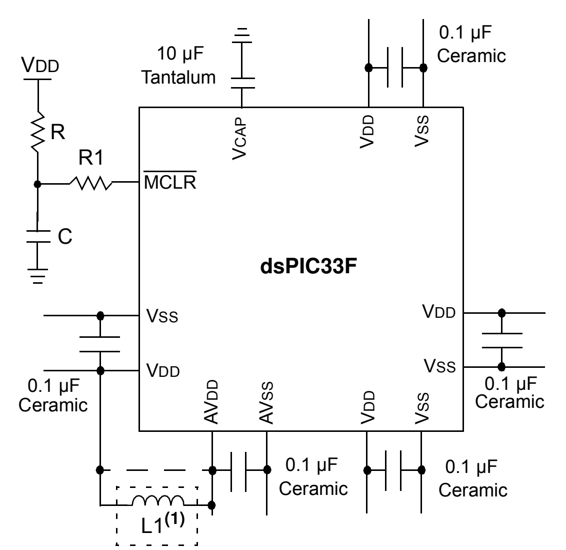
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{F_{CNV}}{2} \quad \text{(i.e., ADC conversion rate/2)}$$

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 5 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor between 4.7 µF and 10 µF, 16V connected to ground. The type can be ceramic or tantalum. Refer to **Section 26.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP. It is recommended that the trace length not exceed one-quarter inch (6 mm). Refer to **Section 23.2 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

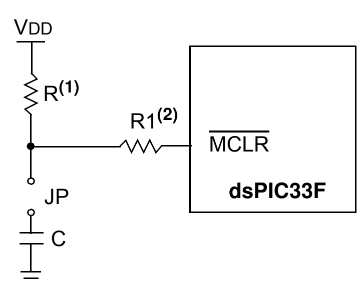
- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor, C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for information on capacitive loading limits, and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to the MPLAB® ICD 3 or REAL ICE™ in-circuit emulator.

For more information on the ICD 3 and REAL ICE in-circuit emulator connection requirements, refer to the following documents that are available on the Microchip web site.

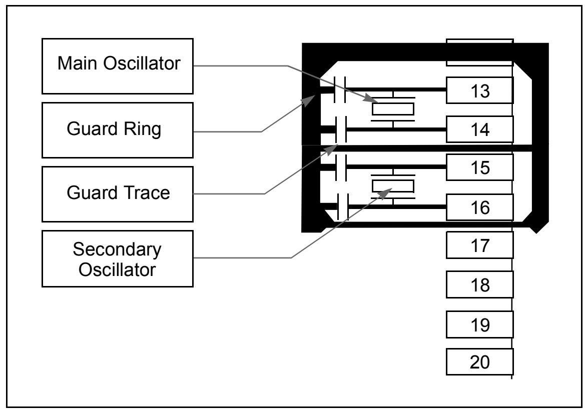
- *"Using MPLAB® ICD 3"* (poster) (DS51765)
- *"MPLAB® ICD 3 Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* (DS51616)
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) (DS51749)

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 9.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to ≤ 8 MHz for start-up with PLL enabled to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start-up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLDBF to a suitable value, and then perform a clock switch to the oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Configuration of Analog and Digital Pins During ICSP Operations

If the MPLAB ICD 3 or REAL ICE in-circuit emulator is selected as a debugger, it automatically initializes all of the A/D input pins (ANx) as “digital” pins by setting all bits in the AD1PCFGL register.

The bits in this register that correspond to the A/D pins that are initialized by the MPLAB ICD 3 or REAL ICE in-circuit emulator, must not be cleared by the user application firmware; otherwise, communication errors will result between the debugger and the device.

If your application needs to use certain A/D pins as analog input pins during the debug session, the user application must clear the corresponding bits in the AD1PCFGL register during initialization of the ADC module.

When the MPLAB ICD 3 or REAL ICE in-circuit emulator is used as a programmer, the user application firmware must correctly configure the AD1PCFGL register. Automatic initialization of this register is only done during debugger operation. Failure to correctly configure the register(s) will result in all A/D pins being recognized as analog input pins, resulting in the port value being read as a logic ‘0’, which may affect user application functionality.

2.9 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between VSS and the unused pins.

3.0 CPU

> **Note 1:** This data sheet summarizes the features of the dsPIC33FJXXXMCX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS70204) in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33FJXXXMCX06A/X08A/X10A CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double word move (`MOV.D`) instruction and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

The dsPIC33FJXXXMCX06A/X08A/X10A devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

The dsPIC33FJXXXMCX06A/X08A/X10A instruction set has two classes of instructions: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum 'C' compiler efficiency. For most instructions, the dsPIC33FJXXXMCX06A/X08A/X10A devices are capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1 and the programmer's model for the dsPIC33FJXXXMCX06A/X08A/X10A is shown in Figure 3-2.

3.1 Data Addressing Overview

The data space can be addressed as 32K words or 64 Kbytes, and is split into two blocks referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page register (PSVPAG). The program to data space mapping feature lets any instruction access program space as if it were data space.

The data space also includes 2 Kbytes of DMA RAM, which is primarily used for DMA data transfers but may be used as general purpose RAM.

3.2 DSP Engine Overview

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value up to 16 bits right or left in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The `MAC` instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers, and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM memory data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

3.3 Special MCU Features

The dsPIC33FJXXXMCX06A/X08A/X10A devices feature a 17-bit by 17-bit, single-cycle multiplier that is shared by both the MCU ALU and DSP engine. The multiplier can perform signed, unsigned and mixed sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication not only allows you to perform mixed sign multiplication, it also achieves accurate results for special operations, such as (-1.0) x (-1.0).

The dsPIC33FJXXXMCX06A/X08A/X10A devices support 16/16 and 32/16 divide operations, both fractional and integer. All divide instructions are iterative operations. They must be executed within a `REPEAT` loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without a loss of data.

A 40-bit barrel shifter is used to perform up to a 16-bit left or right shift in a single cycle. The barrel shifter can be used by both MCU and DSP instructions.

FIGURE 3-1: dsPIC33FJXXXMCX06A/X08A/X10A CPU CORE BLOCK DIAGRAM

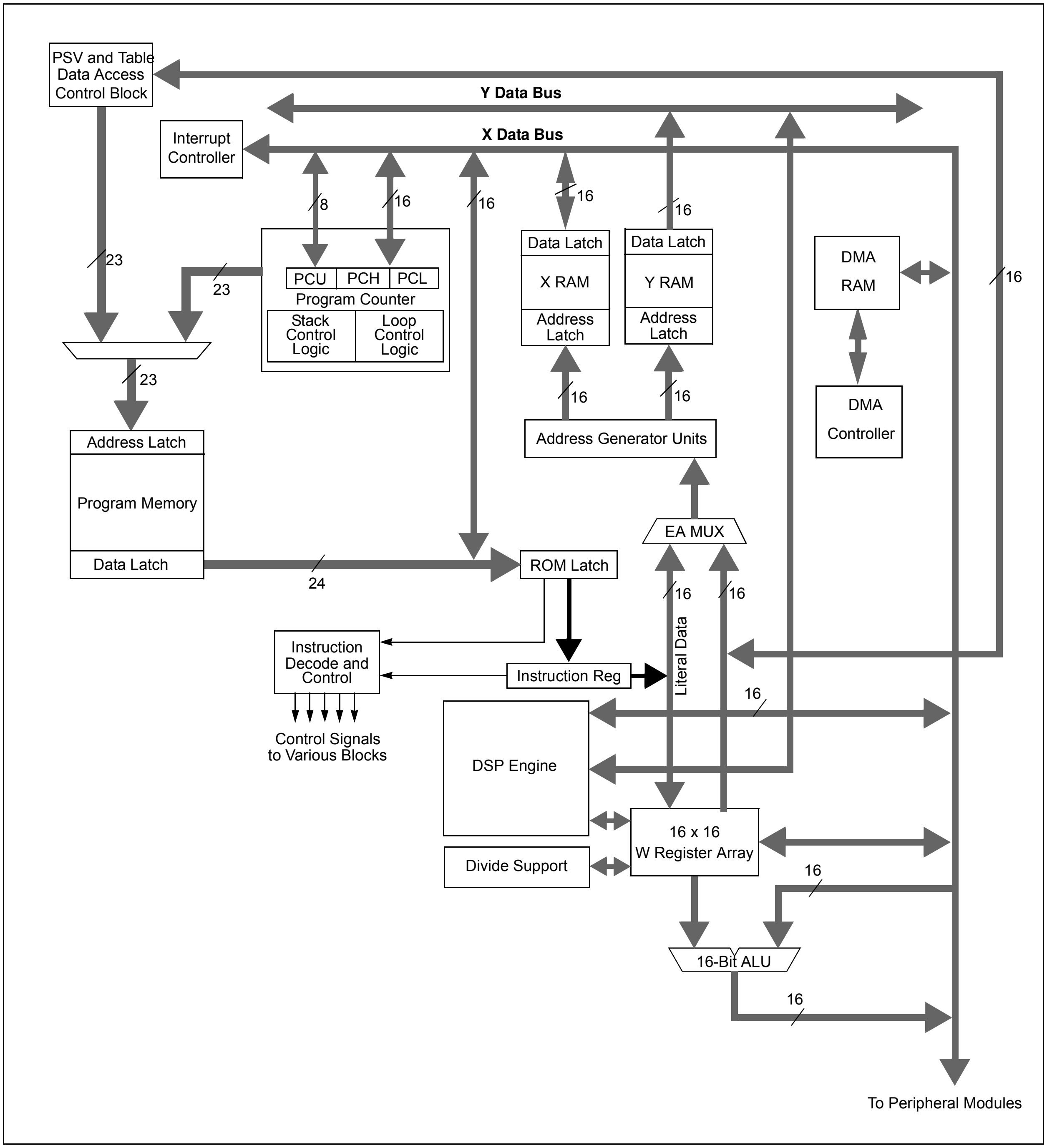


FIGURE 3-2: dsPIC33FJXXXMCX06A/X08A/X10A PROGRAMMER'S MODEL