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dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610

16-Bit Digital Signal Controllers with High-Speed PWM, ADC and Comparators

Operating Conditions

- 3.0V to 3.6V, -40ºC to +85ºC, DC to 50 MIPS
- 3.0V to 3.6V, -40ºC to +125ºC, DC to 40 MIPS

Core: 16-Bit dsPIC33F

- Code-Efficient (C and Assembly) Architecture
- Two 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle Mixed-Sign MUL plus Hardware Divide
- 32-Bit Multiply Support

Clock Management

- ±1% Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer (WDT)
- Fast Wake-up and Start-up

Power Management

- Low-Power Management modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset
- 1.7 mA/MHz Dynamic Current (typical)
- 50 µA IPD Current (typical)

High-Speed PWM

- Up to 9 PWM Pairs with Independent Timing
- Dead Time for Rising and Falling Edges
- 1.04 ns PWM Resolution
- PWM Support for:
  - DC/DC, AC/DC, Inverters, PFC, Lighting
  - BLDC, PMSM, ACIM, SRM
- Programmable Fault Inputs
- Flexible Trigger Configurations for ADC Conversions

Advanced Analog Features

- High-Speed ADC module:
  - 10-bit resolution with up to two Successive Approximation Register (SAR) converters (up to 4 Msps)
  - Up to 24 input channels grouped into 12 conversion pairs plus two voltage reference monitoring inputs
  - Dedicated result buffer for each analog channel
- Flexible and Independent ADC Trigger Sources
- Up to 4 High-Speed Comparators with Direct Connection to the PWM module:
  - 10-bit Digital-to-Analog Converter (DAC) for each comparator
  - DAC reference output
  - Programmable references with 1024 voltage points

Timers/Output Compare/Input Capture

- Six General Purpose Timers:
  - Five 16-bit and up to two 32-bit timers/counters
- Four Output Compare (OC) modules Configurable as Timers/Counters
- Quadrature Encoder Interface (QEI) module Configurable as Timer/Counter
- Four Input Capture (IC) modules

Communication Interfaces

- Two UART modules (12.5 Mbps):
  - With support for LIN/J2602 2.0 protocols and IrDA®
- Two 4-Wire SPI modules (15 Mbps)
- ECAN™ module (1 Mbaud) with ECAN 2.0B Support
- Two I^2C™ modules (up to 1 Mbaud) with SMBus Support

Direct Memory Access (DMA)

- 4-Channel DMA with User-Selectable Priority Arbitration
- UART, SPI, ECAN, IC, OC and Timers

Input/Output

- Sink/Source 18 mA on 18 Pins, 10 mA on 1 Pin or 6 mA on 66 Pins
- 5V Tolerant Pins
- Selectable Open-Drain and Pull-ups
- 29 External Interrupts

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1, -40ºC to +125ºC)
- Class B Safety Library, IEC 60730, VDE Certified

Debugger Development Support

- In-Circuit and In-Application Programming
- Two Program and Two Complex Data Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

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dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. The following pages show their pinout diagrams.

TABLE 1: dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 CONTROLLER FAMILIES

Device	Pins	Program Flash Memory (Kbytes)	RAM (Bytes)	16-Bit Timers	Input Capture	Output Compare	UART	Quadrature Encoder Interfaces	SPI	ECAN™	DMA Channels	PWM	Analog Comparators	External Interrupts	DAC Output	I^2C™	ADC			I/O Pins	Packages
																	SARs	Sample-and-Hold (S&H) Circuits	Analog-to-Digital Inputs		
dsPIC33FJ32GS406	64	32	4K	5	4	4	2	1	2	0	0	6x2	0	5	0	2	1	5	16	58	PT, MR
dsPIC33FJ32GS606	64	32	4K	5	4	4	2	2	2	0	0	6x2	4	5	1	2	2	6	16	58	PT, MR
dsPIC33FJ32GS608	80	32	4K	5	4	4	2	2	2	0	0	8x2	4	5	1	2	2	6	18	74	PT
dsPIC33FJ32GS610	100	32	4K	5	4	4	2	2	2	0	0	9x2	4	5	1	2	2	6	24	85	PT, PF
dsPIC33FJ64GS406	64	64	8K	5	4	4	2	1	2	0	0	6x2	0	5	0	2	1	5	16	58	PT, MR
dsPIC33FJ64GS606	64	64	9K(1)	5	4	4	2	2	2	1	4	6x2	4	5	1	2	2	6	16	58	PT, MR
dsPIC33FJ64GS608	80	64	9K(1)	5	4	4	2	2	2	1	4	8x2	4	5	1	2	2	6	18	74	PT
dsPIC33FJ64GS610	100	64	9K(1)	5	4	4	2	2	2	1	4	9x2	4	5	1	2	2	6	24	85	PT, PF

Note 1: RAM size is inclusive of 1-Kbyte DMA RAM.

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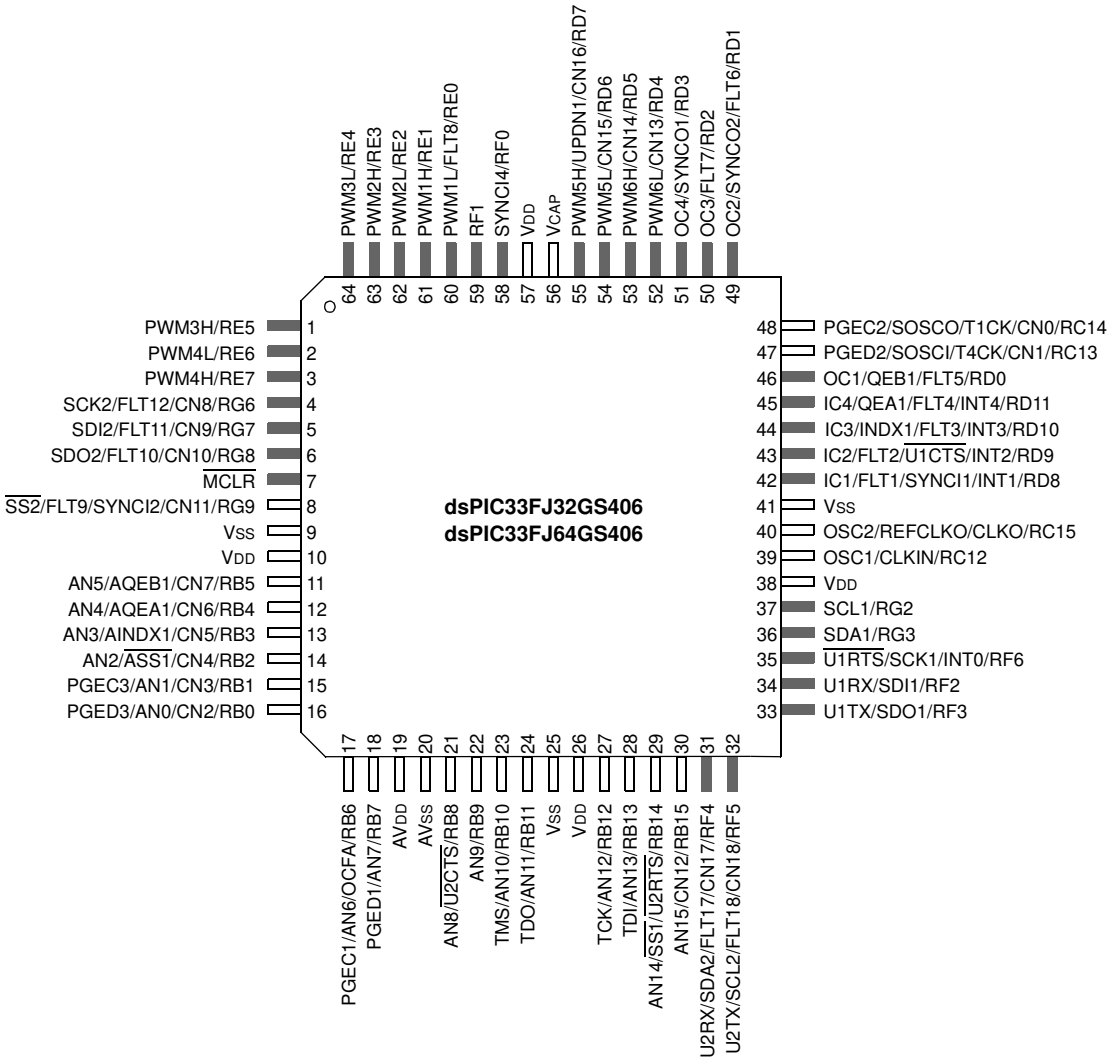
Pin Diagrams

64-Pin TQFP

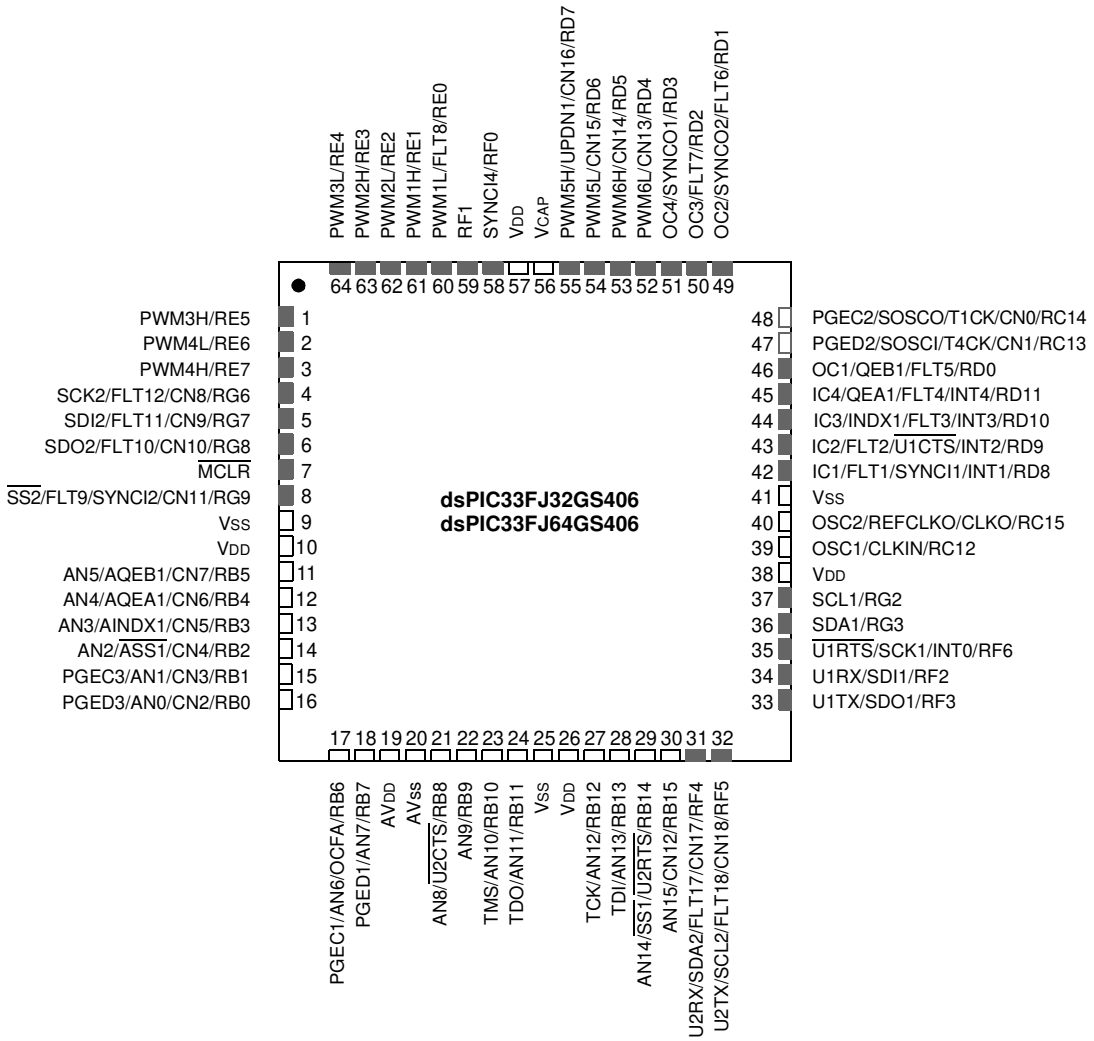
= Pins are up to 5V tolerant



Pin Diagrams (Continued)

64-Pin QFN

■ = Pins are up to 5V tolerant



Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

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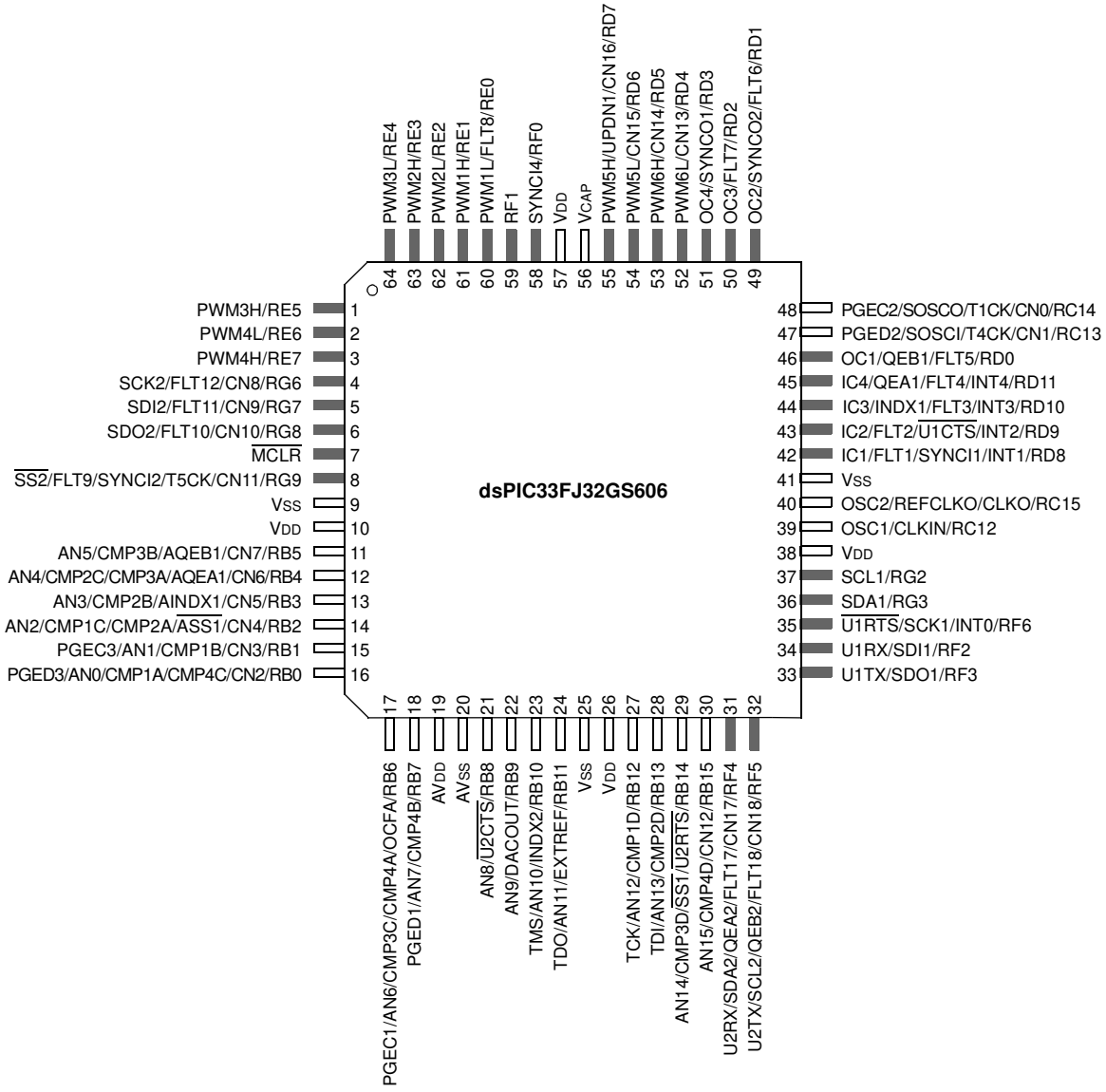
Pin Diagrams (Continued)

64-Pin TQFP

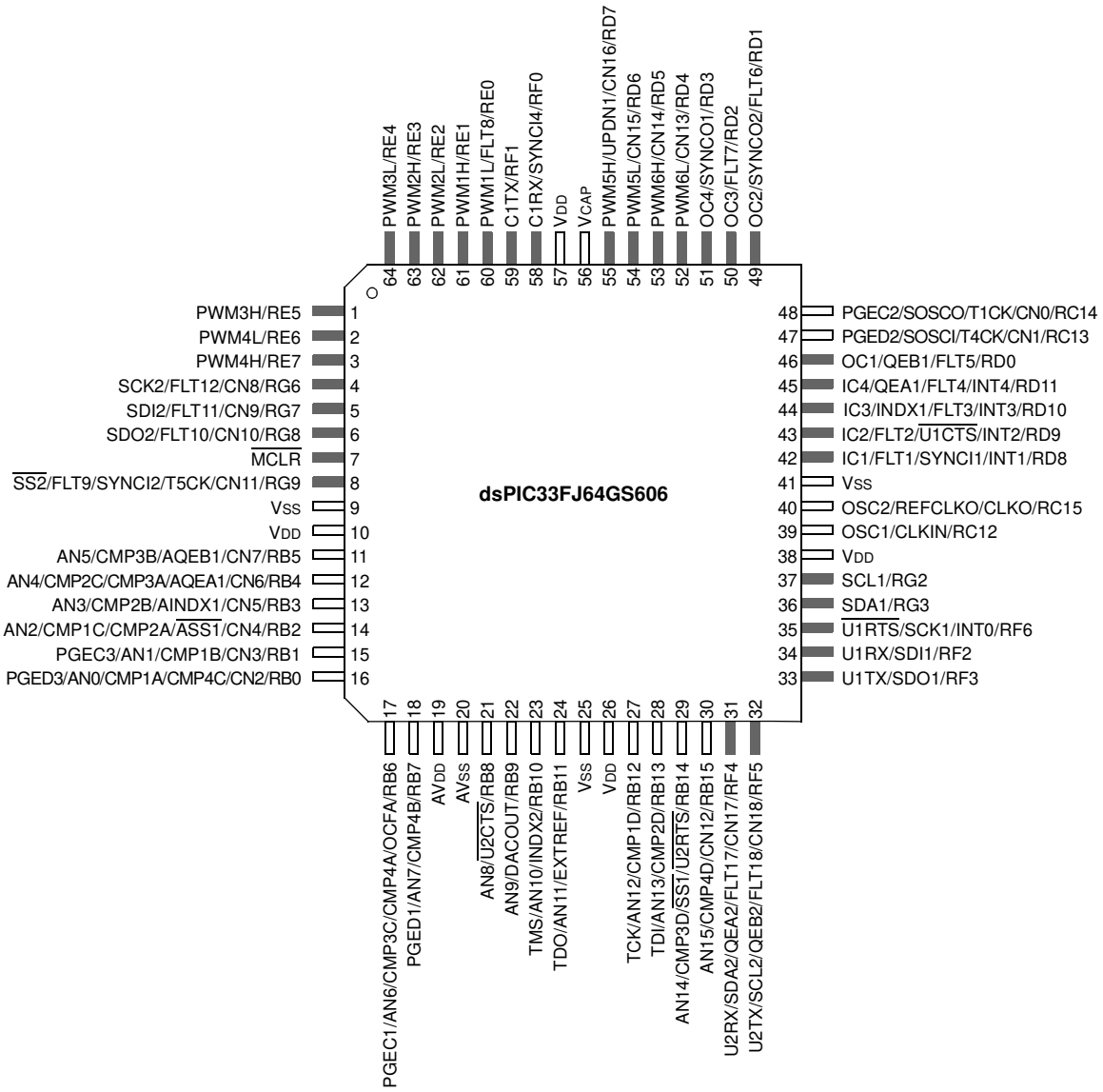
■ = Pins are up to 5V tolerant



Pin Diagrams (Continued)

64-Pin TQFP

= Pins are up to 5V tolerant



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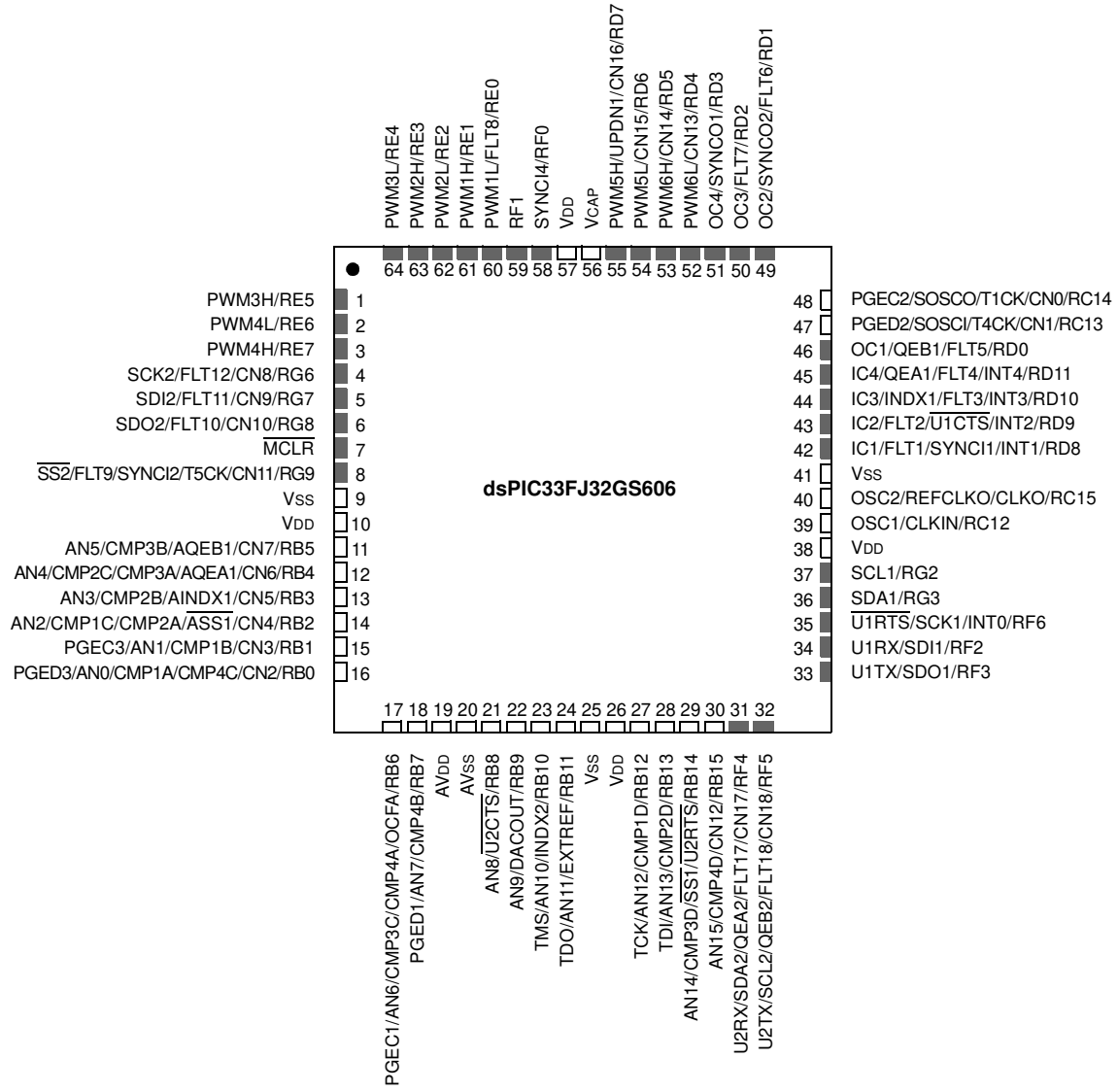
Pin Diagrams (Continued)

64-Pin QFN

■ = Pins are up to 5V tolerant

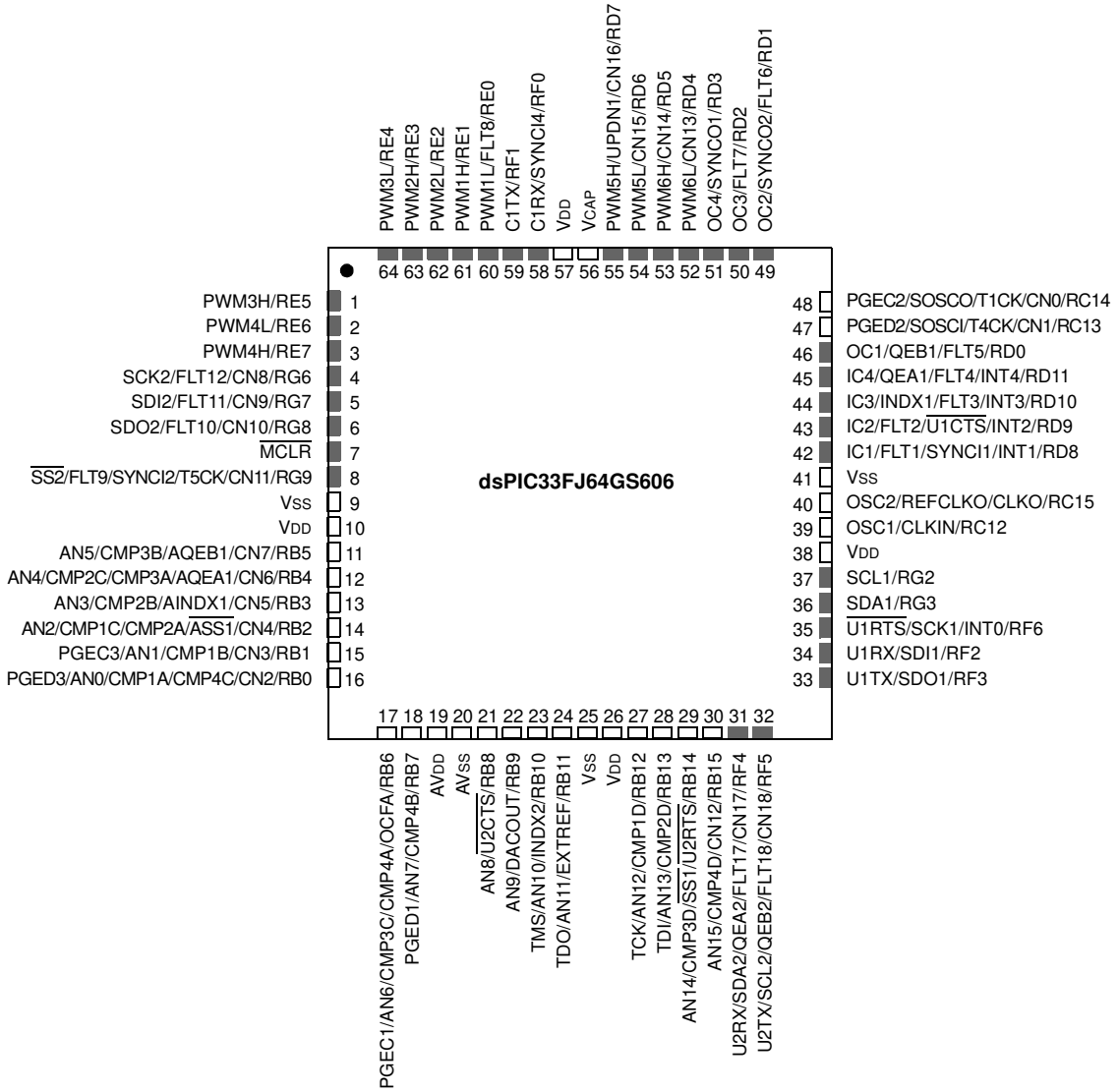


Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

64-Pin QFN

■ = Pins are up to 5V tolerant



Note: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

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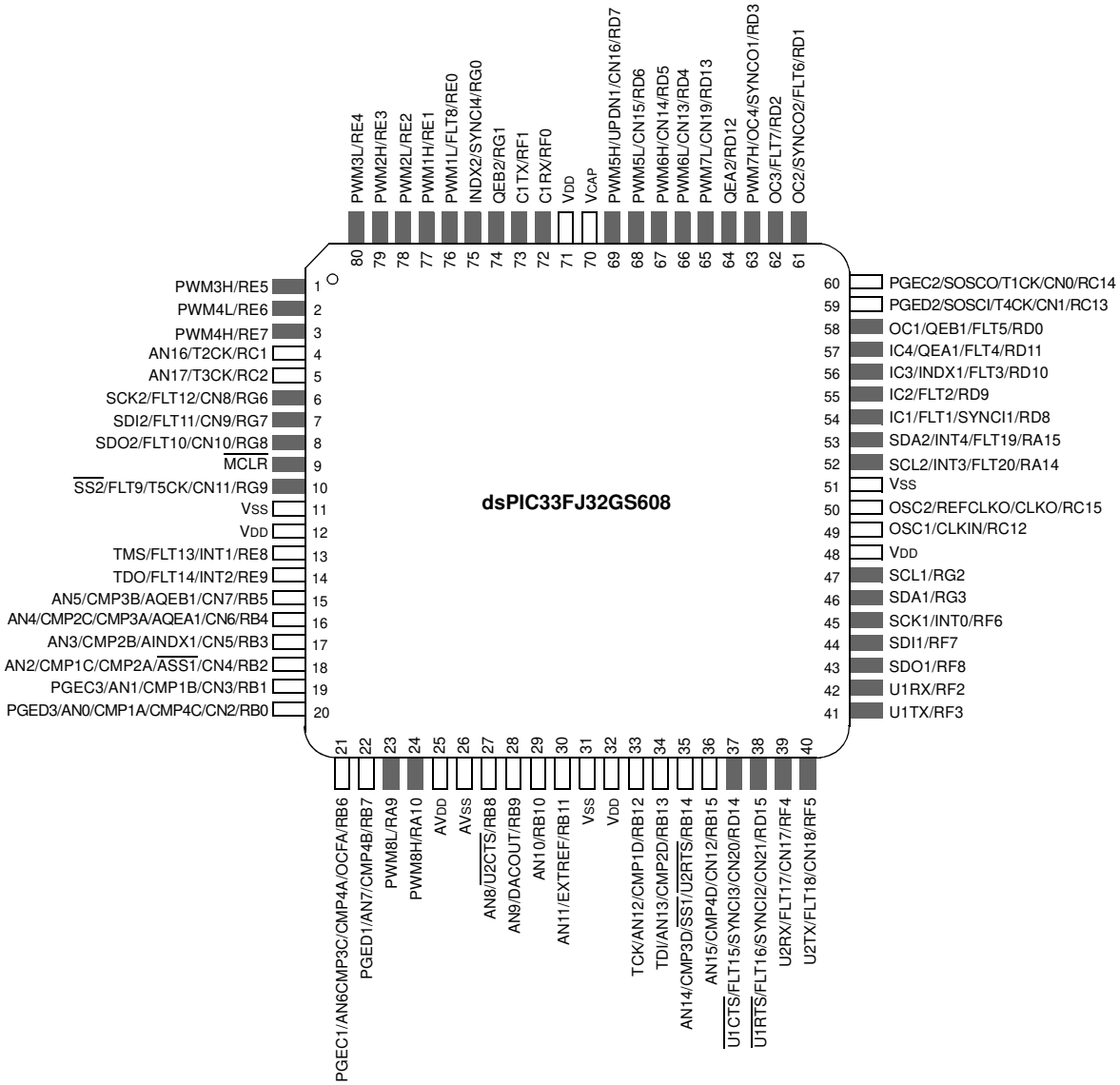
Pin Diagrams (Continued)

80-Pin TQFP

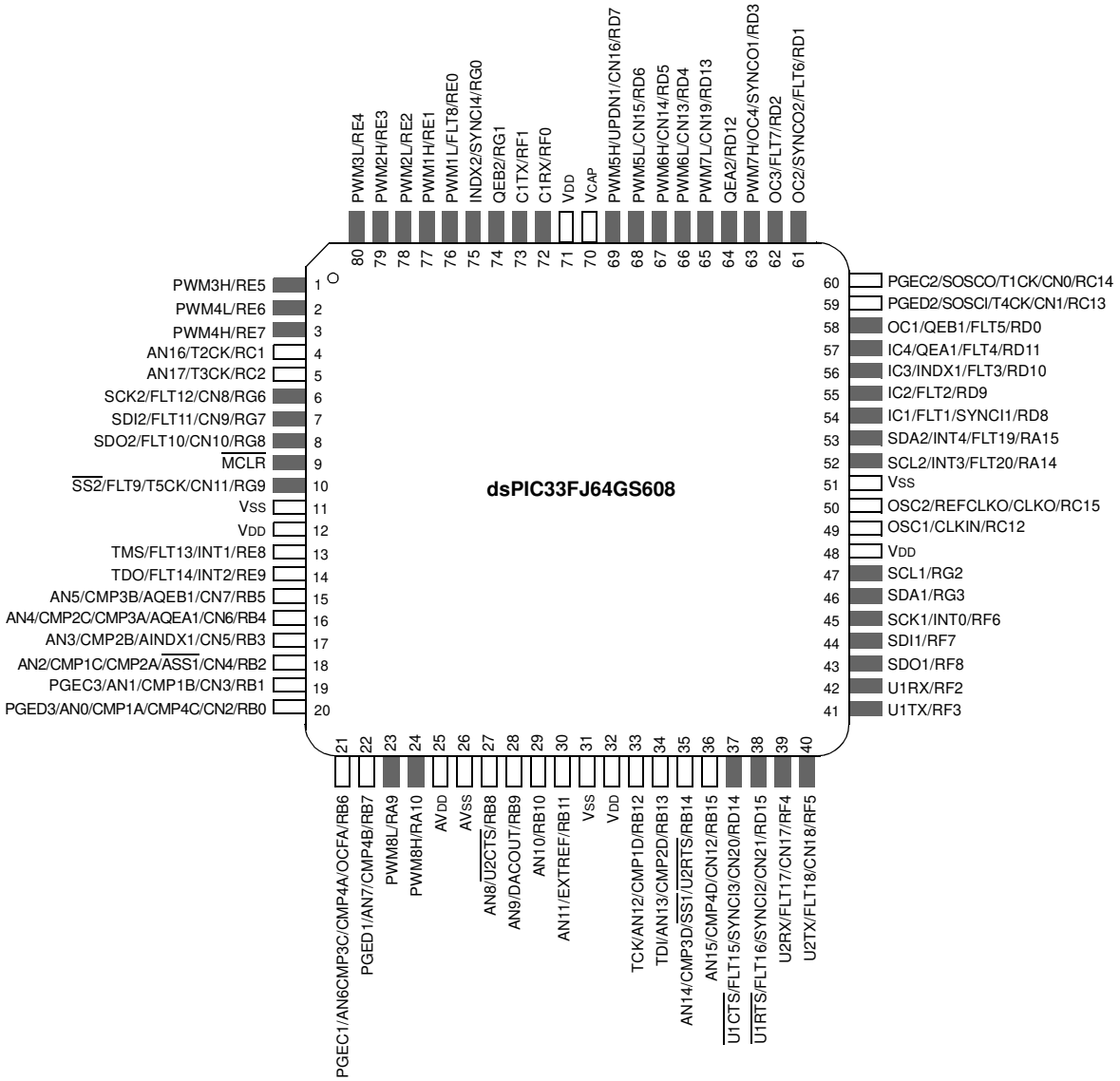
■ = Pins are up to 5V tolerant



Pin Diagrams (Continued)

80-Pin TQFP

■ = Pins are up to 5V tolerant



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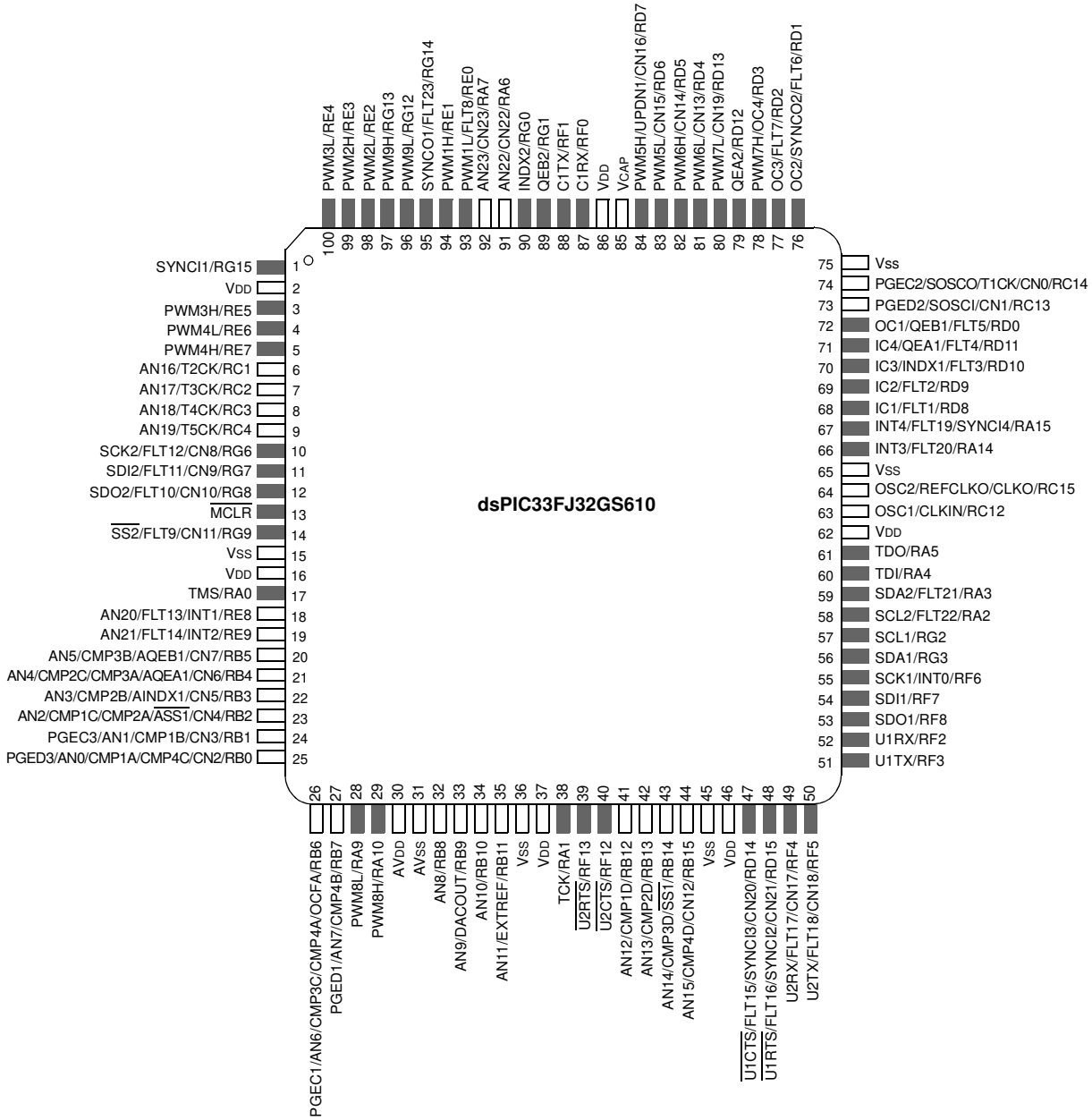
Pin Diagrams (Continued)

100-Pin TQFP

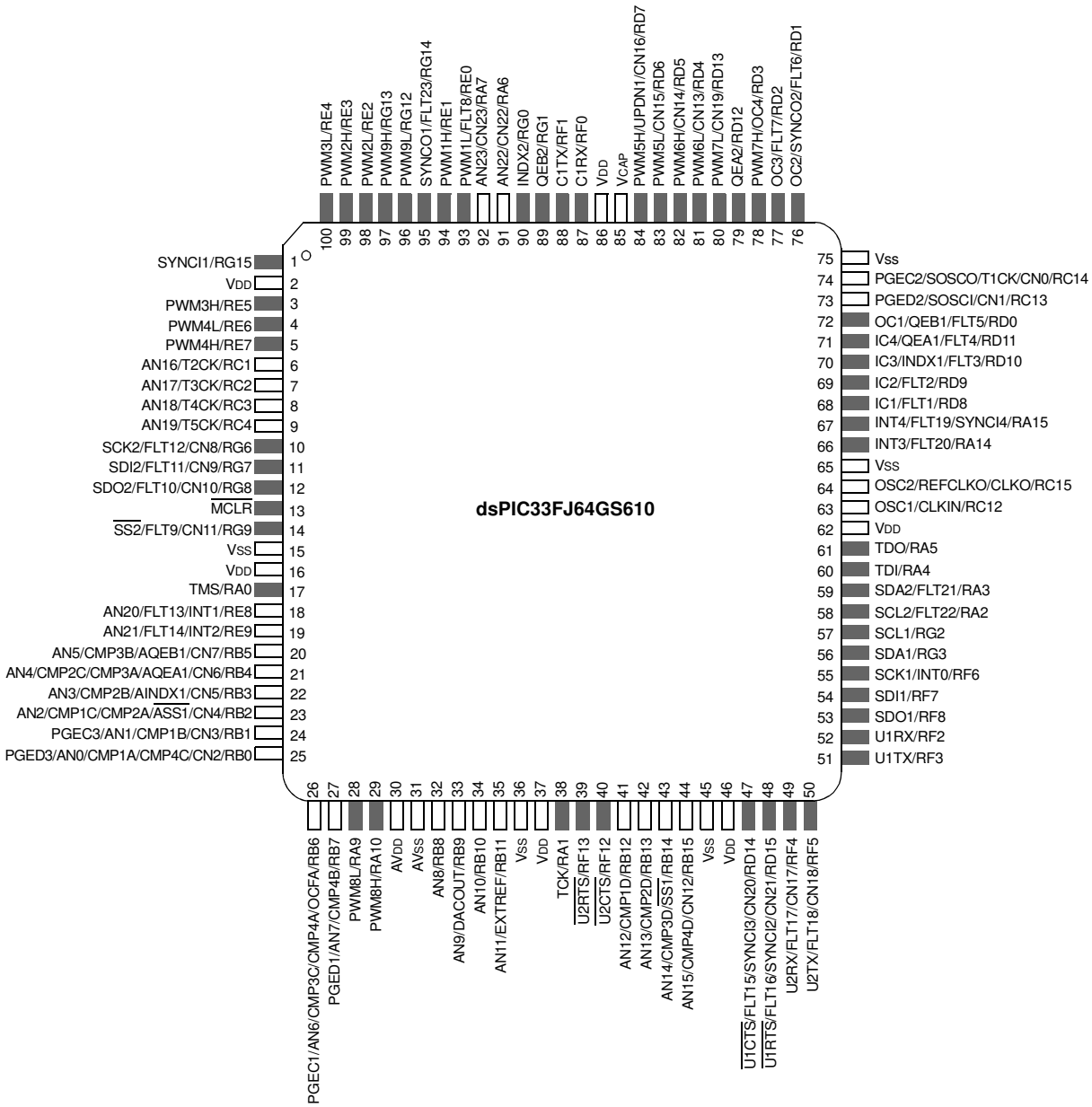
■ = Pins are up to 5V tolerant



Pin Diagrams (Continued)

100-Pin TQFP

■ = Pins are up to 5V tolerant



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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the primary reference for the operation of a particular module or device feature.

Note 1: To access the documents listed below, browse to the documentation section of the dsPIC33FJ64GS610 product page of the Microchip web site (www.microchip.com) to select a family reference manual section from the following list.

In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- **"CPU"** (DS70204)
- **"Data Memory"** (DS70202)
- **"Program Memory"** (DS70203)
- **"Flash Programming"** (DS70191)
- **"Reset"** (DS70192)
- **"Watchdog Timer (WDT) and Power-Saving Modes"** (DS70196)
- **"I/O Ports"** (DS70193)
- **"Timers"** (DS70205)
- **"Input Capture"** (DS70198)
- **"Output Compare"** (DS70005157)
- **"Quadrature Encoder Interface (QEI)"** (DS70208)
- **"Analog-to-Digital Converter (ADC)"** (DS70183)
- **"UART"** (DS70188)
- **"Serial Peripheral Interface (SPI)"** (DS70206)
- **"Inter-Integrated Circuit™ (I^2C™)"** (DS70000195)
- **"ECAN™"** (DS70185)
- **"Direct Memory Access (DMA)"** (DS70182)
- **"CodeGuard™ Security"** (DS70199)
- **"Programming and Diagnostics"** (DS70207)
- **"Device Configuration"** (DS70194)
- **"Development Tool Support"** (DS70200)
- **"Oscillator (Part IV)"** (DS70307)
- **"High-Speed PWM"** (DS70000323)
- **"High-Speed 10-Bit ADC"** (DS70000321)
- **"High-Speed Analog Comparator"** (DS70296)
- **"Interrupts (Part V)"** (DS70597)

NOTES:

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1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the latest sections in the *"dsPIC33/PIC24 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com). The information in this data sheet supersedes the information in the FRM.

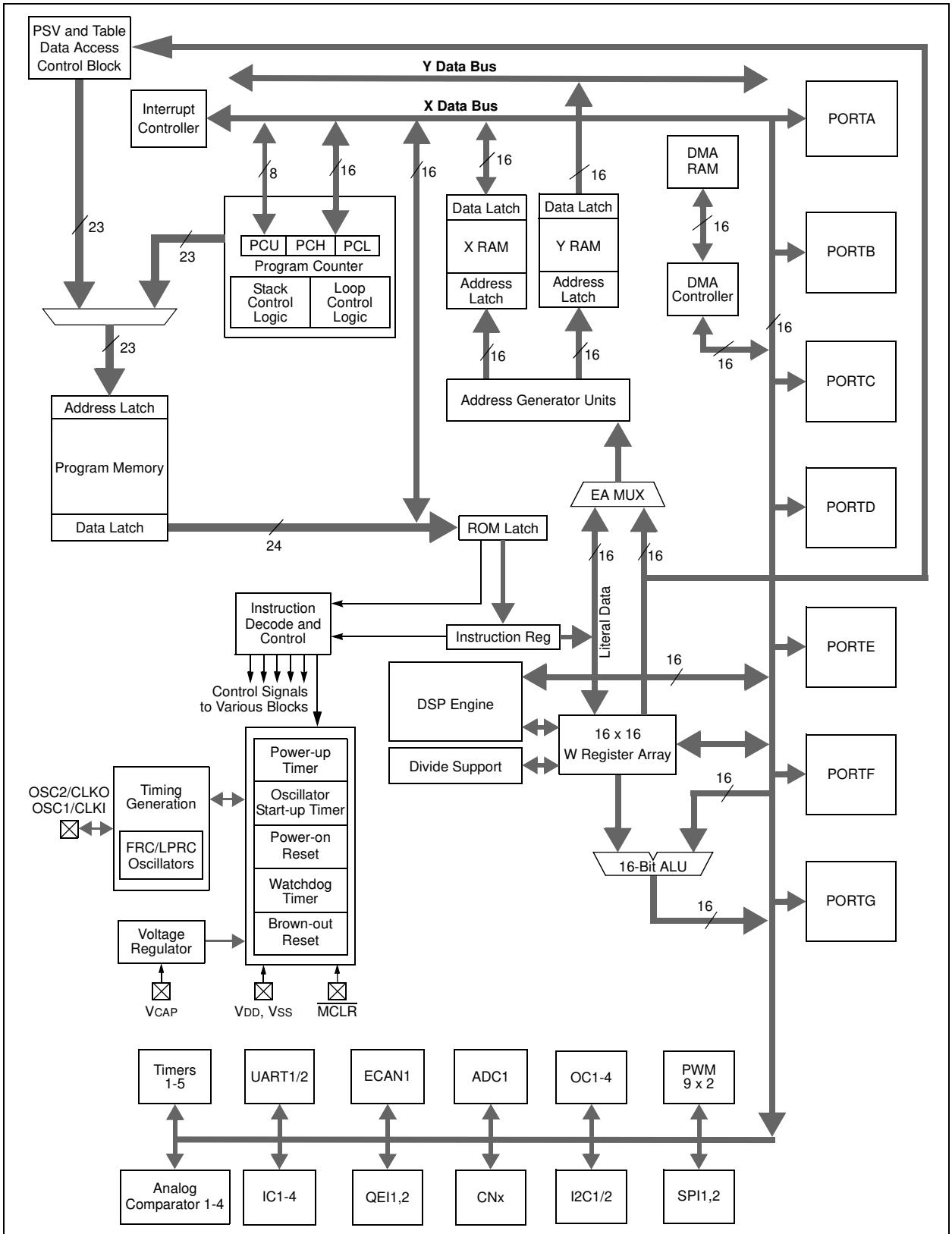
This document contains device-specific information for the following dsPIC33F Digital Signal Controller (DSC) devices:

- dsPIC33FJ32GS406
- dsPIC33FJ32GS606
- dsPIC33FJ32GS608
- dsPIC33FJ32GS610
- dsPIC33FJ64GS406
- dsPIC33FJ64GS606
- dsPIC33FJ64GS608
- dsPIC33FJ64GS610

The dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 families of devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance 16-bit microcontroller (MCU) architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules in the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 devices. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: DEVICE BLOCK DIAGRAM



Note: Not all pins or features are implemented on all device pinout configurations. See pinout diagrams for the specific pins and features present on each device.

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TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	Description
AN0-AN23	I	Analog	Analog input channels.
CLKI	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
SOSCI	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.
SOSCO	O	—	32.768 kHz low-power oscillator crystal output.
CN0-CN23	I	ST	Change Notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
C1RX	I	ST	ECAN1 bus receive pin.
C1TX	O	—	ECAN1 bus transmit pin.
IC1-IC4	I	ST	Capture Inputs 1 through 4.
INDX1, INDX2, AINDX1	I	ST	Quadrature Encoder Index Pulse input.
QEA1, QEA2, AQEA1	I	ST	Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode.
QEB1, QEB2, AQEB1	I	ST	Quadrature Encoder Phase A input in QEI mode. Auxiliary Timer External Clock/Gate input in Timer mode.
UPDN1	O	CMOS	Position Up/Down Counter Direction State.
OCFA	I	ST	Compare Fault A input.
OC1-OC4	O	—	Compare Outputs 1 through 4.
INT0	I	ST	External Interrupt 0.
INT1	I	ST	External Interrupt 1.
INT2	I	ST	External Interrupt 2.
INT3	I	ST	External Interrupt 3.
INT4	I	ST	External Interrupt 4.
RA0-RA15	I/O	ST	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.
RC0-RC15	I/O	ST	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE9	I/O	ST	PORTE is a bidirectional I/O port.
RF0-RF13	I/O	ST	PORTF is a bidirectional I/O port.
RG0-RG15	I/O	ST	PORTG is a bidirectional I/O port.
T1CK	I	ST	Timer1 external clock input.
T2CK	I	ST	Timer2 external clock input.
T3CK	I	ST	Timer3 external clock input.
T4CK	I	ST	Timer4 external clock input.
T5CK	I	ST	Timer5 external clock input.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; I = Input
ST = Schmitt Trigger input with CMOS levels; P = Power; O = Output
TTL = Transistor-Transistor Logic

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
U1CTS	I	ST	UART1 Clear-to-Send.
U1RTS	O	—	UART1 Request-to-Send.
U1RX	I	ST	UART1 receive.
U1TX	O	—	UART1 transmit.
U2CTS	I	ST	UART2 Clear-to-Send.
U2RTS	O	—	UART2 Request-to-Send.
U2RX	I	ST	UART2 receive.
U2TX	O	—	UART2 transmit.
SCK1	I/O	ST	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	SPI1 data in.
SDO1	O	—	SPI1 data out.
SS1, ASS1	I/O	ST	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	SPI2 data in.
SDO2	O	—	SPI2 data out.
SS2	I/O	ST	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	Synchronous serial data input/output for I2C1.
SCL2	I/O	ST	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	Synchronous serial data input/output for I2C2.
TMS	I	TTL	JTAG Test mode select pin.
TCK	I	TTL	JTAG test clock input pin.
TDI	I	TTL	JTAG test data input pin.
TDO	O	—	JTAG test data output pin.
CMP1A	I	Analog	Comparator 1 Channel A.
CMP1B	I	Analog	Comparator 1 Channel B.
CMP1C	I	Analog	Comparator 1 Channel C.
CMP1D	I	Analog	Comparator 1 Channel D.
CMP2A	I	Analog	Comparator 2 Channel A
CMP2B	I	Analog	Comparator 2 Channel B.
CMP2C	I	Analog	Comparator 2 Channel C.
CMP2D	I	Analog	Comparator 2 Channel D.
CMP3A	I	Analog	Comparator 3 Channel A.
CMP3B	I	Analog	Comparator 3 Channel B.
CMP3C	I	Analog	Comparator 3 Channel C.
CMP3D	I	Analog	Comparator 3 Channel D.
CMP4A	I	Analog	Comparator 4 Channel A.
CMP4B	I	Analog	Comparator 4 Channel B.
CMP4C	I	Analog	Comparator 4 Channel C.
CMP4D	I	Analog	Comparator 4 Channel D.
DACOUT	O	—	DAC output voltage.
EXTREF	I	Analog	External voltage reference input for the reference DACs.
REFCLK	O	—	REFCLK output signal is a postscaled derivative of the system clock.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; I = Input
ST = Schmitt Trigger input with CMOS levels; P = Power; O = Output
TTL = Transistor-Transistor Logic

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
FLT1-FLT23	I	ST	Fault inputs to PWM module.
SYNCI1-SYNCI4	I	ST	External synchronization signal to PWM master time base.
SYNCO1-SYNCO2	O	—	PWM master time base for external device synchronization.
PWM1L	O	—	PWM1 low output.
PWM1H	O	—	PWM1 high output.
PWM2L	O	—	PWM2 low output.
PWM2H	O	—	PWM2 high output.
PWM3L	O	—	PWM3 low output.
PWM3H	O	—	PWM3 high output.
PWM4L	O	—	PWM4 low output.
PWM4H	O	—	PWM4 high output.
PWM5L	O	—	PWM5 low output.
PWM5H	O	—	PWM5 high output.
PWM6L	O	—	PWM6 low output.
PWM6H	O	—	PWM6 high output.
PWM7L	O	—	PWM7 low output.
PWM7H	O	—	PWM7 high output.
PWM8L	O	—	PWM8 low output.
PWM8H	O	—	PWM8 high output.
PWM9L	O	—	PWM9 low output.
PWM9H	O	—	PWM9 high output.
PGED1	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2	I	ST	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3	I	ST	Clock input pin for Programming/Debugging Communication Channel 3.
$\overline{MCLR}$	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	P	P	Positive supply for analog modules.
AVSS	P	P	Ground reference for analog modules.
V_{DD}	P	—	Positive supply for peripheral logic and I/O pins.
V_{CAP}	P	—	CPU logic filter capacitor connection.
V_{SS}	P	—	Ground reference for logic and I/O pins.

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = Transistor-Transistor Logic
Analog = Analog input
P = Power
I = Input
O = Output

NOTES:

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2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*. Please see the Microchip web site (www.microchip.com) for the latest dsPIC33/PIC24 Family Reference Manual sections. The information in this data sheet supersedes the information in the FRM.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33FJ32GS406/606/608/610 and dsPIC33FJ64GS406/606/608/610 family of 16-bit Digital Signal Controllers (DSC) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used)
  (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP
  (see **Section 2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

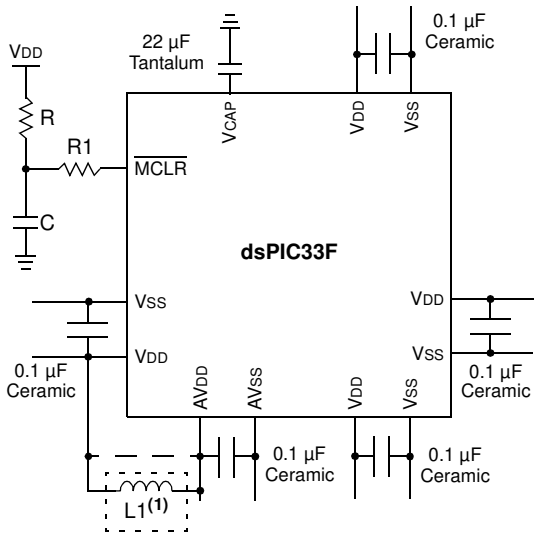
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2} \quad \text{(i.e., ADC conversion rate/2)}$$

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 Capacitor on Internal Voltage Regulator (VCAP)

A low-ESR (< 0.5 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a minimum capacitor of 22 µF, 16V connected to ground. The type can be ceramic or tantalum. Refer to **Section 27.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP. It is recommended that the trace length not exceed one-quarter inch (6 mm). Refer to **Section 24.2 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

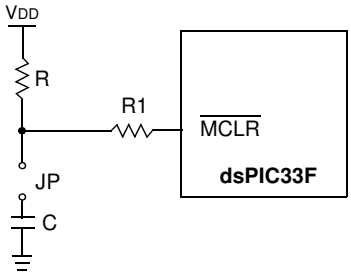
- Device Reset
- Device programming and debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor C, be isolated from the MCLR pin during programming and debugging operations.

Place the components shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS(1,2)



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

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2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™.

For more information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) (DS51765)
- *"MPLAB® ICD 3 Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Debugger User's Guide" (*DS51616)
- *"Using MPLAB® REAL ICE™"* (poster) (DS51749)

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 9.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT