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DTC114TKA

NPN Digital Transistor

Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit)
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects
- Only the on/off conditions need to be set for operation, making device design easy

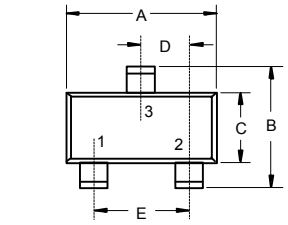
Absolute Maximum Ratings

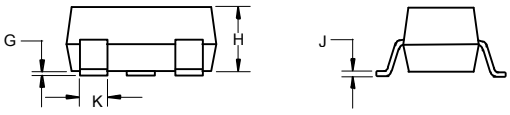
Parameter	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Emitter-Base voltage	V_{EBO}	5	V
Collector Current-Continuous	I_C	100	mA
Collector Dissipation	P_C	200	mW
Junction Temperature	T_J	150	℃
Storage Temperature Range	T_{STG}	-55~150	℃

Electrical Characteristics

Sym	Parameter	Min	Typ	Max	Unit
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage (I_C=50uA, I_E=0)	50	---	---	V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage (I_C=1mA, I_B=0)	50	---	---	V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage (I_E=50uA, I_C=0)	5	---	---	V
I_{CBO}	Collector Cut-off Current (V_{CB}=50V, I_E=0)	---	---	0.5	uA
I_{EBO}	Emitter Cut-off Current (V_{EB}=4V, I_C=0)	---	---	0.5	uA
h_{FE}	DC Current Gain (V_{CE}=5V, I_C=1mA)	100	300	600	---
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage (I_C=10mA, I_B=1mA)	---	---	0.3	V
R_1	Input Resistor	7	10	13	KΩ
f_T	Transition Frequency (V_{CE}=10V, I_C=-5mA, f=100MHz)	---	250	---	MHz

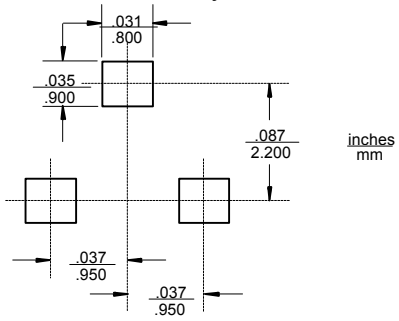
SOT-23-3L





DIMENSIONS					
	INCHES		MM		
DIM	MIN	MAX	MIN	MAX	NOTE
A	.113	.117	2.87	2.97	
B	.108	.112	2.75	2.85	
C	.061	.065	1.55	1.65	
D	.036	.038	.925	.975	
E	.073	.077	1.85	1.95	
G	.0016	.0039	.04	.100	
H	.044	.049	1.12	1.25	
J	.006	.007	.14	.17	
K	.013	.015	.34	.37	

Suggested Solder Pad Layout



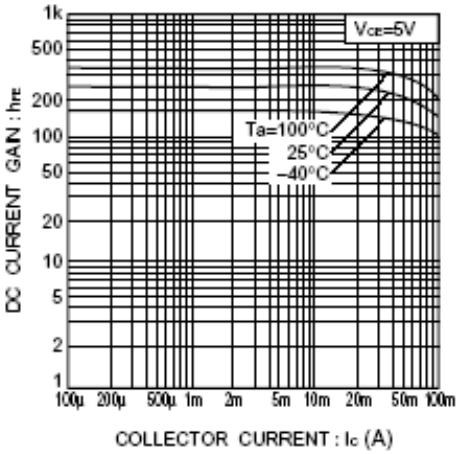


Fig.1 DC current gain vs. collector current

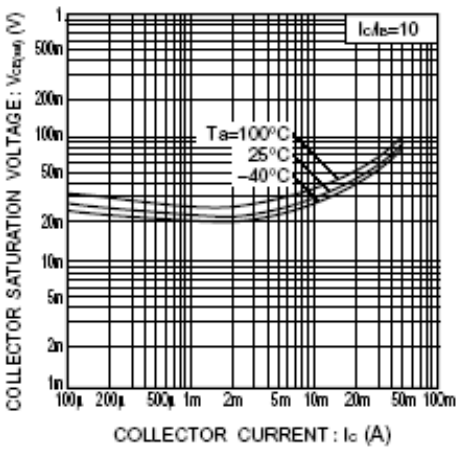


Fig.2 Collector-emitter saturation voltage vs. collector current

●Equivalent circuit