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C8051F300/1/2/3/4/5

Mixed Signal ISP Flash MCU Family

Analog Peripherals
- **8-Bit ADC ('F300/2 only)**
  - Up to 500 ksps
  - Up to 8 external inputs
  - Programmable amplifier gains of 4, 2, 1, & 0.5
  - VREF from external pin or V_{DD}
  - Built-in temperature sensor
  - External conversion start input
- **Comparator**
  - Programmable hysteresis and response time
  - Configurable as interrupt or reset source
  - Low current (<0.5 µA)

On-chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Complete development kit

Supply Voltage 2.7 to 3.6 V
- Typical operating current: 6.6 mA @ 25 MHz; 14 µA @ 32 kHz
- Typical stop mode current: 0.1 µA
- Temperature range: –40 to +85 °C

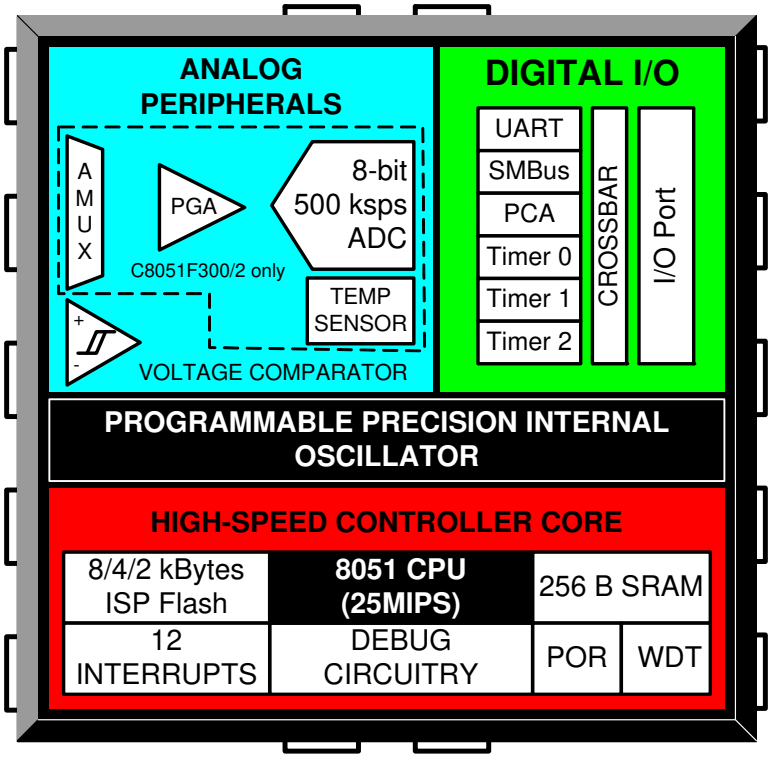
High Speed 8051 µc Core
- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Expanded interrupt handler

Memory
- 256 bytes internal data RAM
- Up to 8 kB ('F300/1/2/3), 4 kB ('F304), or 2 kB ('F305) Flash; 512 bytes are reserved in the 8 kB devices

Digital Peripherals
- 8 Port I/O; All 5 V tolerant with high sink current
- Hardware enhanced UART and SMBus™ serial ports
- Three general-purpose 16-bit counter/timers
- 16-bit programmable counter array (PCA) with three capture/compare modules
- Real time clock mode using PCA or timer and external clock source

Clock Sources
- Internal oscillator: 24.5 MHz with ±2% accuracy supports UART operation
- External oscillator: Crystal, RC, C, or clock (1 or 2 pin modes)
- Can switch between clock sources on-the-fly; Useful in power saving modes

11-Pin QFN or 14-Pin SOIC Package
- QFN Size = 3x3 mm



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1. System Overview

C8051F300/1/2/3/4/5 devices are fully integrated mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 1.1 on page 14 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 8-bit 500 ksps 11-channel ADC with programmable gain pre-amplifier and analog multiplexer (C8051F300/2 only)
- Precision programmable 25 MHz internal oscillator
- Up to 8 kB of on-chip Flash memory
- 256 bytes of on-chip RAM
- SMBus/I^2C and Enhanced UART serial interfaces implemented in hardware
- Three general-purpose 16-bit timers
- Programmable counter/timer array (PCA) with three capture/compare modules and watchdog timer function
- On-chip power-on reset, V_{DD} monitor, and temperature sensor
- On-chip voltage comparator
- Byte-wide I/O port (5 V tolerant)

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F300/1/2/3/4/5 devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Laboratories 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 2.7 to 3.6 V operation over the industrial temperature range (–45 to +85 °C). The Port I/O and $\overline{RST}$ pins are tolerant of input signals up to 5 V. The C8051F300/1/2/3/4/5 are available in 3 x 3 mm 11-pin QFN or 14-pin SOIC packaging.

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory	RAM	Calibrated Internal Oscillator	SMBus/I^2C	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	8-bit 500ksps ADC	Temperature Sensor	Analog Comparators	Lead-free (RoHS compliant)	Package
C8051F300-GM	25	8 k	256	✓	✓	✓	3	✓	8	✓	✓	1	✓	QFN-11
C8051F300-GS	25	8 k	256	✓	✓	✓	3	✓	8	✓	✓	1	✓	SOIC-14
C8051F301-GM	25	8 k	256	✓	✓	✓	3	✓	8	—	—	1	✓	QFN-11
C8051F301-GS	25	8 k	256	✓	✓	✓	3	✓	8	—	—	1	✓	SOIC-14
C8051F302-GM	25	8 k	256	—	✓	✓	3	✓	8	✓	✓	1	✓	QFN-11
C8051F302-GS	25	8 k	256	—	✓	✓	3	✓	8	✓	✓	1	✓	SOIC-14
C8051F303-GM	25	8 k	256	—	✓	✓	3	✓	8	—	—	1	✓	QFN-11
C8051F303-GS	25	8 k	256	—	✓	✓	3	✓	8	—	—	1	✓	SOIC-14
C8051F304-GM	25	4 k	256	—	✓	✓	3	✓	8	—	—	1	✓	QFN-11
C8051F304-GS	25	4 k	256	—	✓	✓	3	✓	8	—	—	1	✓	SOIC-14
C8051F305-GM	25	2 k	256	—	✓	✓	3	✓	8	—	—	1	✓	QFN-11
C8051F305-GS	25	2 k	256	—	✓	✓	3	✓	8	—	—	1	✓	SOIC-14

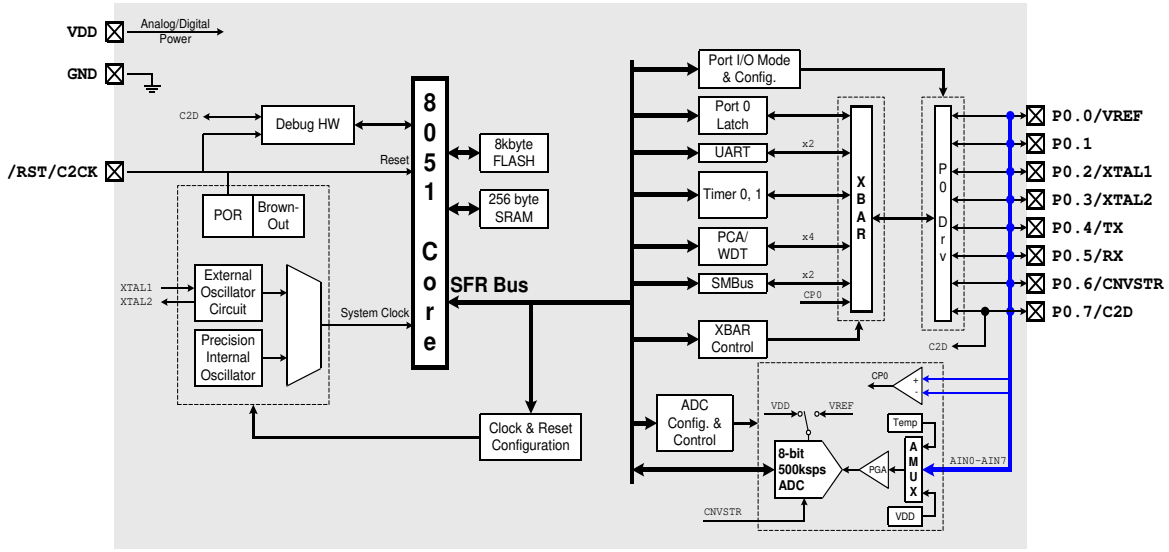

Figure 1.1. C8051F300/2 Block Diagram

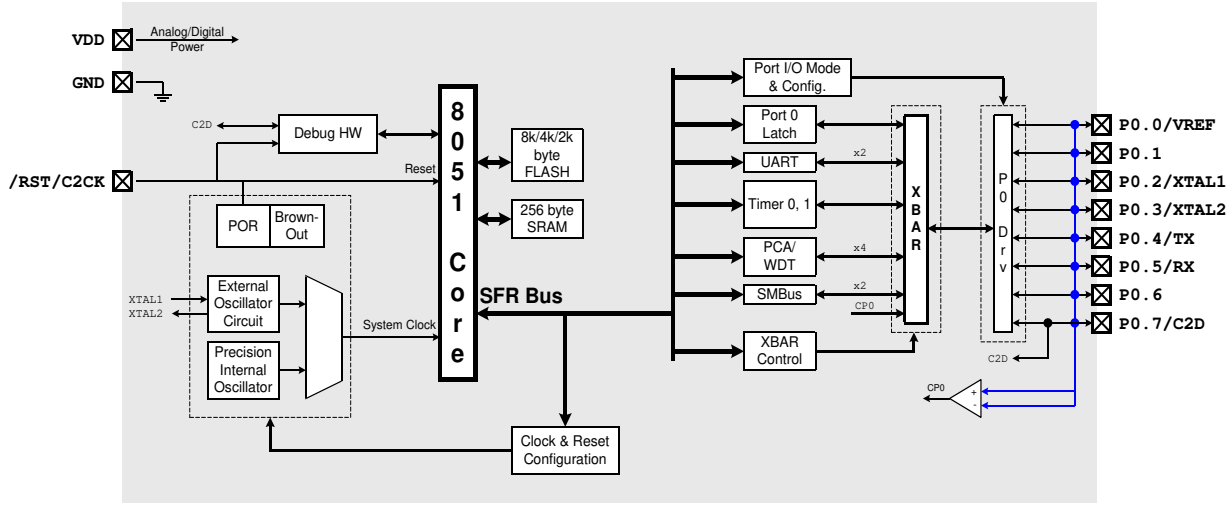

Figure 1.2. C8051F301/3/4/5 Block Diagram

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F300/1/2/3/4/5 family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052, including two standard 16-bit counter/timers, one enhanced 16-bit counter/timer with external oscillator input, a full-duplex UART with extended baud rate configuration, 256 bytes of internal RAM, 128 byte Special Function Register (SFR) address space, and a byte-wide I/O Port.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12 to 24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.3 shows a comparison of peak throughputs for various 8-bit microcontroller cores with their maximum system clocks.

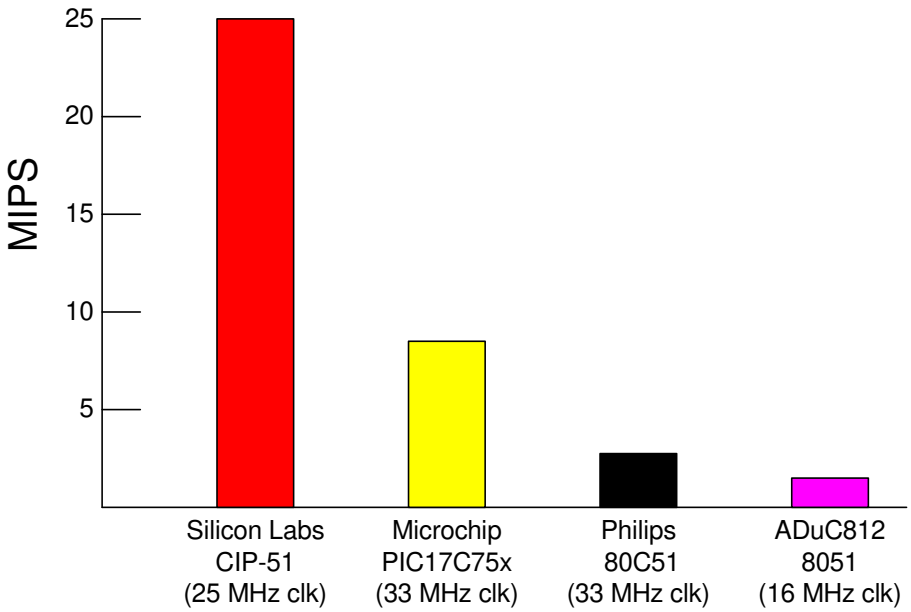

Figure 1.3. Comparison of Peak MCU Execution Speeds

1.1.3. Additional Features

The C8051F300/1/2/3/4/5 SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides 12 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multitasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor (forces reset when power supply voltage drops below 2.7 V), a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal Flash read/write protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash protection may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator is available as a factory calibrated 24.5 MHz ±2% (C8051F300/1 devices); an uncalibrated version is available on C8051F302/3/4/5 devices. On all C8051F300/1/2/3/4/5 devices, the internal oscillator period may be user programmed in ~0.5% increments. An external oscillator drive circuit is also included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly to the external oscillator circuit. An external oscillator can be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) external crystal source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed.

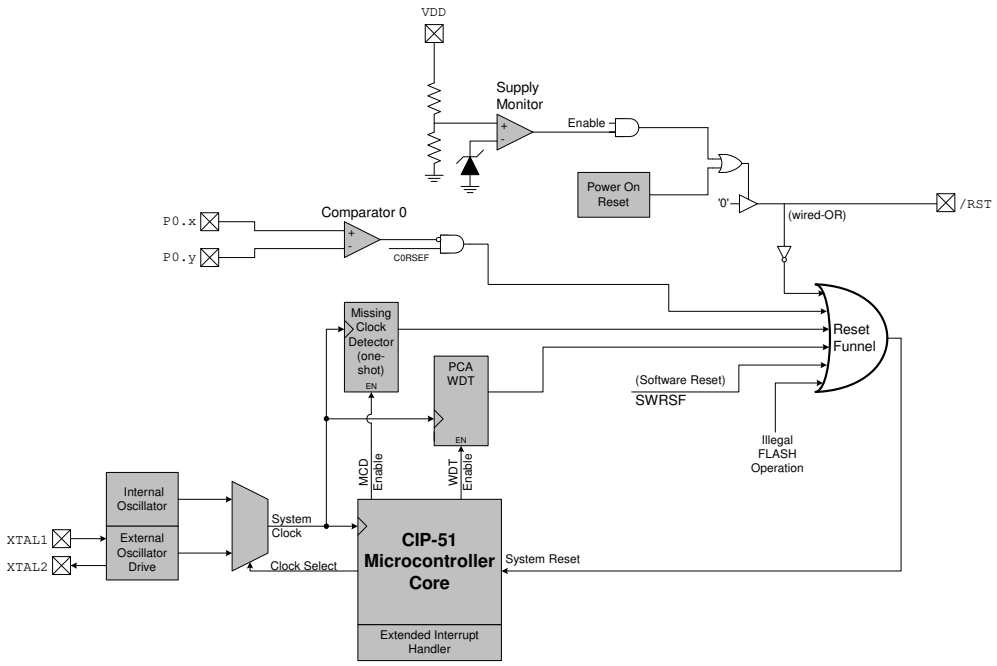

Figure 1.4. On-Chip Clock and Reset

1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

The C8051F300/1/2/3 includes 8k bytes of Flash program memory (the C8051F304 includes 4k bytes; the C8051F305 includes 2k bytes). This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. See Figure 1.5 for the C8051F300/1/2/3 system memory map.

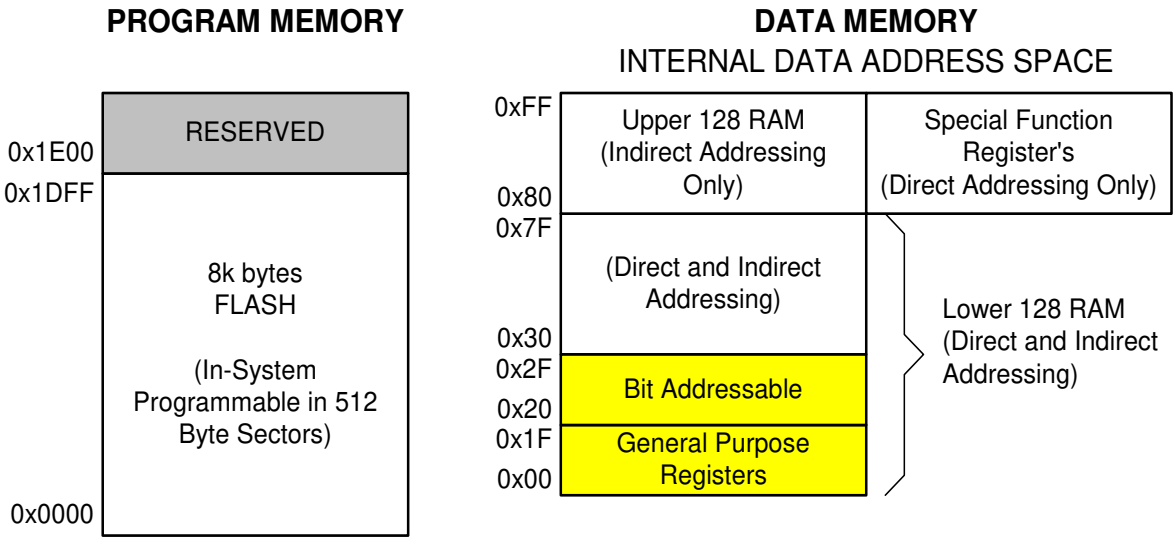

Figure 1.5. On-chip Memory Map (C8051F300/1/2/3 Shown)

1.3. On-Chip Debug Circuitry

The C8051F300/1/2/3/4/5 devices include on-chip Silicon Labs 2-Wire (C2) debug circuitry that provides non-intrusive, full-speed, in-circuit debugging of the production part *installed in the end application.*

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC and SMBus) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F300DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F300/1/2/3/4/5 MCUs. The kit includes software with a developer's studio and debugger, an integrated 8051 assembler, and a C2 debug adapter. It also has a target application board with the associated MCU installed and large prototyping area, plus the necessary communication cables and wall-mount power supply. The Development Kit requires a computer with Windows® 98 SE or later. The Silicon Labs IDE interface is a vastly superior developing and debugging configuration, compared to standard MCU emulators that use onboard "ICE Chips" and require the MCU in the application board to be socketed. Silicon Labs' debug paradigm increases ease of use and preserves the performance of the precision analog peripherals.

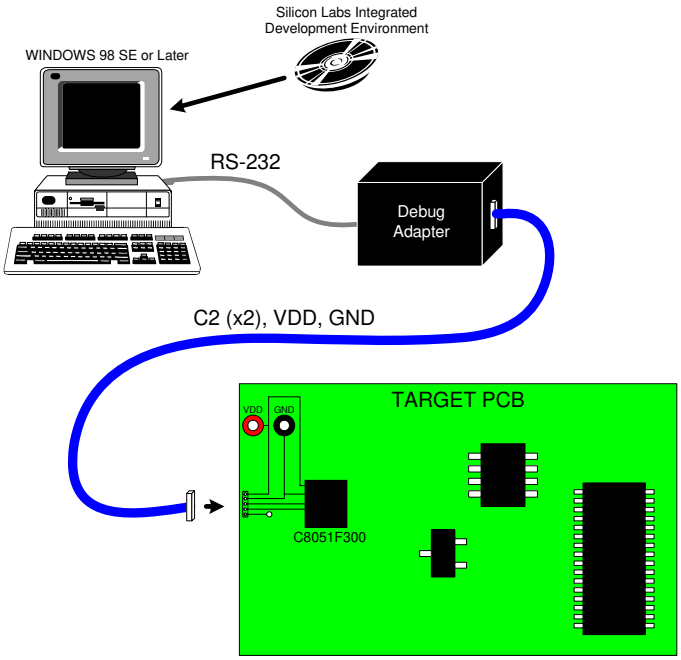

Figure 1.6. Development/In-System Debug Diagram

1.4. Programmable Digital I/O and Crossbar

C8051F300/1/2/3/4/5 devices include a byte-wide I/O Port that behaves like a typical 8051 Port with a few enhancements. Each Port pin may be configured as an analog input or a digital I/O pin. Pins selected as digital I/Os may additionally be configured for push-pull or open-drain output. The “weak pull-ups” that are fixed on typical 8051 devices may be globally disabled, providing power savings capabilities.

Perhaps the most unique Port I/O enhancement is the Digital Crossbar. This is essentially a digital switching network that allows mapping of internal digital system resources to Port I/O pins (See Figure 1.7). On-chip counter/timers, serial buses, HW interrupts, comparator output, and other digital signals in the controller can be configured to appear on the Port I/O pins specified in the Crossbar Control registers. This allows the user to select the exact mix of general purpose Port I/O and digital resources needed for the particular application.

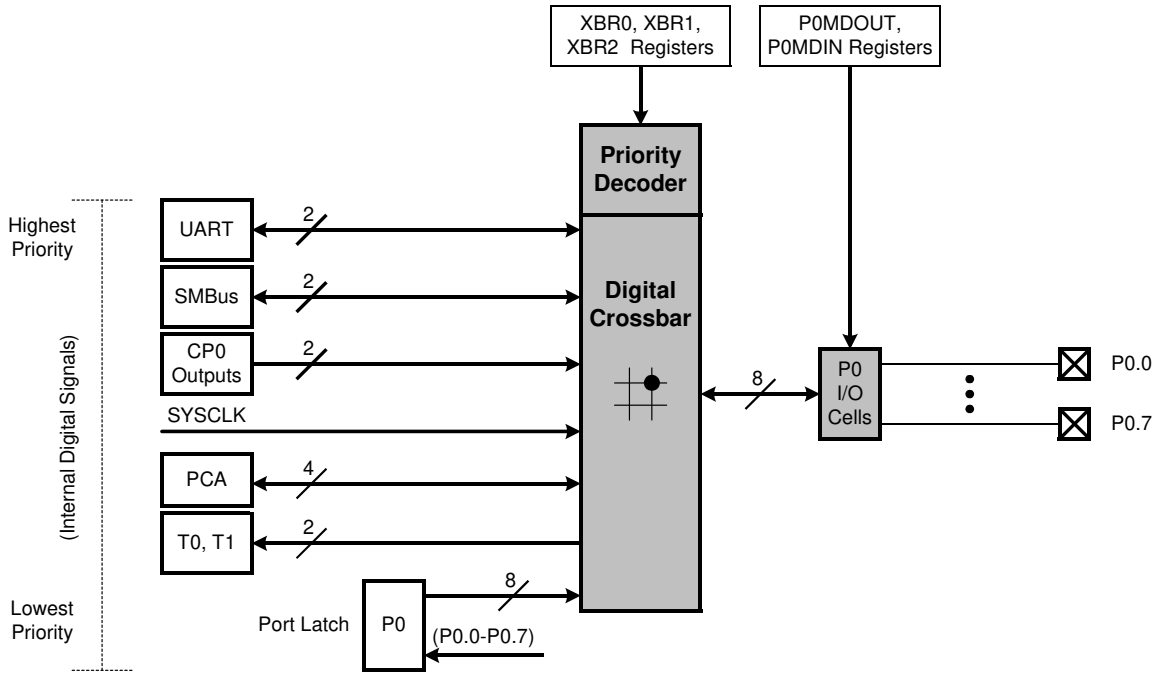

Figure 1.7. Digital Crossbar Diagram

1.5. Serial Ports

The C8051F300/1/2/3/4/5 Family includes an SMBus/I^2C interface and a full-duplex UART with enhanced baud rate configuration. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

1.6. Programmable Counter Array

An on-chip Programmable Counter/Timer Array (PCA) is included in addition to the three 16-bit general purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer time base with three programmable capture/compare modules. The PCA clock is derived from one of six sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflows, an External Clock Input (ECI), the system clock, or the external oscillator clock source divided by 8. The external clock source selection is useful for real-time clock functionality, where the PCA is clocked by an external source while the internal oscillator drives the system clock.

Each capture/compare module can be configured to operate in one of six modes: Edge-Triggered Capture, Software Timer, High Speed Output, 8- or 16-bit Pulse Width Modulator, or Frequency Output. Additionally, Capture/Compare Module 2 offers watchdog timer (WDT) capabilities. Following a system reset, Module 2 is configured and enabled in WDT mode. The PCA Capture/Compare Module I/O and External Clock Input may be routed to Port I/O via the Digital Crossbar.

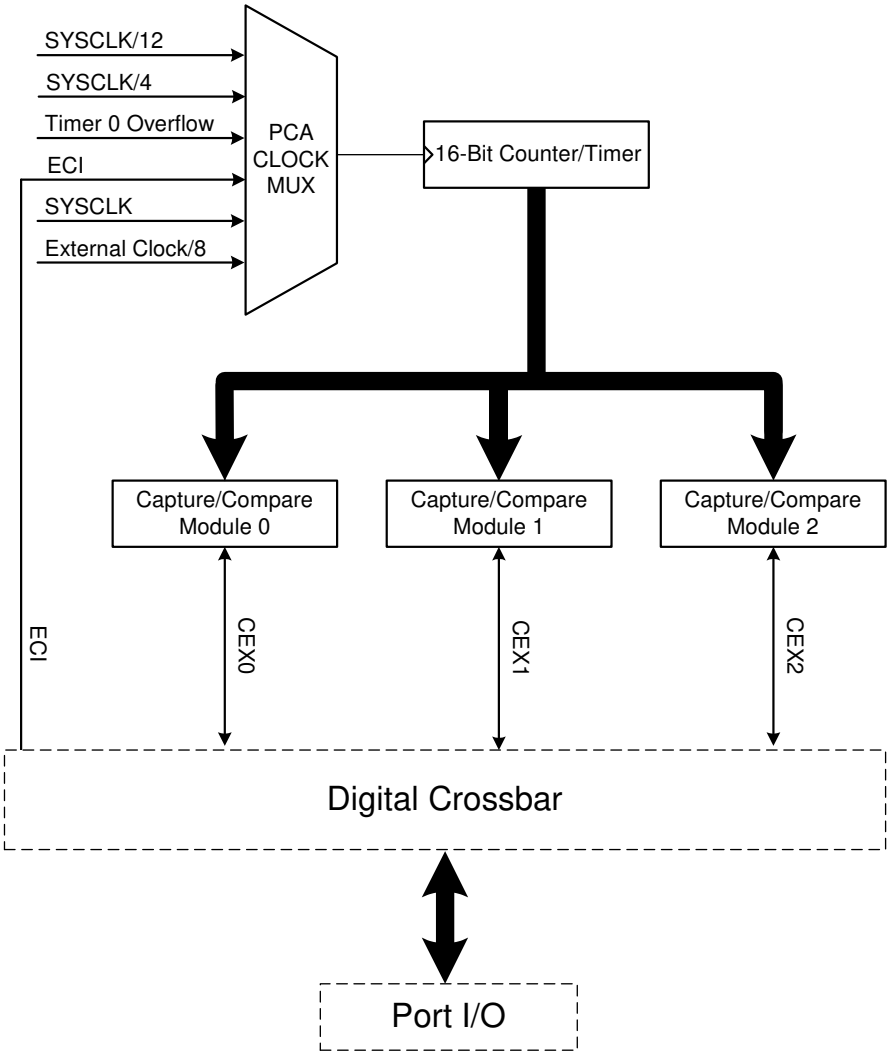

Figure 1.9. PCA Block Diagram

1.7. 8-Bit Analog to Digital Converter (C8051F300/2 Only)

The C8051F300/2 includes an on-chip 8-bit SAR ADC with a 10-channel differential input multiplexer and programmable gain amplifier. With a maximum throughput of 500 ksps, the ADC offers true 8-bit accuracy with an INL of ±1LSB. The ADC system includes a configurable analog multiplexer that selects both positive and negative ADC inputs. Each Port pin is available as an ADC input; additionally, the on-chip Temperature Sensor output and the power supply voltage (V_{DD}) are available as ADC inputs. User firmware may shut down the ADC to save power.

The integrated programmable gain amplifier (PGA) amplifies the ADC input by 0.5, 1, 2, or 4 as defined by user software. The gain stage is especially useful when different ADC input channels have widely varied input voltage signals, or when it is necessary to "zoom in" on a signal with a large DC offset.

Conversions can be started in five ways: a software command, an overflow of Timer 0, 1, or 2, or an external convert start signal. This flexibility allows the start of conversion to be triggered by software events, a periodic signal (timer overflows), or external HW signals. Conversion completions are indicated by a status bit and an interrupt (if enabled). The resulting 8-bit data word is latched into an SFR upon completion of a conversion.

Window compare registers for the ADC data can be configured to interrupt the controller when ADC data is either within or outside of a specified range. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within/outside the specified range.

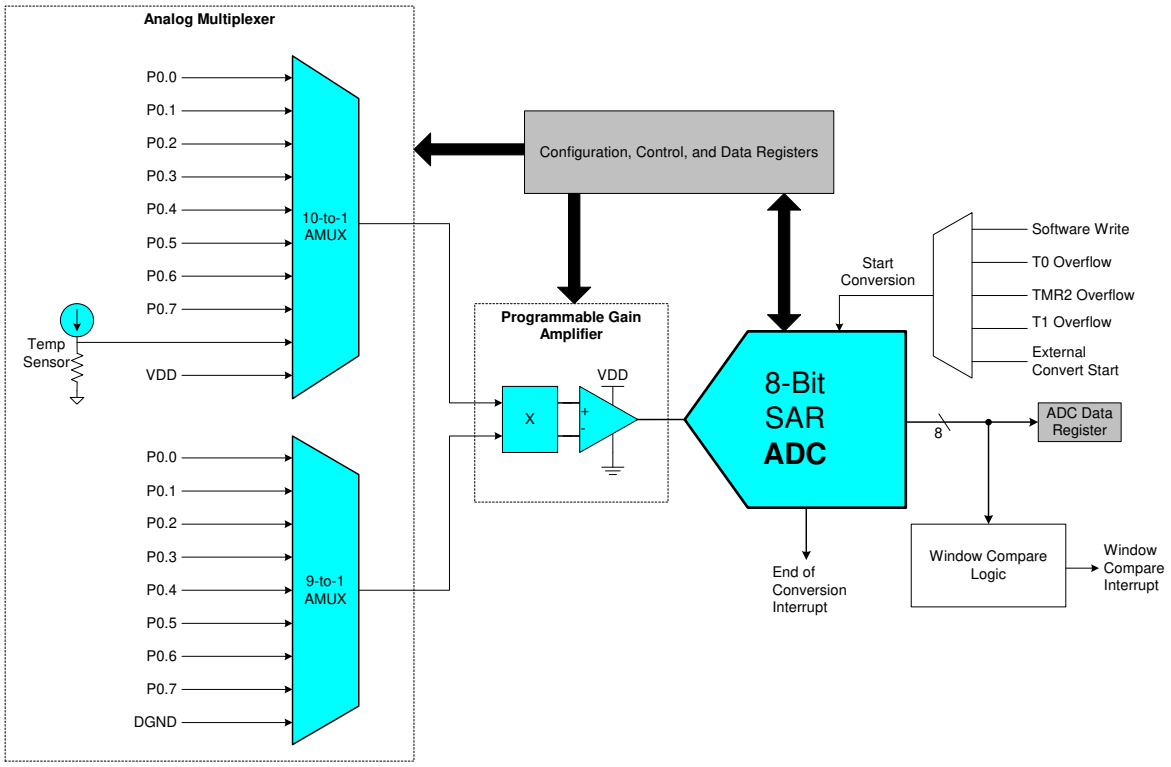

Figure 1.10. 8-Bit ADC Block Diagram

1.8. Comparator

C8051F300/1/2/3/4/5 devices include an on-chip voltage comparator that is enabled/disabled and configured via user software. All Port I/O pins may be configurated as comparator inputs. Two comparator outputs may be routed to a Port pin if desired: a latched output and/or an unlatched (asynchronous) output. Comparator response time is programmable, allowing the user to select between high-speed and low-power modes. Positive and negative hysteresis is also configurable.

Comparator interrupts may be generated on rising, falling, or both edges. When in IDLE mode, these interrupts may be used as a “wake-up” source. The comparator may also be configured as a reset source.

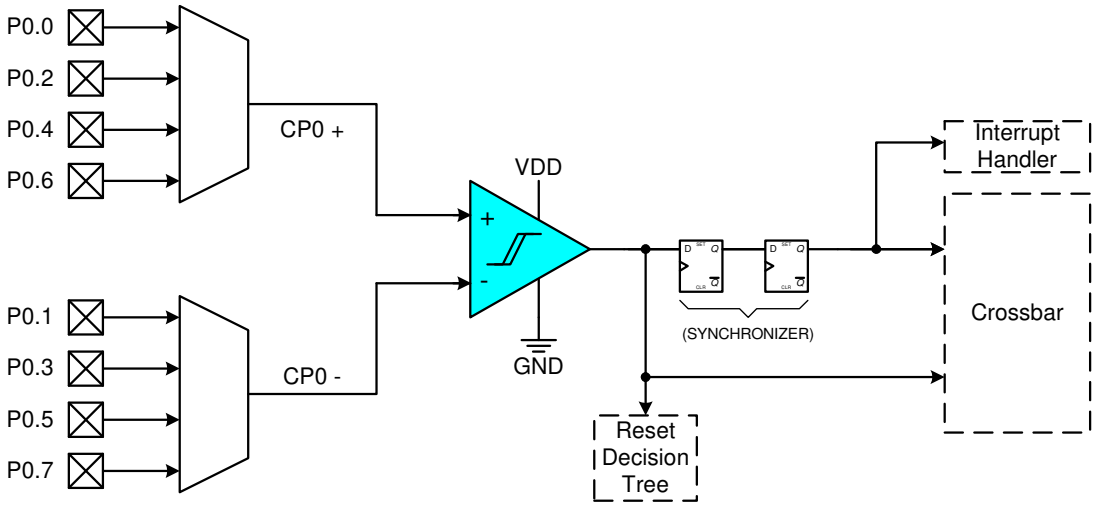

Figure 1.11. Comparator Block Diagram

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings*

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any Port I/O Pin or $\overline{\text{RST}}$ with respect to GND		–0.3	—	5.8	V
Voltage on V_{DD} with respect to GND		–0.3	—	4.2	V
Maximum Total current through V_{DD} and GND		—	—	500	mA
Maximum output current sunk by $\overline{\text{RST}}$ or any Port pin		—	—	100	mA

***Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. Global Electrical Characteristics

Table 3.1. Global Electrical Characteristics

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Voltage		V_{RST}[1]	3.0	3.6	V
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
SYSCLK (System Clock) (Note 2)		0	—	25	MHz
T_{SYSH} (SYSCLK High Time)		18	—	—	ns
T_{SYSL} (SYSCLK Low Time)		18	—	—	ns
Specified Operating Temperature Range		–40	—	+85	°C
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash)					
I_{DD} (Note 3)	V_{DD} = 3.6 V, F = 25 MHz	—	9.4	10.2	mA
	V_{DD} = 3.0 V, F = 25 MHz	—	6.6	7.2	mA
	V_{DD} = 3.0 V, F = 1 MHz	—	0.45	—	mA
	V_{DD} = 3.0 V, F = 80 kHz	—	36	—	µA
I_{DD} Supply Sensitivity (Note 3)	F = 25 MHz	—	69	—	%/V
	F = 1 MHz	—	51	—	%/V
I_{DD} Frequency Sensitivity (Note 3, Note 4)	V_{DD} = 3.0 V, F <= 15 MHz, T = 25 °C	—	0.45	—	mA/MHz
	V_{DD} = 3.0 V, F > 15 MHz, T = 25 °C	—	0.16	—	mA/MHz
	V_{DD} = 3.6 V, F <= 15 MHz, T = 25 °C	—	0.69	—	mA/MHz
	V_{DD} = 3.6 V, F > 15 MHz, T = 25 °C	—	0.20	—	mA/MHz
Digital Supply Current—CPU Inactive (Idle Mode, not fetching instructions from Flash)					
I_{DD} (Note 3)	V_{DD} = 3.6 V, F = 25 MHz	—	3.3	4.0	mA
	V_{DD} = 3.0 V, F = 25 MHz	—	2.5	3.2	mA
	V_{DD} = 3.0 V, F = 1 MHz	—	0.10	—	mA
	V_{DD} = 3.0 V, F = 80 kHz	—	8	—	µA