Chipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Product Overview

The DW1000 is a fully integrated single chip Ultra Wideband (UWB) low-power low-cost transceiver IC compliant to IEEE802.15.4-2011. It can be used in 2-way ranging or TDOA location systems to locate assets to a precision of 10 cm. It also supports data transfer at rates up to 6.8 Mbps

Key Features

- IEEE802.15.4-2011 UWB compliant
- Supports 6 RF bands from 3.5 GHz to 6.5 GHz
- Programmable transmitter output power
- Fully coherent receiver for maximum range and accuracy
- Complies with FCC & ETSI UWB spectral masks
- Supply voltage 2.8 V to 3.6 V
- Low power consumption
- SLEEP mode current 1 µA
- DEEP SLEEP mode current 50 nA
- Data rates of 110 kbps, 850 kbps, 6.8 Mbps
- Maximum packet length of 1023 bytes for high data throughput applications
- Integrated MAC support features
- Supports 2-way ranging and TDOA
- SPI interface to host processor
- 6 mm x 6 mm 48-pin QFN package with 0.4 mm lead pitch
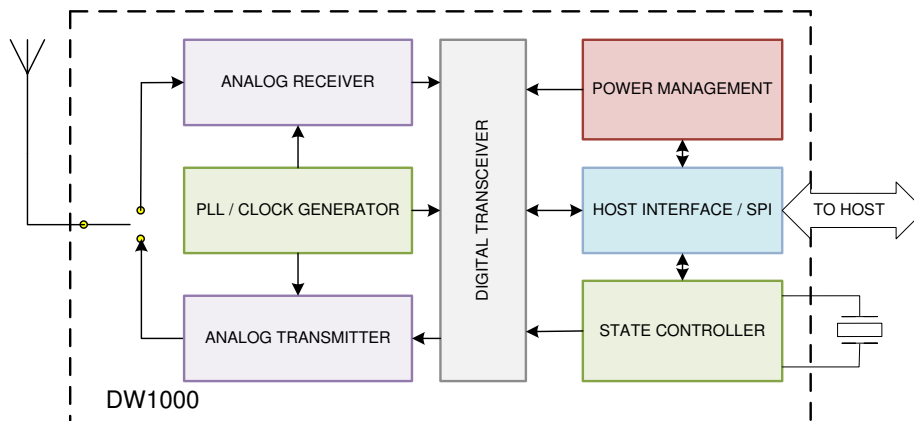- Small number of external components

Key Benefits

- Supports precision location and data transfer concurrently
- Asset location to a precision of 10 cm
- Extended communications range up to 290 m @ 110 kbps 10% PER minimises required infrastructure in RTLS
- High multipath fading immunity
- Supports high tag densities in RTLS
- Small PCB footprint allows cost-effective hardware implementations
- Long battery life minimises system lifetime cost

Applications

- Precision real time location systems (RTLS) using two-way ranging or TDOA schemes in a variety of markets: -
  o Healthcare
  o Consumer
  o Industrial
  o Other
- Location aware wireless sensor networks

DW1000 *IEEE802.15.4-2011 UWB Transceiver*

High Level Block Diagram

Table of Contents

List of Figures

List of Tables

DOCUMENT INFORMATION

Disclaimer

Decawave reserves the right to change product specifications without notice. As far as possible changes to functionality and specifications will be issued in product specific errata sheets or in new versions of this document. Customers are advised to check with Decawave for the most recent updates on this product.

LIFE SUPPORT POLICY

Decawave products are not authorized for use in safety-critical applications (such as life support) where a failure of the Decawave product would reasonably be expected to cause severe personal injury or death. Decawave customers using or selling Decawave products in such a manner do so entirely at their own risk and agree to fully indemnify Decawave and its representatives against any damages arising out of the use of Decawave products in such safety-critical applications.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

REGULATORY APPROVALS

The DW1000, as supplied from Decawave, has not been certified for use in any particular geographic region by the appropriate regulatory body governing radio emissions in that region although it is capable of such certification depending on the region and the manner in which it is used.

All products developed by the user incorporating the DW1000 must be approved by the relevant authority governing radio emissions in any given jurisdiction prior to the marketing or sale of such products in that jurisdiction and user bears all responsibility for obtaining such approval as needed from the appropriate authorities.

1 IC DESCRIPTION
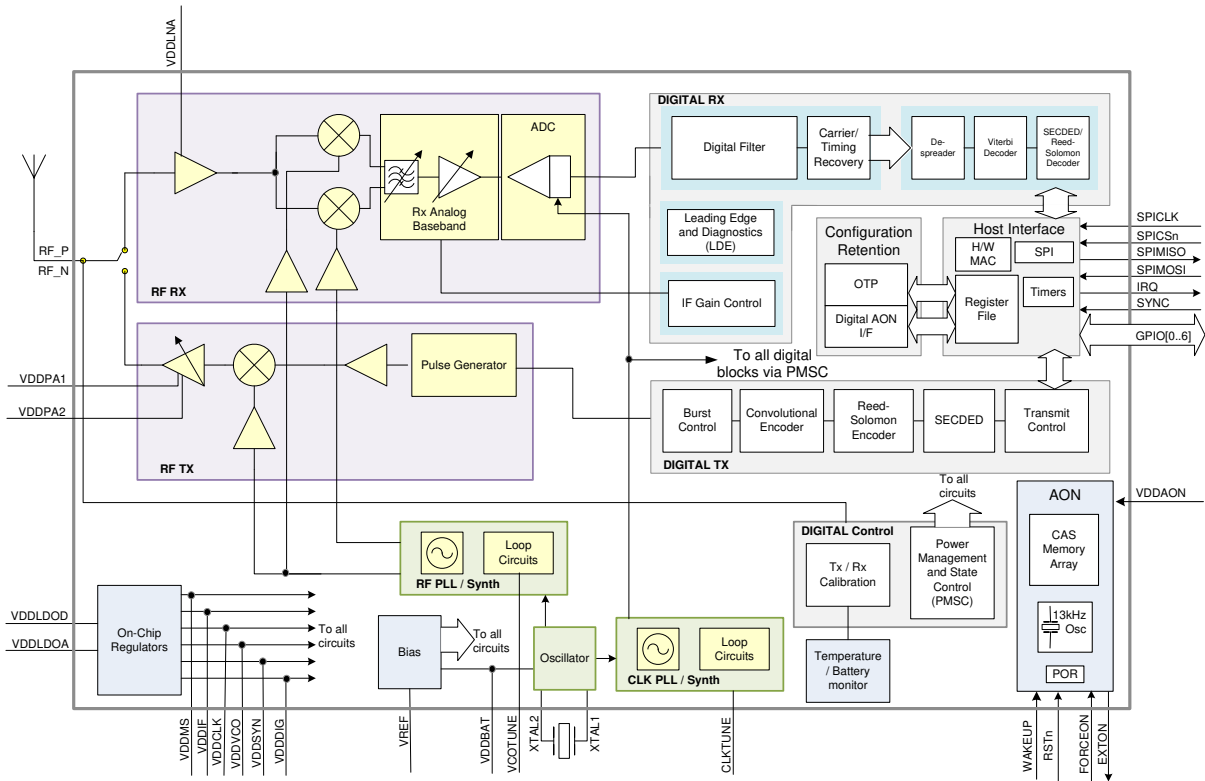
Figure 1: IC Block Diagram

DW1000 is a fully integrated low-power, single chip CMOS RF transceiver IC compliant with the IEEE802.15.4-2011 [1] UWB standard.

DW1000 consists of an analog front end containing a receiver and a transmitter and a digital back end that interfaces to an off-chip host processor. A TX/RX switch is used to connect the receiver or transmitter to the antenna port. Temperature and voltage monitors are provided on-chip

The receiver consists of an RF front end which amplifies the received signal in a low-noise amplifier before down-converting it directly to baseband. The receiver is optimized for wide bandwidth, linearity and noise figure. This allows each of the supported IEEE802.15.4-2011 [1] UWB channels to be down converted with minimum additional noise and distortion. The baseband signal is demodulated and the resulting received data is made available to the host controller via SPI.

The transmit pulse train is generated by applying digitally encoded transmit data to the analog pulse generator. The pulse train is up-converted by a double balanced mixer to a carrier generated by the synthesizer and centered on one of the permitted IEEE802.15.4-2011 [1] UWB channels. The modulated RF waveform is amplified before transmission from the external antenna.

The IC has an on-chip One-Time Programmable (OTP) memory. This memory can be used to store calibration data such as TX power level, crystal initial frequency error adjustment, and range accuracy adjustment. These adjustment values can be automatically retrieved when needed. See section 5.14 for more details.

The Always-On (AON) memory can be used to retain DW1000 configuration data during the lowest power operational states when the on-chip voltage regulators are disabled. This data is uploaded and downloaded automatically. Use of DW1000 AON memory is configurable.

The DW1000 clocking scheme is based around 3 main circuits; Crystal Oscillator, Clock PLL and RF PLL. The on-chip oscillator is designed to operate at a frequency of 38.4 MHz using an external crystal. An external 38.4 MHz clock signal may be applied in place of the crystal if an appropriately stable clock is available elsewhere in the user's system. This 38.4 MHz clock is used as the reference clock input to the two on-chip PLLs. The clock PLL (denoted CLKPLL) generates the clock required by the digital back end for signal processing. The RF PLL generates the down-conversion local oscillator (LO) for the receive chain and the up-conversion LO for the transmit chain. An internal 13 kHz oscillator is provided for use in the SLEEP state.

The host interface includes a slave-only SPI for device communications and configuration. A number of MAC features are implemented including CRC generation, CRC checking and receive frame filtering.

2 PIN CONNECTIONS

2.1 Pin Numbering

QFN-48 package with pin assignments as follows: -
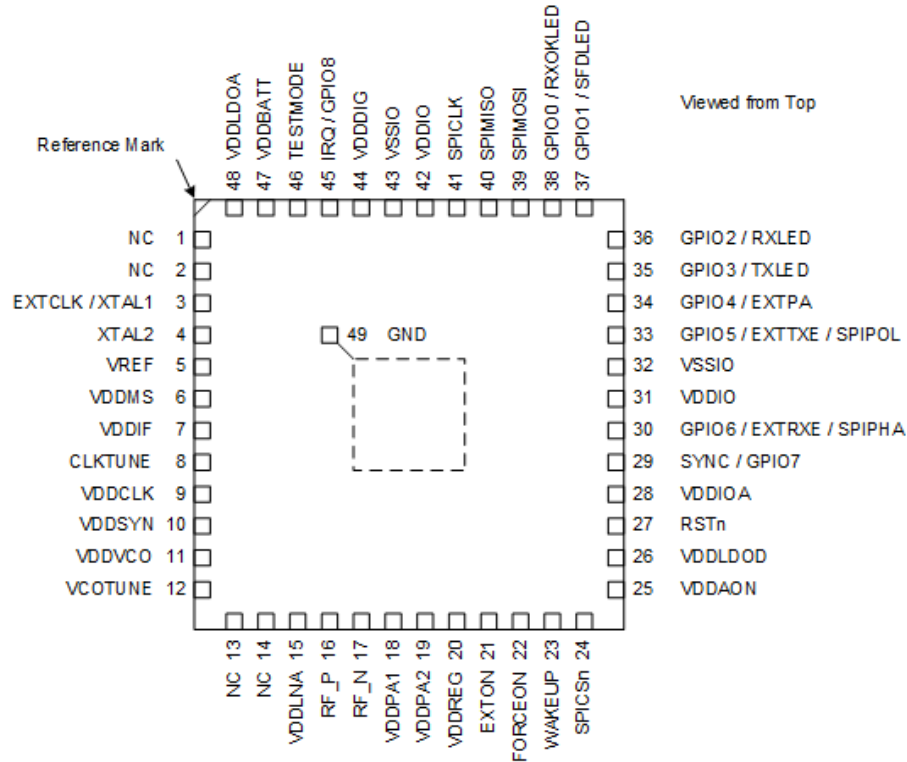
Figure 2: DW1000 Pin Assignments

2.2 Pin Descriptions

Table 1: DW1000 Pin functions

SIGNAL NAME	PIN	I/O (default)	DESCRIPTION
Crystal Interface			
EXTCLK / XTAL1	3	AI	Reference crystal input or external reference overdrive pin.
XTAL2	4	AI	Reference crystal input.
Digital Interface			
SPICLK	41	DI	SPI clock
SPIMISO	40	DO (O-L)	SPI data output. Refer to section 5.8.
SPIMOSI	39	DI	SPI data input. Refer to section 5.8.
SPICSn	24	DI	SPI chip select. This is an active low enable input. The high-to-low transition on SPICSn signals the start of a new SPI transaction. SPICSn can also act as a wake-up signal to bring DW1000 out of either SLEEP or DEEPSLEEP states. Refer to section 6.
SYNC / GPIO7	29	DIO (I)	The SYNC input pin is used for external synchronization (see section 5.13). When the SYNC input functionality is not being used this pin may be reconfigured as a general purpose I/O pin, GPIO7.
WAKEUP	23	DI	When asserted into its active high state, the WAKEUP pin brings the DW1000 out of SLEEP or DEEPSLEEP states into operational mode. When this pin is not being used as WAKEUP it should be tied to VSSIO

SIGNAL NAME	PIN	I/O (default)	DESCRIPTION
EXTON	21	DO (O-L)	External device enable. Asserted during wake up process and held active until device enters sleep mode. Can be used to control external DC-DC converters or other circuits that are not required when the device is in sleep mode so as to minimize power consumption. Refer to sections 5.5.1 & 7.
FORCEON	22	DI	Not used in normal operation. Must be connected to ground
IRQ / GPIO8	45	DIO (O-L)	Interrupt Request output from the DW1000 to the host processor. By default IRQ is an active-high output but may be configured to be active low if required. For correct operation in SLEEP and DEEPSLEEP modes it should be configured for active high operation. This pin will float in SLEEP and DEEPSLEEP states and may cause spurious interrupts unless pulled low. When the IRQ functionality is not being used the pin may be reconfigured as a general purpose I/O line, GPIO8. This pin has an internal pulldown to VSSIO and can be left unconnected if not being used.
GPIO6 / EXTRXE / SPIPHA	30	DIO (I)	General purpose I/O pin. On power-up it acts as the SPIPHA (SPI phase selection) pin for configuring the SPI operation mode. For details of this please refer to section 5.8. After power-up, the pin will default to a General Purpose I/O pin. It may be configured for use as EXTRXE (External Receiver Enable). This pin goes high when the DW1000 is in receive mode. This pin has an internal pulldown to VSSIO and can be left unconnected if not being used.
GPIO5 / EXTTXE / SPIPOL	33	DIO (I)	General purpose I/O pin. On power-up it acts as the SPIPOL (SPI polarity selection) pin for configuring the SPI mode of operation. Refer to section 5.8 for further information. After power-up, the pin will default to a General Purpose I/O pin. It may be configured for use as EXTTXE (External Transmit Enable). This pin goes high when the DW1000 is in transmit mode. This pin has an internal pulldown to VSSIO and can be left unconnected if not being used.
GPIO4 / EXTPA	34	DIO (I)	General purpose I/O pin. It may be configured for use as EXTPA (External Power Amplifier). This pin can enable an external Power Amplifier. This pin has an internal pulldown to VSSIO and can be left unconnected if not being used.
GPIO3 / TXLED	35	DIO (I)	General purpose I/O pin. It may be configured for use as a TXLED driving pin that can be used to light a LED following a transmission. Refer to the DW1000 User Manual [2] for details of LED use. This pin has an internal pulldown to VSSIO and can be left unconnected if not being used.
GPIO2 / RXLED	36	DIO (I)	General purpose I/O pin. It may be configured for use as a RXLED driving pin that can be used to light a LED during receive mode. Refer to the DW1000 User Manual [2] for details of LED use. This pin has an internal pulldown to VSSIO and can be left unconnected if not being used.
GPIO1 / SFDLED	37	DIO (I)	General purpose I/O pin. It may be configured for use as a SFDLED driving pin that can be used to light a LED when SFD (Start Frame Delimiter) is found by the receiver. Refer to the DW1000 User Manual [2] for details of LED use. This pin has an internal pulldown to VSSIO and can be left unconnected if not being used.

SIGNAL NAME	PIN	I/O (default)	DESCRIPTION
GPIO0 / RXOKLED	38	DIO (I)	General purpose I/O pin. It may be configured for use as a RXOKLED driving pin that can be used to light a LED on reception of a good frame. Refer to the DW1000 User Manual [2] for details of LED use. This pin has an internal pulldown to VSSIO and can be left unconnected if not being used.
RSTn	27	DIO (O-H)	Reset pin. Active Low Output. May be pulled low by external open drain driver to reset the DW1000. Must not be pulled high by external source. Refer to section 5.6**.**
TESTMODE	46	DI	Not used in normal operation. Must be connected to ground.
Reference voltages			
VREF	5	AIO	Used for on-chip reference current generation. Must be connected to an 11 kΩ (1% tolerance) resistor to ground.
Digital Power Supplies			
VDDLDOD	26	P	External supply for digital circuits.
VDDIOA	28	P	External supply for digital IO ring.
VSSIO	32 43	G	Negative I/O ring supply. Must be connected to ground.
Digital Decoupling			
VDDREG	20	PD	Output of on-chip regulator. Connect to VDDDIG on PCB if using the GPIOs to drive high-current outputs such as LEDs. Requires a local 100 nF capacitor to VSSIO.
VDDDIG	44	PD	Output of on-chip regulator. Connect to VDDREG on PCB if using the GPIOs to drive high-current outputs such as LEDs. Requires a local 100 nF capacitor to VSSIO.
VDDIO	31 42	PD	Digital IO Ring Decoupling.
RF Interface			
RF_P	16	AIO	Positive pin of the 100 Ω differential RF pair. Should be AC coupled.
RF_N	17	AIO	Negative pin of the 100 Ω differential RF pair. Should be AC coupled.
PLL Interface			
CLKTUNE	8	AIO	Clock PLL loop filter connection to off-chip filter components. Referenced to VDDCLK.
VCOTUNE	12	AIO	RF PLL loop filter connection to off-chip filter components. Referenced to VDDVCO.
Analog Power Supplies			
VDDAON	25	P	External supply for the Always-On (AON) portion of the chip. See 7.3
VDDPA1	18	P	External supply to the transmitter power amplifier.
VDDPA2	19	P	External supply to the transmitter power amplifier.
VDDLNA	15	P	External supply to the receiver LNA.
VDDLDOA	48	P	External supply to analog circuits.
VDDBATT	47	P	External supply to all other on-chip circuits. If a TCXO is being used with the DW1000 this pin should be supplied by the regulated supply used to power the TCXO. See Figure 37.
Analog Supply Decoupling			
VDDCLK	9	PD	Output of on-chip regulator to off-chip decoupling capacitor.
VDDIF	7	PD	Output of on-chip regulator to off-chip decoupling capacitor.
VDDMS	6	PD	Output of on-chip regulator to off-chip decoupling capacitor.
VDDSYN	10	PD	Output of on-chip regulator to off-chip decoupling capacitor.
VDDVCO	11	PD	Output of on-chip regulator to off-chip decoupling capacitor.
Ground Paddle			

SIGNAL NAME	PIN	I/O (default)	DESCRIPTION
GND	49	G	Ground Paddle on underside of package. Must be soldered to the PCB ground plane for thermal and RF performance.
Others			
NC	1 2 13 14	NC	Not used in normal operation. Do not connect.

Table 2: Explanation of Abbreviations

ABBREVIATION	EXPLANATION
AI	Analog Input
AIO	Analog Input / Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input / Output
DO	Digital Output
G	Ground
P	Power Supply
PD	Power Decoupling
NC	No Connect
O-L	Defaults to output, low level after reset
O-H	Defaults to output, high level after reset
I	Defaults to input.
Note: Any signal with the suffix 'n' indicates an active low signal.	

3 ELECTRICAL SPECIFICATIONS

3.1 Nominal Operating Conditions

Table 3: DW1000 Operating Conditions

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Operating temperature	-40		+85	˚C	
Supply voltage VDDIOA	2.8	3.3	3.6	V	
Supply voltage VDDBATT, VDDAON, VDDLNA, VDDPA	2.8	3.3	3.6	V	
Supply voltage VDDLDOA, VDDLDOD	1.6	1.8	3.6	V	See section 7.2
Optional: Supply voltage VDDIO	3.7	3.8	3.9	V	Only to be used if programming the OTP memory. See the DW1000 User Manual [2] for details.
Voltage on GPIO0..8, WAKEUP, RSTn, SPICSn, SPIMOSI, SPICLK, TESTMODE, FORCEON			3.6	V	Note that 3.6 V is the max voltage that should be applied to these pins

Note: Unit operation is guaranteed by design when operating within these ranges

3.2 DC Characteristics

T_{amb} = 25 ˚C, all supplies centered on typical values

Table 4: DW1000 DC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Supply current DEEP SLEEP mode		50		nA	Total current drawn from all 3.3 V and 1.8 V supplies.
Supply current SLEEP mode		1		µA	
Supply current IDLE mode		19		mA	
Supply current INIT mode		5		mA	
TX : 3.3 V supplies (VDDBAT, VDDPA1, VDDPA2, VDDLNA, VDDAON, VDDIOA)			70	mA	Channel 5 TX Power = MAX mean (-9.3 dBm/500 MHz)
TX : 1.8 V supplies (VDDLDOA, VDDLDOD)			90*	mA	
RX : 3.3 V supplies (VDDBAT, VDDPA1, VDDPA2, VDDLNA, VDDAON, VDDIOA)			30	mA	Channel 5
RX : 1.8 V supplies (VDDLDOA, VDDLDOD)			210*	mA	
Digital input voltage high	0.7*VDDIO			V	
Digital input voltage low			0.3*VDDIO	V	
Digital output voltage high	0.7*VDDIO			V	Assumes 500 Ω load.
Digital output voltage low			0.3*VDDIO	V	Assumes 500 Ω load.
Digital Output Drive Current GPIOx, IRQ SPIMISO EXTON	4 8 3	6 10 4		mA	

* These currents are on the 1.8 V supplies, not referenced back to the 3.3 V supply

3.3 Receiver AC Characteristics

T_{amb} = 25 ˚C, all supplies centered on nominal values

Table 5: DW1000 Receiver AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Frequency range	3244		6999	MHz	

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Channel bandwidths		500 900		MHz	Channel 1,2,3 and 5 Channel 4 and 7
Input P1Db compression point			-39	dBm	Measured at balun input
In-band blocking level		30		dBc	Continuous wave interferer
Out-of-band blocking level		55		dBc	Continuous wave interferer
Relative velocity between Receiver & Transmitter	0		5	m/s	4096 preamble 110kbps, 128 bytes
	0		500	m/s	64 preamble 6.8 Mbps, 12 bytes

3.4 Receiver Sensitivity Characteristics

T_{amb} = 25 ˚C, all supplies centered on typical values. 20 byte payload

Table 6: Typical Receiver Sensitivity Characteristics

Packet Error Rate	Data Rate	Typical Receiver Sensitivity	Units	Condition/Note	
1%	110 kbps	-106	dBm/500 MHz	Preamble 2048	Carrier frequency offset ±1 ppm. Requires use of the "tight" Rx operating parameter set – see [2]	All measurements performed on Channel 5, PRF 16 MHz. Channel 2 is approximately 1 dB less sensitive
10%	110 kbps	-107	dBm/500 MHz	Preamble 2048	
1%	110 kbps	-102	dBm/500 MHz	Preamble 2048	Carrier frequency offset ±10 ppm
	850 kbps	-101	dBm/500 MHz	Preamble 1024	
	6.8 Mbps	-93 (*-97)	dBm/500 MHz	Preamble 256	
10%	110 kbps	-106	dBm/500 MHz	Preamble 2048	
	850 kbps	-102	dBm/500 MHz	Preamble 1024	
	6.8 Mbps	-94 (*-98)	dBm/500 MHz	Preamble 256	

*equivalent sensitivity with Smart TX Power enabled

3.5 Reference Clock AC Characteristics

T_{amb} = 25 ˚C, all supplies centered on typical values

3.5.1 Reference Frequency

Table 7: DW1000 Reference Clock AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Crystal oscillator reference frequency		38.4		MHz	A 38.4 MHz signal can be provided from an external reference in place of a crystal if desired. See Figure 37
Crystal specifications					
Load capacitance	0		35	pF	Depends on crystal used and PCB parasitics
Shunt capacitance	0		4	pF	
Drive level			200	µW	Depends on crystal & load capacitance used
Equivalent Series Resistance (ESR)			60	Ω	
Frequency tolerance			±20	ppm	DW1000 includes circuitry to trim the crystal oscillator to reduce the initial frequency offset.
Crystal trimming range		±25		ppm	Trimming range provided by on-chip circuitry. Depends on the crystal used and PCB design.
External Reference					
Amplitude	0.8			V_{pp}	Must be AC coupled. A coupling capacitor value of 2200 pF is recommended
SSB phase noise power			-132	dBc/Hz	@1 kHz offset.

Parameter	Min.	Typ.	Max.	Units	Condition/Note
density					
SSB phase noise power density			-145	dBc/Hz	@10 kHz offset.
Duty Cycle	40		60	%	
Low Power RC Oscillator	5	12	15	kHz	

3.6 Transmitter AC Characteristics

T_{amb} = 25 ˚C, all supplies centered on typical values

Table 8: DW1000 Transmitter AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Frequency range	3244		6999	MHz	
Channel Bandwidths		500 900		MHz	Channel 1, 2, 3 and 5 Channel 4 and 7
Output power spectral density (programmable)		-39	-35	dBm/MHz	See Section 5.5
Load impedance		100		Ω	Differential
Power level range		37		dB	
Coarse Power level step		3		dB	
Fine Power level step		0.5		dB	
Output power variation with temperature		0.05		dB/^{O}C	
Output power variation with voltage		2.73 3.34		dB/V	Channel 2 Channel 5

3.7 Temperature and Voltage Monitor Characteristics

Table 9: DW1000 Temperature and Voltage Monitor Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Voltage Monitor Range	2.4		3.75	V	
Voltage Monitor Precision		20		mV	
Voltage Monitor Accuracy		140		mV	
Temperature Monitor Range	-40		+100	°C	
Temperature Monitor Precision		0.9		°C	
Temperature Monitor Accuracy		2		°C	

3.8 Absolute Maximum Ratings

Table 10: DW1000 Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Voltage VDDPA / VDDLNA / VDDLDOD / VDDLDOA / VDDBATT / VDDIOA / VDDAON / VDDIO	-0.3	4.0	V
Receiver Power		0	dBm
Temperature - Storage temperature	-65	+150	˚C
Temperature – Operating temperature	-40	+85	˚C
ESD (Human Body Model)		2000	V

Stresses beyond those listed in this table may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operating conditions of the specification is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

4 TYPICAL PERFORMANCE
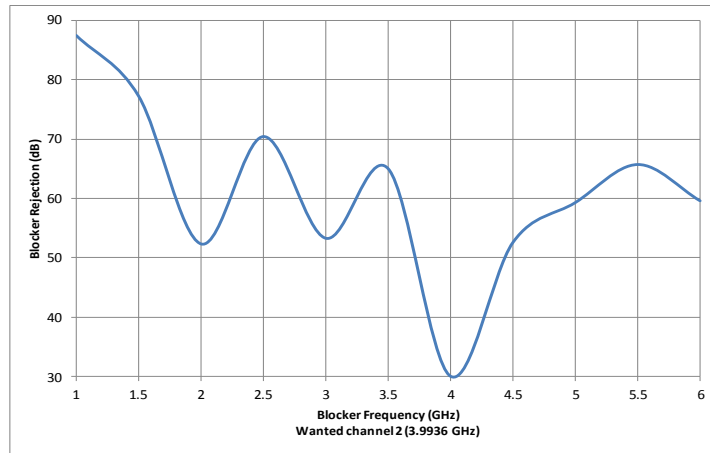
Figure 3 : RX Interferer Immunity on Channel 2
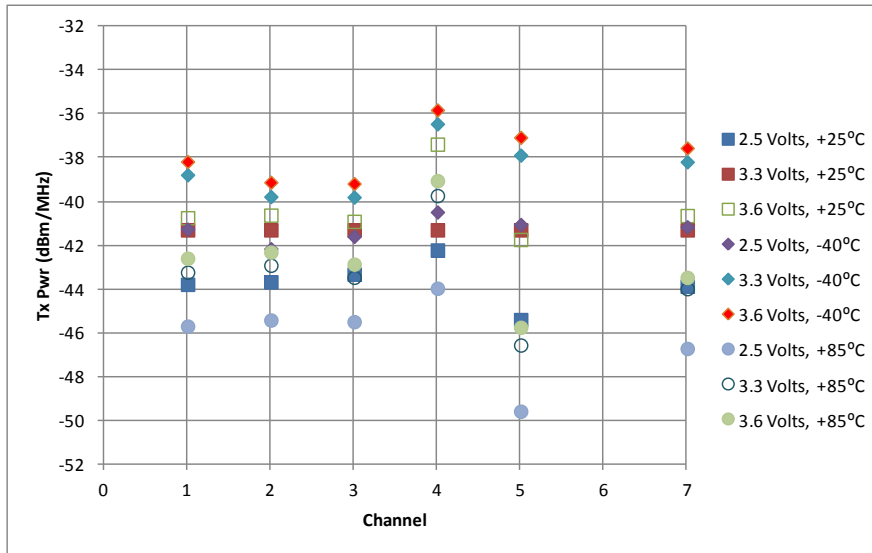
Figure 4: TX output Power over Temp & Voltage

(note that 2.5 volt data points are shown for information only)
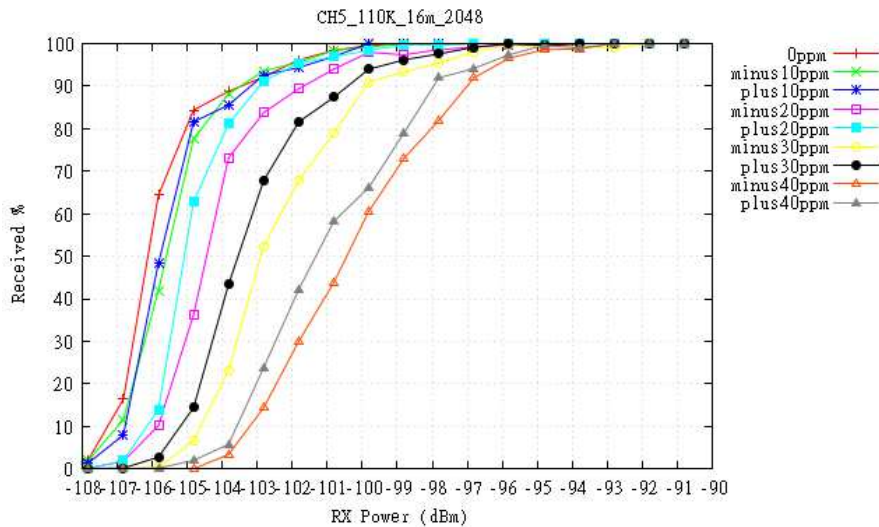
Figure 5: Receiver Sensitivity Channel 5 110kbps Data Rate 16 MHz PRF 2048 Preamble Symbols
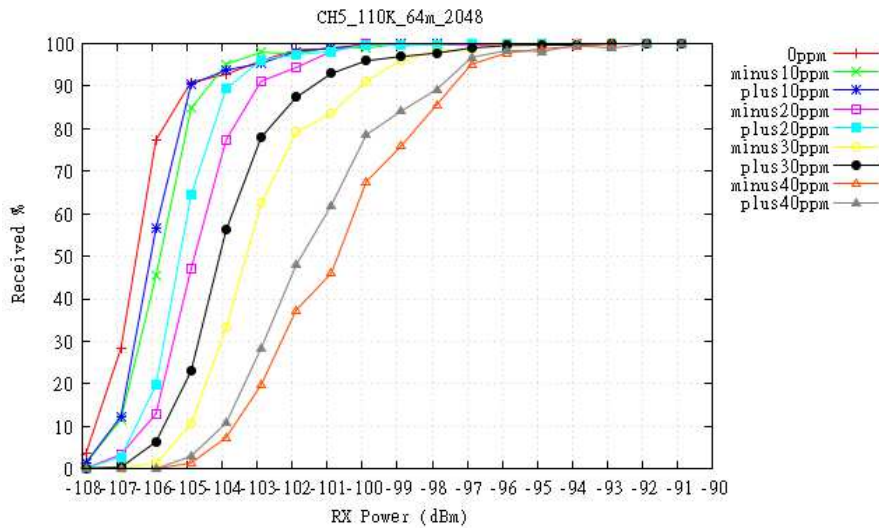
Figure 6: Receiver Sensitivity Channel 5 110kbps Data Rate 64 MHz PRF 2048 Preamble Symbols
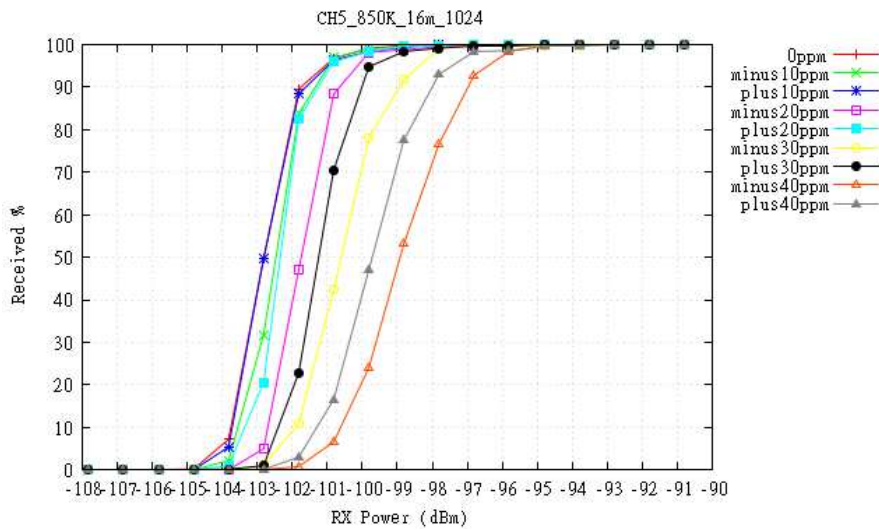
Figure 7: Receiver Sensitivity Channel 5 850kbps Data Rate 16 MHz PRF 1024 Preamble Symbols
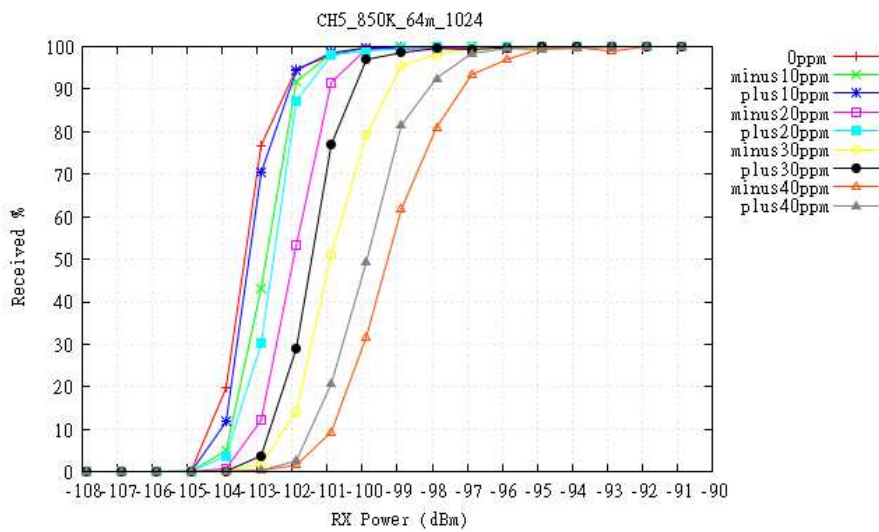
Figure 8: Receiver Sensitivity Channel 5 850kbps Data Rate 64 MHz PRF 1024 Preamble Symbols
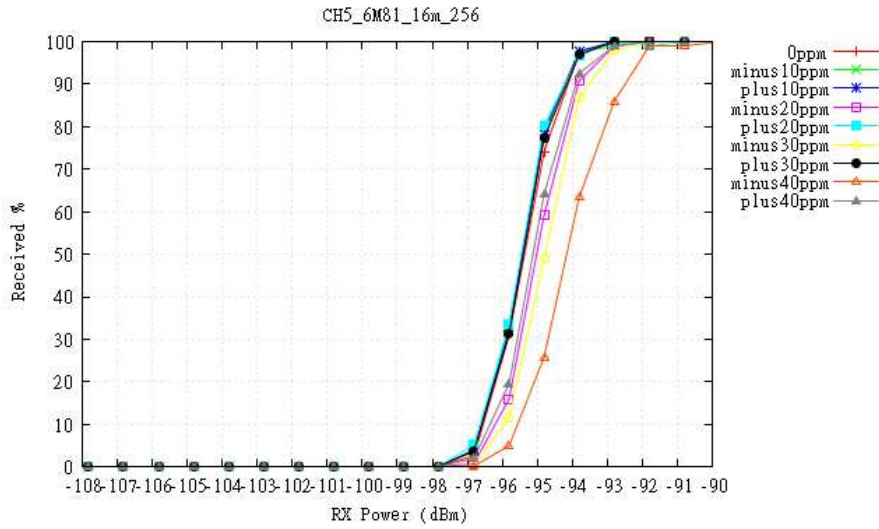
Figure 9: Receiver Sensitivity Channel 5 6.81Mbps Data Rate 16 MHz PRF 256 Preamble Symbols
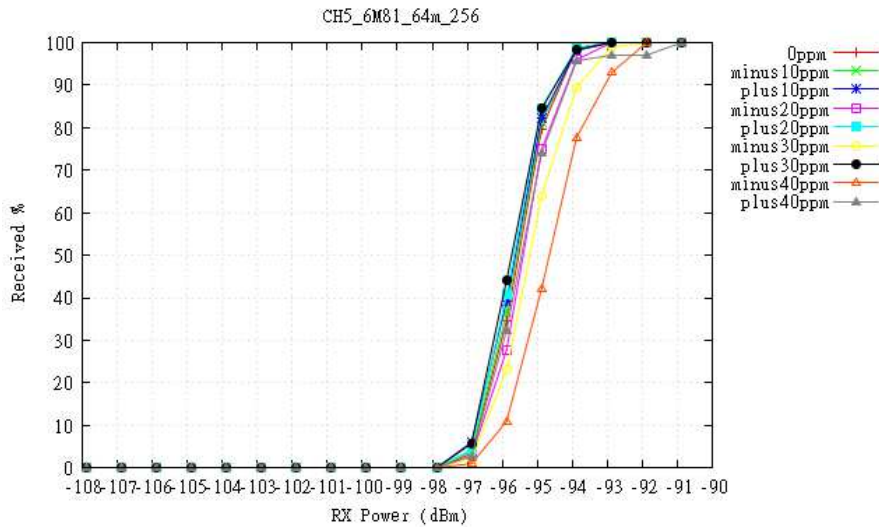
Figure 10: Receiver Sensitivity Channel 5 6.81Mbps Data Rate 64 MHz PRF 1256 Preamble Symbols
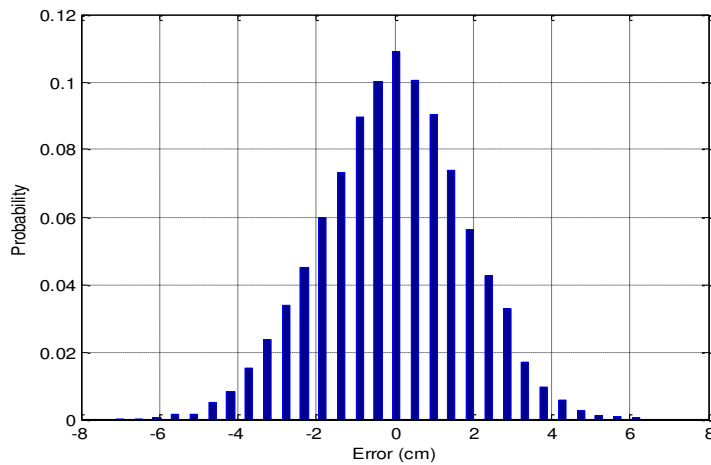
Figure 11: Typical probability distribution of Line of Sight 2-way ranging performance
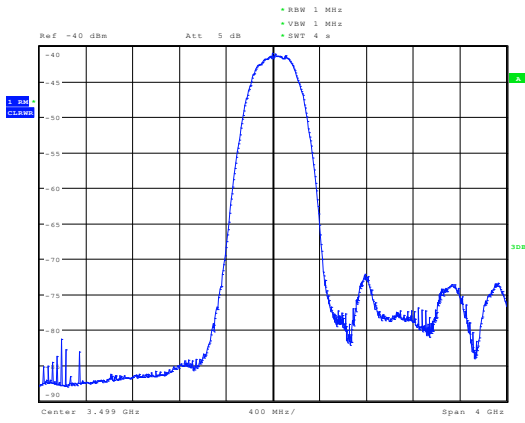
Date: 25.SEP.2013 16:07:44

Figure 12: TX Spectrum Channel 1
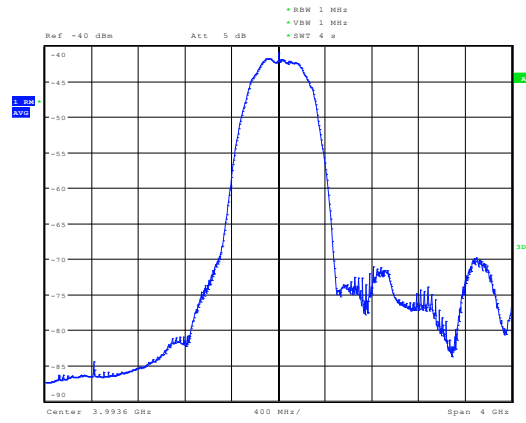
Date: 25.SEP.2013 15:47:44

Figure 13: TX Spectrum Channel 2
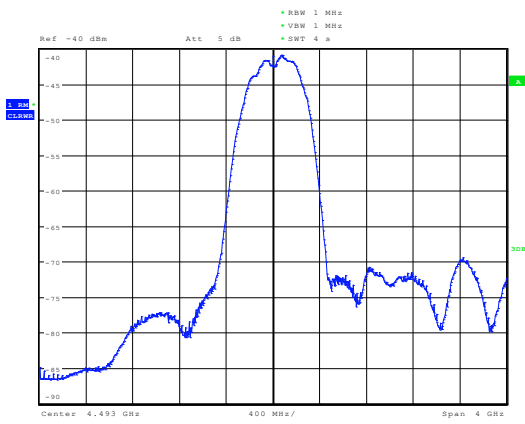
Date: 25.SEP.2013 16:09:23

Figure 14: TX Spectrum Channel 3
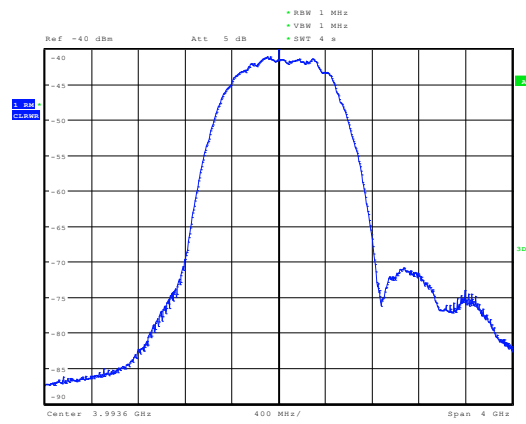
Date: 25.SEP.2013 15:49:33

Figure 15: TX Spectrum Channel 4
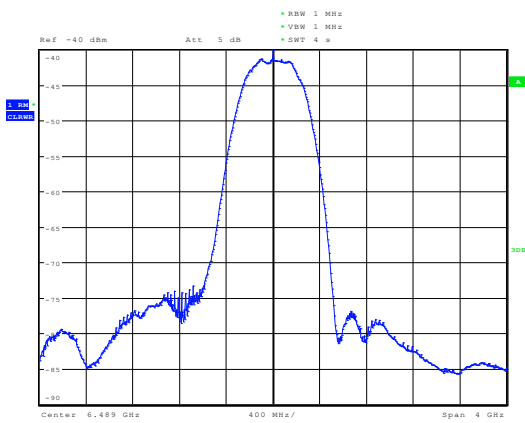
Date: 25.SEP.2013 16:10:30

Figure 16: TX Spectrum Channel 5
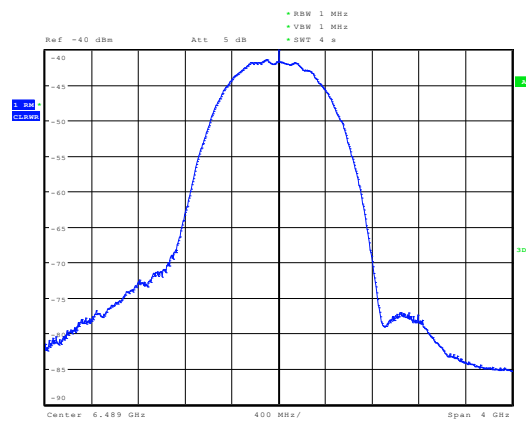
Date: 25.SEP.2013 16:20:23

Figure 17: TX Spectrum Channel 7

5 FUNCTIONAL DESCRIPTION

5.1 Physical Layer Modes

Please refer to IEEE802.15.4-2011 [1] for the PHY specification.

5.1.1 Supported Channels and Bandwidths

The DW1000 supports the following six IEEE802.15.4-2011 [1] UWB channels: -

Table 11: UWB IEEE802.15.4-2011 UWB channels supported by the DW1000

UWB Channel Number	Centre Frequency (MHz)	Band (MHz)	Bandwidth (MHz)
1	3494.4	3244.8 – 3744	499.2
2	3993.6	3774 – 4243.2	499.2
3	4492.8	4243.2 – 4742.4	499.2
4	3993.6	3328 – 4659.2	1331.2*
5	6489.6	6240 – 6739.2	499.2
7	6489.6	5980.3 – 6998.9	1081.6*

DW1000 maximum receiver bandwidth is approximately 900 MHz

5.1.2 Supported Bit Rates and Pulse Repetition Frequencies (PRF)

The DW1000 supports IEEE802.15.4-2011 [1] UWB standard bit rates of 110 kbps, 850 kbps and 6.81 Mbps and nominal PRF values of 16 and 64 MHz.

Table 12: UWB IEEE802.15.4-2011 [1] UWB bit rates and PRF modes supported by the DW1000

PRF* (MHz)	Data Rate (Mbps)
16	0.11
16	0.85
16	6.81
64	0.11
64	0.85
64	6.81

Actual PRF mean values are slightly higher for SYNC as opposed to the other portions of a frame. Mean PRF values are 16.1/15.6 MHz and 62.89/62.4 MHz, nominally referred to as 16 and 64MHz in this document. Refer to [1] for full details of peak and mean PRFs.

Generally speaking, lower data rates give increased receiver sensitivity, increased link margin and longer range but due to longer frame lengths for a given number of data bytes they result in increased air occupancy per frame and a reduction in the number of individual transmissions that can take place per unit time.

16 MHz PRF gives a marginal reduction in transmitter power consumption over 64 MHz PRF. 16 MHz and 64 MHz PRF can coexist on the same physical channel without interfering.

5.1.3 Frame Format

IEEE802.15.4-2011 [1] frames are structured as shown in Figure 18. Detailed descriptions of the frame format are given in the standard [1]. The frame consists of a synchronisation header (SHR) which includes the preamble symbols and start frame delimiter (SFD), followed by the PHY header (PHR) and data. The data frame is usually specified in number of bytes and the frame format will include 48 Reed-Solomon parity bits following each block of 330 data bits (or less).

The maximum standard frame length is 127 bytes, including the 2-byte FCS.
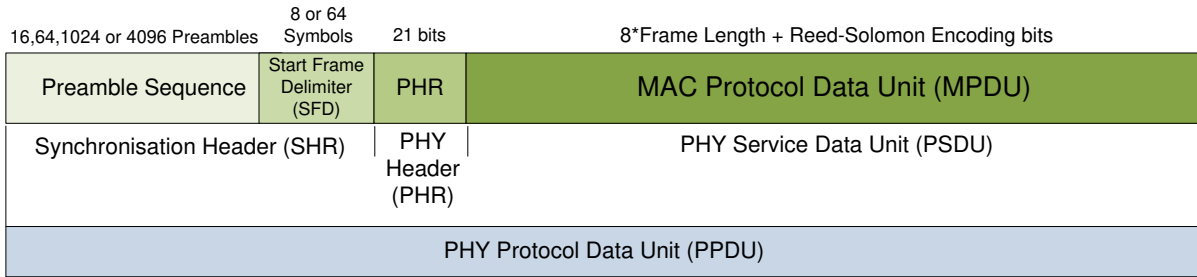
Figure 18: IEEE802.15.4-2011 PPDU Structure

5.1.4   Symbol Timings

Timing durations in IEEE802.15.4-2011 [1] are expressed in an integer number of symbols. This convention is adopted in DW1000 documentation. Symbol times vary depending on the data rate and PRF configuration of the device and the part of the frame. See Table 13: DW1000 Symbol Durations, for all symbol timings supported by DW1000.

Table 13: DW1000 Symbol Durations

PRF (MHz)	Data Rate (Mbps)	SHR (ns)	PHR (ns)	Data (ns)
16	0.11	993.59	8205.13	8205.13
16	0.85	993.59	1025.64	1025.64
16	6.81	993.59	1025.64	128.21
64	0.11	1017.63	8205.13	8205.13
64	0.85	1017.63	1025.64	1025.64
64	6.81	1017.63	1025.64	128.21

5.1.5   Proprietary Long Frames

The DW1000 offers a proprietary long frame mode where frames of up to 1023 bytes may be transferred. This requires a non-standard PHR encoding and so cannot be used in a standard system. Refer to the DW1000 User Manual for full details [2].

5.1.6   Turnaround Times

Turn-around times given in the table below are as defined in [1].

Table 14: Turn-around Times

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Turn-around time RX to TX*.		10		µs	Achievable turnaround time depends on device configuration and frame parameters and on external host controller.
Turn-around time TX to RX*.		6		µs	

5.1.7   Frame Filter

A standard frame filtering format is defined in IEEE802.15.4-2011 [1]. An overview of the MAC frame format is given in Figure 19 . Note that the Auxiliary Security Header is not processed in DW1000 hardware.
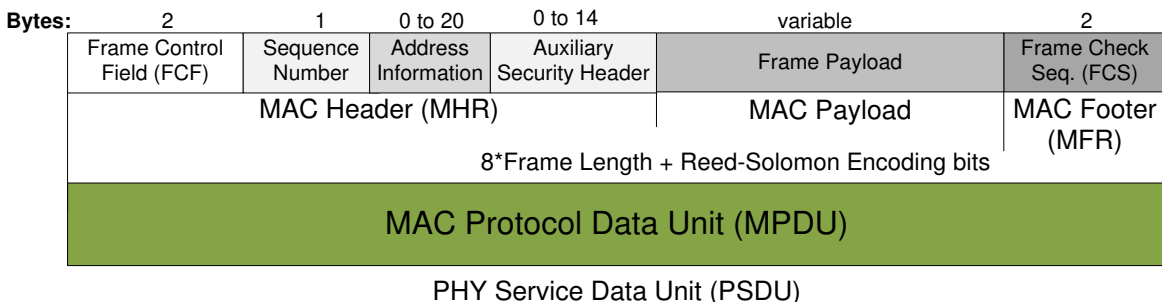
Figure 19: IEEE802.15.4-2011 MAC Frame Format

Frame filtering allows the receiver to automatically discard frames that do not match a defined set of criteria. The DW1000 has a number of separately configurable frame filtering criteria to allow selection of the frame types to accept or discard. See IEEE802.15.4-2011 [1] for filtering field definition and acceptance rules.

5.1.8 Frame Check Sequence (FCS)

The FCS is also known as the MAC Footer (MFR). It is a 2-byte CRC appended to frames. See IEEE802.15.4-2011 [1] for information on FCS generation.

5.2 Reference Crystal Oscillator

The on-chip crystal oscillator generates the reference frequency for the integrated frequency synthesizers RFPLL and CLKPLL. The oscillator operates at a frequency of 38.4 MHz.

DW1000 provides the facility to trim out initial frequency error in the 38.4 MHz reference crystal, see section 5.14. The trimming range depends on the crystal chosen and the loading capacitors used. Typically a trimming range of ±25 ppm is possible. Loading capacitors should be chosen such that minimum frequency error (from the channel center frequency) is achieved when the trim value is approximately mid-range.

In applications that require tighter frequency tolerance (maximum range) an external oscillator such as a TCXO can be used to drive the XTAL1 pin directly.

5.3 Synthesizer

DW1000 contains 2 frequency synthesizers, RFPLL which is used as a local oscillator (LO) for the TX and RX and CLKPLL which is used as a system clock. Both of these synthesizers are fully integrated apart from external passive 2nd order loop filters. The component values for these loop filters do not change regardless of the RF channel used. The register programming values for these synthesizers is contained in the user manual [2]

5.4 Receiver

5.4.1 Bandwidth setting

The receiver can be configured to operate in one of two bandwidth modes; 500 MHz or 900 MHz. The selection of a particular bandwidth mode is made by register settings and is described in the DW1000 User Manual [2].

5.4.2 Automatic Gain Control (AGC)

Automatic Gain Control is provided to ensure optimum receiver performance by adjusting receiver gain for changing signal and environmental conditions. The DW1000 monitors the received signal level and makes appropriate automatic adjustments to ensure optimum receiver performance is maintained.

5.5 Transmitter

5.5.1 Transmit Output Power

DW1000 transmit power is fully adjustable as is the transmit spectrum width ensuring that applicable regulatory standards such as FCC [4] and ETSI [3] can be met. For maximum range the transmit power should be set such that the EIRP at the antenna is as close as possible to the maximum allowed, -41.3 dBm/MHz in most regions. See section 5.14.3 for more details.

5.5.2 Transmit Bandwidth Setting

The transmitter can be configured to operate over a wide range of bandwidths. The selection of a particular bandwidth mode is made by register settings and is described in the DW1000 User Manual [2].

Transmit spectral shape can also be adjusted to compensate for PCB and external components in order to give an optimal transmit spectral mask.

5.6 Power-up sequence

5.6.1 Typical power-up sequence
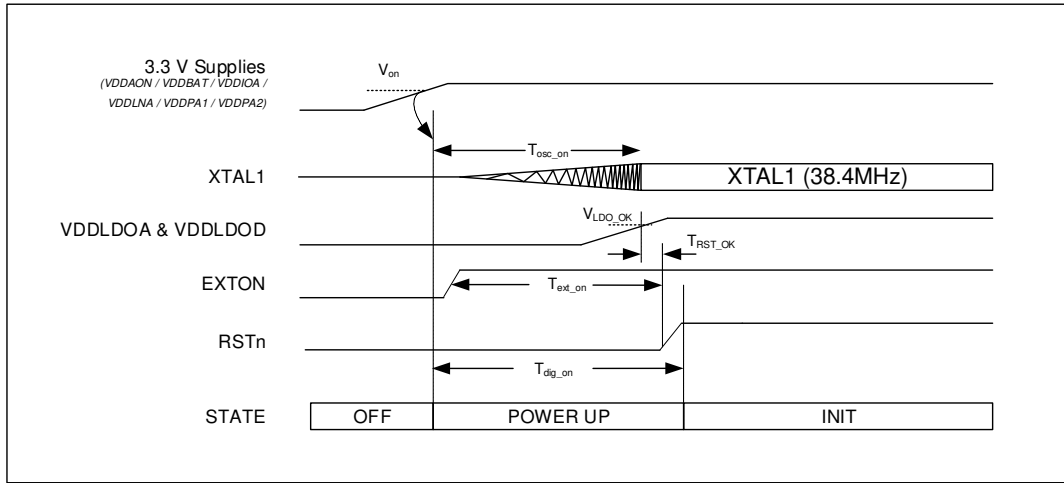
Figure 20: DW1000 Power-up Sequence

When power is applied to the DW1000, RSTn is driven low by the DW1000 internal circuitry as part of its power up sequence. See Figure 20 above. RSTn remains low until the XTAL oscillator has powered up and its output is suitable for use by the rest of the device. Once that time is reached the DW1000 de-asserts RSTn.

Table 15: DW1000 Power-up Timings

Parameter	Description	Min Value	Nominal Value	Units
V_{ON}	Voltage threshold to enable overall IC power up.		2.0	V
T_{OSC_ON}	Time taken for oscillator to start up and stabilise.	1.0	1.5	ms
T_{EXT_ON}	EXTON goes high this long before RSTn is released.	1.5	2	ms
T_{DIG_ON}	RSTn held low by internal reset circuit / driven low by external reset circuit.	1.5	2	ms
V_{LDO_OK}	Voltage threshold on the VDDLDOD supply at which the digital core powers up.	1.6		V
T_{RST_OK}	Time for which RSTn must continue to remain low once VDDLDOD exceeds V_{LDO_OK} min. If T_{RST_OK} min cannot be met due to the timing of the VDDLDOD supply ramp then RSTn should be manually driven low for at least T_{RST_OK} min time to ensure correct reset operation	10	50	ns

5.6.2 Variation in the power-up sequence

It is possible, that in some circuit arrangements, the start-up sequence may need to be altered. This can happen if, for example, the VDDLDOD supply is controlled via an external controller or if a slow ramp regulator is used to provide the VDDLDOD supply. In these situations the RSTn pin would have to be controlled by the external circuitry to ensure the digital circuits receive proper reset on power up.

Figure 21: Power up example where VDDLDOD cannot be guaranteed to be ready in time for the RSTn going high

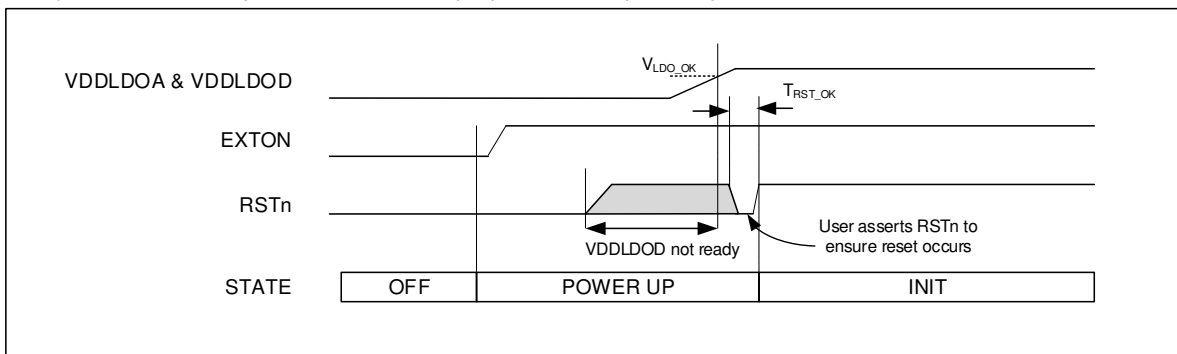Figure 21 shows a situation where the VDDLDOD supply is not high until after the first RSTn low to high transition (start of shaded area of RSTn). In this case the external circuitry must pull RSTn down again after the VDDLDOD supply has exceeded $V_{LDO\_OK.}$ This will ensure the digital circuits receive proper reset on power up. The RSTn pin should be either held low during power up until T_{RST_OK} is met or driven low for a minimum of $T_{RST\_OK.}$

5.6.3   External control of RSTn / use of RSTn by external circuitry

5.6.3.1   External control of RSTn

An external circuit can reset the DW1000 by asserting RSTn for a minimum of T_{RST_OK}. RSTn is an asynchronous input. DW1000 initialization will proceed when the RSTn pin is released to high impedance.

An external source should <u>open-drain</u> the RSTn pin once the DW1000 has been reset. If RSTn is controlled by a GPIO of an external micro-controller care should be taken to ensure that the GPIO is configured as high-impedance as soon as it is released from the LOW state.

When in DEEPSLEEP mode, the DW1000 drives RSTn to ground. This can result in current flowing if RSTn is driven high externally and will result in incorrect wake-up operation.

RSTn should never be driven high by an external source.

5.6.3.2   Use of RSTn by external circuitry

Table 16: External use of RSTn

Use of RSTn	Description
As output to control external circuitry	RSTn may be used as an **output** to reset external circuitry as part of an orderly bring up of a system as power is applied.
As interrupt input to external host	RSTn may be used as an **interrupt input** to the external host to indicate that the DW1000 has entered the INIT state. When RSTn is used in this way care should be taken to ensure that the interrupt pin of the external host does not pull-up the RSTn signal which should be left open-drain. Refer to Table 1 and Figure 37.

5.7   Voltage/Temperature Monitors

The on-chip voltage and temperature monitors allow the host to read the voltage on the VDDAON pin and the internal die temperature information from the DW1000. See Table 9 for characteristics.

5.8   Host Controller Interface

The DW1000 host communications interface is a slave-only SPI. Both clock polarities (SPIPOL=0/1) and phases (SPIPHA=0/1) are supported. The data transfer protocol supports single and multiple byte read/writes accesses. All bytes are transferred MSB first and LSB last. A transfer is initiated by asserting SPICSn low and terminated when SPICSn is deasserted high.

The DW1000 transfer protocols for each SPIPOL and SPIPHA setting are given in Figure 22 and Figure 23.

Note: Figure 22 and Figure 23 detail the SPI protocol as defined for SPICLK polarities and phases. The sampling and launch edges used by the SPI bus master are shown. DW1000 is a SPI slave device and will comply with the protocol by ensuring that the SPIMISO data is valid on the required SPICLK edge with setup and hold times as given by Table 18.
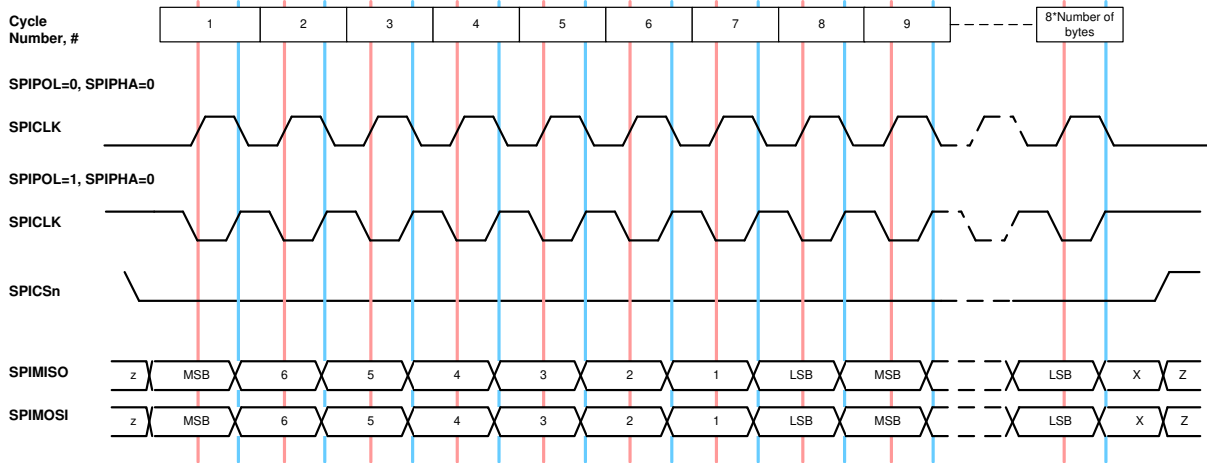
Figure 22: DW1000 SPIPHA=0 Transfer Protocol
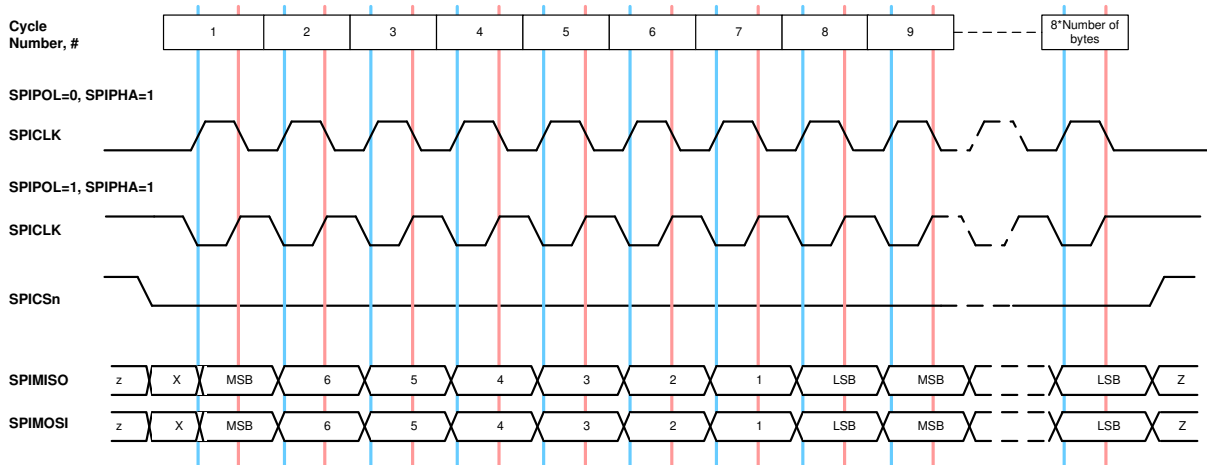
Figure 23: DW1000SPIPHA=1 Transfer Protocol

The MSB of the first byte is the read/write indicator, a low bit indicates a read access and a high bit indicates a write access. The second bit, bit 6 of the first byte, indicates whether a sub address byte will be included in the SPI access, a high bit indicates a further address byte to follow the initial byte and a low bit indicating that the bytes to follow the first byte are data. The 6 LSBs of the first byte contain an access address.

The second byte of a transfer command, if included, gives the sub address being accessed. If the MSB of this optional second byte is high, it indicates a second sub address byte to follow in the third transfer byte. The 7 LSBs of this second byte give the 7 LSBs of the sub address.

The third byte of a transfer command, if included give the 8 MSBs of the sub address.

The number of data bytes to follow the 1-3 command bytes is not limited by the DW1000 transfer protocol.

Figure 24: SPI Byte Formatting

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command	Read/Write 0 – Read 1 – Write	Sub address 0 – no sub address 1 – sub address present	6-bit access address					
Sub Address 0 (Optional)	Extended sub address 0 – 1 byte sub address 1 – 2 byte sub address	7-bits of sub address. These will be the LSBs if more bits are to follow.						
Sub Address 1 (Optional)	8 bits of sub address. These will form the MSBs, bits [14:7] of the 15-bit sub address.							
Data	8-bit read/write bytes (variable number).							

The SPIMISO line may be connected to multiple slave SPI devices each of which is required to go open-drain when their respective SPICSn lines are de-asserted.

The DW1000 has internal pull up and pull down circuits to ensure safe operation in the event of the host interface signals being disconnected. These are for internal use only, and should not be used to pull an external signal high or low.

Internal pull-down resistance values are in the range 34 kΩ – 90 kΩ, internal pull-up resistance values are in the range 40 kΩ - 90 kΩ.
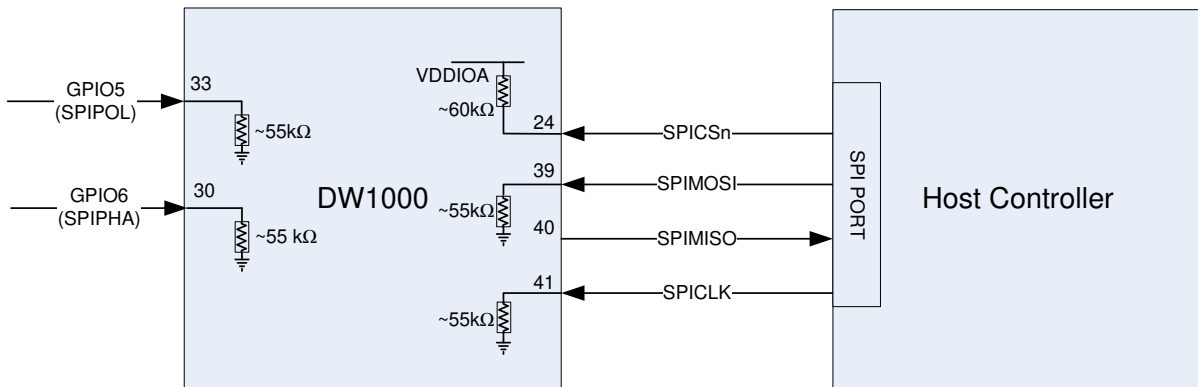

Figure 25: SPI Connections

More details of the protocol used for data transfer, the description of the accessible registers and the description of the bit functions of those registers are published in the DW1000 User Manual [2].

5.8.1 Configuring the SPI Mode

The SPI interface supports a number of different clock polarity and clock / data phase modes of operation. These modes are selected using GPIO5 & 6 as follows: -

Table 17: DW1000 SPI Mode Configuration

GPIO 5 (SPIPOL)	GPIO 6 (SPIPHA)	SPI Mode	Description (from the master / host point of view)
0	0	0	Data is sampled on the rising (first) edge of the clock and launched on the falling (second) edge.
0	1	1	Data is sampled on the falling (second) edge of the clock and launched on the rising (first) edge.
1	0	2	Data is sampled on the falling (first) edge of the clock and launched on the rising (second) edge.
1	1	3	Data is sampled on the rising (second) edge of the clock and launched on the falling (first) edge.
Note: The 0 on the GPIO pins can either be open circuit or a pull down to ground. The 1 on the GPIO pins is a pull up to VDDIO.			

GPIO 5 / 6 are sampled / latched on the rising edge of the RSTn pin to determine the SPI mode. They are internally pulled low to configure a default SPI mode 0 without the use of external components. If a mode other 0 is required then they should be pulled up using an external resistor of value no greater than 10 kΩ to the VDDIO output supply.

If GPIO5 / 6 are also being used to control an external transmit / receive switch then external pull-up resistors of no less than 1 kΩ should be used so that the DW1000 can correctly drive these outputs in normal operation after the reset sequence / SPI configuration operation is complete.

The recommended range of resistance values to pull-up GPIO 5 / 6 is in the range of 1-10 kΩ. If it is required to pull-down GPIO 5 / 6, such as in the case where the signal is also pulled high at the input to an external IC, the resistor value chosen needs to take account of the DW1000 internal pull-down resistor values as well as those of any connected external pull-up resistors.

It is possible to set the SPI mode using the DW1000's one-time programmable configuration block to avoid the need for external components and to leave the GPIO free for use. This is a one-time activity and cannot be reversed so care must be taken to ensure that the desired SPI mode is set. Please refer to the DW1000 User Manual [2] for details of OTP use and configuration.
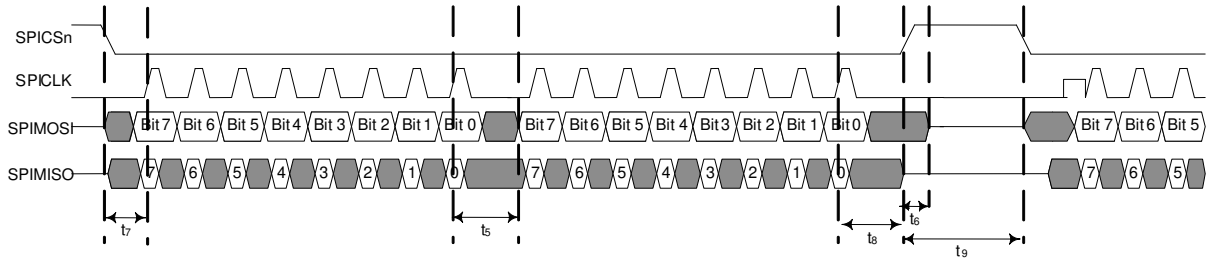
5.8.2 SPI Signal Timing
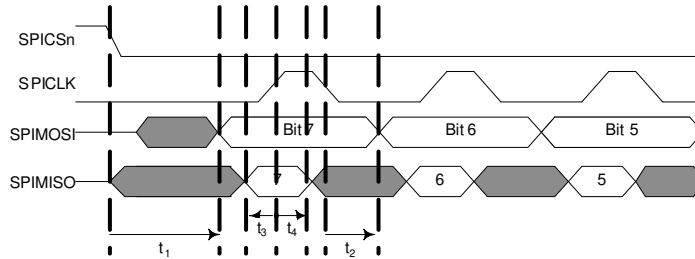

Figure 26: DW1000 SPI Timing Diagram

Figure 27: DW1000 SPI Detailed Timing Diagram

Table 18: DW1000 SPI Timing Parameters

Parameter	Min	Typ	Max	Unit	Description
SPICLK Period	50			ns	The maximum SPI frequency is 20 MHz when the CLKPLL is locked, otherwise the maximum SPI frequency is 3 MHz.
t_1			38	ns	SPICSn select asserted low to valid slave output data
t_2	12			ns	SPICLK low to valid slave output data
t_3	10			ns	Master data setup time
t_4	10			ns	Master data hold time
t_5	32			ns	LSB last byte to MSB next byte
t_6			10	ns	SPICSn de-asserted high to SPIMISO tri-state
t_7	16			ns	Start time; time from select asserted to first SPICLK
t_8	40			ns	Idle time between consecutive accesses
t_9	40			ns	Last SPICLK to SPICSn de-asserted

5.9 General Purpose Input Output (GPIO)

The DW1000 provides 8 user-configurable I/O pins.

On reset, all GPIO pins default to input. GPIO inputs, when appropriately configured, are capable of generating interrupts to the host processor via the IRQ signal. Some GPIO lines have multiple functions as described in 2.2 above.

GPIO0, 1, 2, & 3, as one of their optional functions, can drive LEDs to indicate the status of various chip operations. Any GPIO line being used to drive an LED in this way should be connected as shown. GPIO5 & 6 are used to configure the operating mode of the SPI as described in 5.8.1. GPIO4, 5 & 6 may be optionally used to implement a scheme with an external power amplifier to provide a transmit power level in excess of that provided by the DW1000.
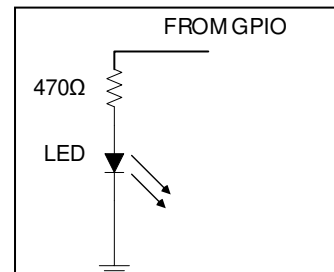
The DW1000 User Manual [2] provides details of the configuration and use of the GPIO lines.

5.10 Memory

The DW1000 includes a number of user accessible memories: -

5.10.1 Receive and Transmit data buffers

Buffers used to store received data to be read from the DW1000 by the host controller and data for transmission written into the DW1000 by the host controller. These are sized as follows: -

Table 19: Transmit & Receive Buffer Memory Size

Memory	Size (bits)	Description
Tx Buffer	1024 x 8	Transmit data buffer. Contains data written by the host processor to be transmitted via the transmitter
Rx Buffer	1024 x 8 x 2	Receive data buffer. Contains data received via the receiver to be read by the host processor via the SPI interface. Double buffered so that the receiver can receive a second packet while the first is being read by the host controller

5.10.2 Accumulator memory

The accumulator memory is used to store the channel impulse response estimate.

Table 20: Accumulator Memory Size

Memory	Size (bits)	Description
Accumulator	1016 x 32	Accumulator buffer. Used to store channel impulse response estimate data to be optionally read by the host controller

5.10.3 One Time Programmable (OTP) Calibration Memory

The DW1000 contains a small amount of user programmable OTP memory that is used to store per chip calibration information. When programming the OTP, the user should ensure that the VDDIO pins are supplied with 3.7 V minimum. If the VDDIO pin is unavailable, then the VDDIOA pin should be driven instead.

Table 21: OTP calibration memory

Memory	Size (bits)	Description
Calibration	56 x 32	One time programmable area of memory used for storing calibration data.

5.11 Interrupts and Device Status

DW1000 has a number of interrupt events that can be configured to drive the IRQ output pin. The default IRQ pin polarity is active high. A number of status registers are provided in the system to monitor and report data of interest. See DW1000 User Manual [2] for a full description of system interrupts and their configuration and status registers.

5.12 MAC Features

5.12.1 Timestamping

DW1000 generates transmit timestamps and captures receive timestamps. These timestamps are 40-bit values at a nominal 64 GHz resolution, for approximately 15 ps event timing precision. These timestamps enable ranging calculations.

DW1000 allows antenna delay values to be programmed for automatic adjustment of timestamps. See the DW1000 User Manual [2] for more details of DW1000 implementation and IEEE802.15.4-2011 [1] for details of definitions and required precision of timestamps and antenna delay values.

5.12.2 FCS Generation and Checking

DW1000 will automatically append a 2-byte FCS to transmitted frames and check received frames' FCS. The DW1000 can be used to send frames with a host-generated FCS, if desired.

5.12.3 Automatic Frame Filtering

Automatic frame filtering can be carried out using the DW1000. Incoming frames can be rejected automatically if they fail frame type or destination address checks. See the DW1000 User Manual [2] for details.