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DWM1000 *IEEE 802.15.4-2011 UWB Transceiver Module*

Product Overview

The DWM1000 module is based on Decawave's DW1000 Ultra Wideband (UWB) transceiver IC. It integrates antenna, all RF circuitry, power management and clock circuitry in one module. It can be used in 2-way ranging or TDOA location systems to locate assets to a precision of 10 cm and supports data rates of up to 6.8 Mbps

Key Features

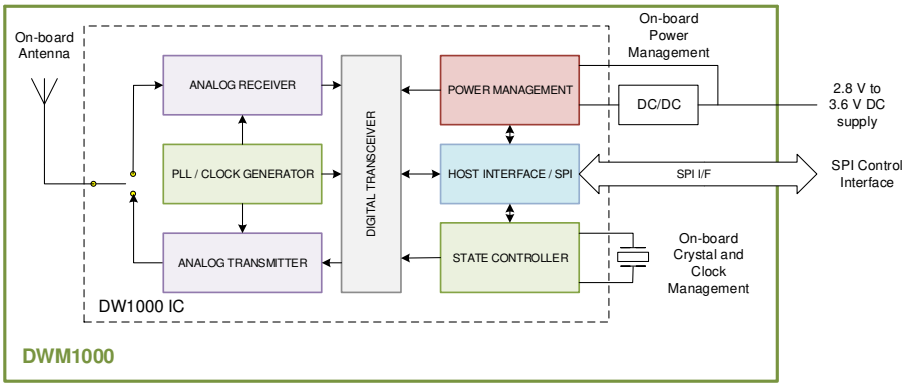
- IEEE 802.15.4-2011 UWB compliant
- Supports 4 RF bands from 3.5 GHz to 6.5 GHz
- Programmable transmitter output power
- Fully coherent receiver for maximum range and accuracy
- Designed to comply with FCC & ETSI UWB spectral masks
- Supply voltage 2.8 V to 3.6 V
- Low power consumption
- Data rates of 110 kbps, 850 kbps, 6.8 Mbps
- Maximum packet length of 1023 bytes for high data throughput applications
- Integrated MAC support features
- Supports 2-way ranging and TDOA
- SPI interface to host processor
- 23 mm x 13 mm x 2.9 mm 24-pin side castellation package

Key Benefits

- Simplifies integration, no RF design required
- Very precise location of tagged objects delivers enterprise efficiency gains and cost reductions
- Extended communications range minimises required infrastructure in RTLS
- High multipath fading immunity
- Supports very high tag densities in RTLS
- Low cost allows cost-effective implementation of solutions
- Low power consumption reduces the need to replace batteries and lowers system lifetime costs

Applications

- Precision real time location systems (RTLS) using two-way ranging or TDOA schemes in a variety of markets.
- Location aware wireless sensor networks (WSNs)



High Level Block Diagram

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DOCUMENT INFORMATION

Disclaimer

Decawave reserves the right to change product specifications without notice. As far as possible changes to functionality and specifications will be issued in product specific errata sheets or in new versions of this document. Customers are advised to check with Decawave for the most recent updates on this product.

LIFE SUPPORT POLICY

Decawave products are not authorized for use in safety-critical applications (such as life support) where a failure of the Decawave product would reasonably be expected to cause severe personal injury or death. Decawave customers using or selling Decawave products in such a manner do so entirely at their own risk and agree to fully indemnify Decawave and its representatives against any damages arising out of the use of Decawave products in such safety-critical applications.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

REGULATORY APPROVALS

The DWM1000, as supplied from Decawave, has not been certified for use in any particular geographic region by the appropriate regulatory body governing radio emissions in that region although it is capable of such certification depending on the region and the manner in which it is used.

All products developed by the user incorporating the DWM1000 must be approved by the relevant authority governing radio emissions in any given jurisdiction prior to the marketing or sale of such products in that jurisdiction and user bears all responsibility for obtaining such approval as needed from the appropriate authorities.

1 OVERVIEW

The DWM1000 module is an IEEE 802.15.4-2011 UWB implementation. RF components, Decawave DW1000 UWB transceiver, and other components reside on-module. DWM1000 enables cost effective and reduced complexity integration of UWB communications and ranging features, greatly accelerating design implementation.

1.1 DWM1000 Functional Description

The DW1000 on board the DWM1000 is a fully integrated low-power, single chip CMOS RF transceiver IC compliant with the IEEE 802.15.4-2011 [1] UWB standard. The DWM1000 module requires no RF design as the antenna and associated analog and RF components are on the module.

The module contains an on-board 38.4 MHz reference crystal. The crystal has been trimmed in production to reduce the initial frequency error to approximately 2 ppm, using the DW1000 IC's internal on-chip crystal trimming circuit, see section 2.1.1.

Always-On (AON) memory can be used to retain DWM1000 configuration data during the lowest power operational states when the on-chip voltage regulators are disabled. This data is uploaded and downloaded automatically. Use of DWM1000 AON memory is configurable.

The on-chip voltage and temperature monitors allow the host to read the voltage on the VDDAON pin and the internal die temperature information from the DW1000.

See the DW1000 Datasheet [2] for more detailed information on device functionality, electrical specifications and typical performance.

1.2 DWM1000 Power Up

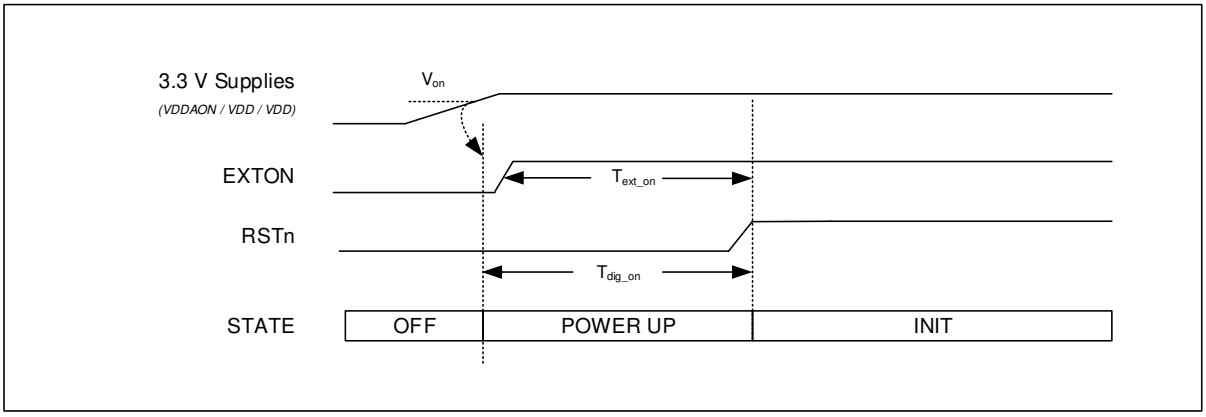


Figure 1: DWM1000 Power-up Sequence

When power is applied to the DWM1000, RSTn is driven low by internal circuitry as part of its power up sequence. See Figure 1 above. RSTn remains low until the on-module crystal oscillator has powered up and its output is suitable for use by the rest of the device, at which time RSTn is deasserted high.

Table 1: DW1000 Power-up Timings

Parameter	Description	Nominal Value	Units
V_{ON}	Voltage threshold to enable power up	2.0	V
T_{EXT_ON}	Time at which EXTON goes high before RSTn is released	3	ms
T_{DIG_ON}	RSTn held low by internal reset circuit / driven low by external reset circuit	3	ms

RSTn may be used as an output to reset external circuitry as part of system bring-up as power is applied.

An external circuit can reset the DWM1000 by asserting RSTn for a minimum of 10 ns. RSTn is an asynchronous input. DW1000 initialization will proceed when the pin is released to high impedance**. RSTn should never be driven high by an external source.**

Please see DW1000 Datasheet [2] for more details of DW1000 power up.

1.3 SPI Host Interface

The DW1000 host communications interface is a slave-only SPI. Both clock polarities (SPIPOL=0/1) and phases (SPIPHA=0/1) are supported. The data transfer protocol supports single and multiple byte read/writes accesses. All bytes are transferred MSB first and LSB last. A transfer is initiated by asserting SPICSn low and terminated when SPICSn is deasserted high.

See the DW1000 Datasheet [2] for full details of the SPI interface operation and mode configuration for clock phase and polarity.

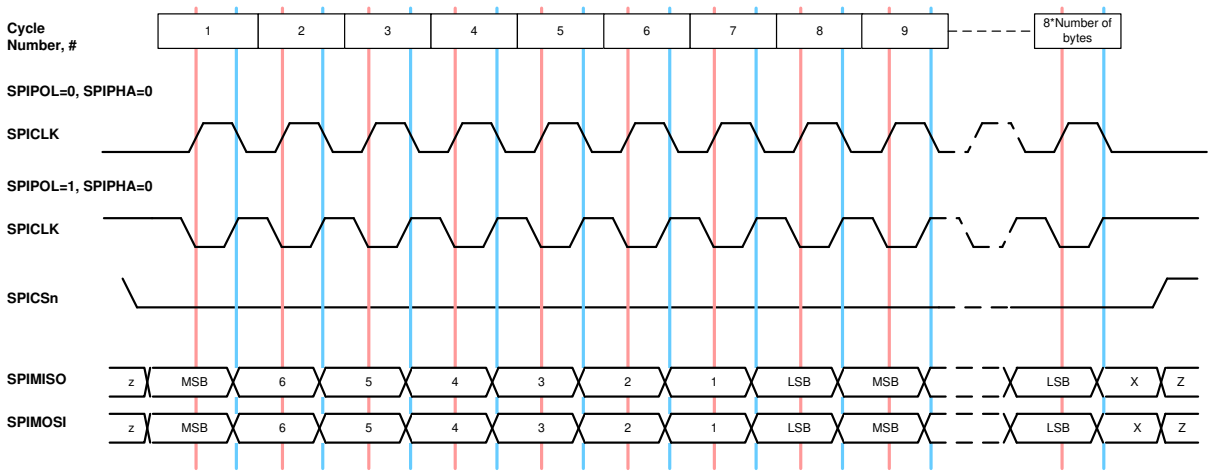


Figure 2: DW1000 SPIPHA=0 Transfer Protocol

1.3.1 SPI Signal Timing

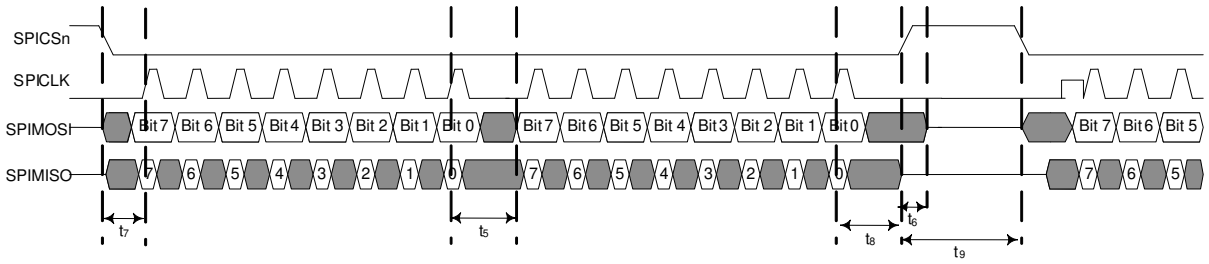


Figure 3: DWM1000 SPI Timing Diagram

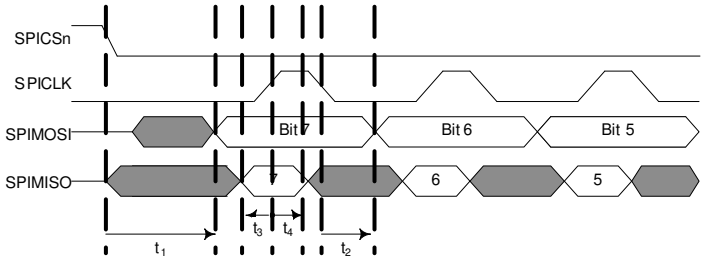


Figure 4: DWM1000 SPI Detailed Timing Diagram

Table 2: DWM1000 SPI Timing Parameters

Parameter	Min	Typ	Max	Unit	Description
SPICLK Period	50			ns	The maximum SPI frequency is 20 MHz when the CLKPLL is locked, otherwise the maximum SPI frequency is 3 MHz.
t_1			38	ns	SPICSn select asserted low to valid slave output data
t_2	12			ns	SPICLK low to valid slave output data
t_3	10			ns	Master data setup time
t_4	10			ns	Master data hold time
t_5	32			ns	LSB last byte to MSB next byte

Parameter	Min	Typ	Max	Unit	Description
t_6			10	ns	SPICSn de-asserted high to SPIMISO tri-state
t_7	16			ns	Start time; time from select asserted to first SPICLK
t_8	40			ns	Idle time between consecutive accesses
t_9	40			ns	Last SPICLK to SPICSn de-asserted

1.4 General Purpose Input Output (GPIO)

The DWM1000 provides 8 configurable pins.

On reset, all GPIO pins default to input. GPIO inputs, when appropriately configured, are capable of generating interrupts to the host processor via the IRQ signal.

GPIO0, 1, 2, & 3, as one of their optional functions, can drive LEDs to indicate the status of various chip operations. Any GPIO line being used to drive an LED in this way should be connected as shown. GPIO5 & 6 are used to configure the operating mode of the SPI as described in the DW1000 Datasheet [2].

See DW1000 Datasheet [2] and DW1000 User Manual [3] provide full details of the configuration and use of the GPIO lines.

1.5 Always-On (AON) Memory

Configuration retention in lowest power states is enabled in DWM1000 by provision of an Always-On (AON) memory array with a separate power supply, VDDAON. The DWM1000 may be configured to upload its configuration to AON before entering a low-power state and to download the configuration when waking up from the low –power state.

1.6 One-Time Programmable (OTP) Memory

The DWM1000 contains a 56x32 -bit user programmable OTP memory on the DW1000 device that is used to store per chip calibration information.

1.7 Interrupts and Device Status

DWM1000 has a number of interrupt events that can be configured to drive the IRQ output pin. The default IRQ pin polarity is active high. A number of status registers are provided in the system to monitor and report data of interest. See DW1000 User Manual [3] for a full description of system interrupts and their configuration and of status registers.

1.8 MAC

A number of MAC features are implemented including CRC generation, CRC checking and receive frame filtering. See the DW1000 Datasheet [2] and DW1000 User Manual [3] for full details.

2 DWM1000 CALIBRATION

Depending on the end-use application s and the system design, DWM1000 settings may need to be tuned. To help with this tuning a number of built in functions such as continuous wave TX and continuous packet transmission can be enabled. See the DW1000 User Manual [3] for further details.

2.1.1 Crystal Oscillator Trim

DWM1000 modules are calibrated at production to minimise initial frequency error to reduce carrier frequency offset between modules and thus improve receiver sensitivity. The calibration carried out at module production will trim the initial frequency offset to less than 2 ppm, typically.

2.1.2 Transmitter Calibration

In order to maximise range, DWM1000 transmit power spectral density (PSD) should be set to the maximum allowable for the geographic region in which it will be used. For most regions this is -41.3 dBm/MHz.

As the module contains an integrated antenna, the transmit power can only be measured over the air. The Effective Isotropic Radiated Power (EIRP) must be measured and the power level adjusted to ensure compliance with applicable regulations.

The DWM1000 provides the facility to adjust the transmit power in coarse and fine steps; 3 dB and 0.5 dB nominally. It also provides the ability to adjust the spectral bandwidth. These adjustments can be used to maximise transmit power whilst meeting regulatory spectral mask.

If required, transmit calibration should be carried out on a per DWM1000 module basis, see DW1000 User Manual [3] for full details.[1]

2.1.3 Antenna Delay Calibration

In order to measure range accurately, precise calculation of timestamps is required. To do this the antenna delay must be known. The DWM1000 allows this delay to be calibrated and provides the facility to compensate for delays introduced by PCB, external components, antenna and internal DWM1000 delays.

To calibrate the antenna delay, range is measured at a known distance using two DWM1000 systems. Antenna delay is adjusted until the known distance and reported range agree. The antenna delay can be stored in OTP memory.

Antenna delay calibration must be carried out as a once off measurement for each DWM1000 design implementation. If required, for greater accuracy, antenna delay calibration should be carried out on a per DWM1000 module basis, see DW1000 User Manual [3] for full details.

[1]To achieve best results when using the DWM1000 with Decawave's DecaRanging software, you will need to adjust the default transmit power value programmed into the DWM1000 by the software. This is because DecaRanging software is targeted at Decawave's EVB1000 evaluation board which has a different RF path compared to the DWM1000. You should increase the transmit power by approximately 3 dB.

3 DWM1000 PIN CONNECTIONS

3.1 Pin Numbering

DWM1000 module pin assignments are as follows (viewed from top): -

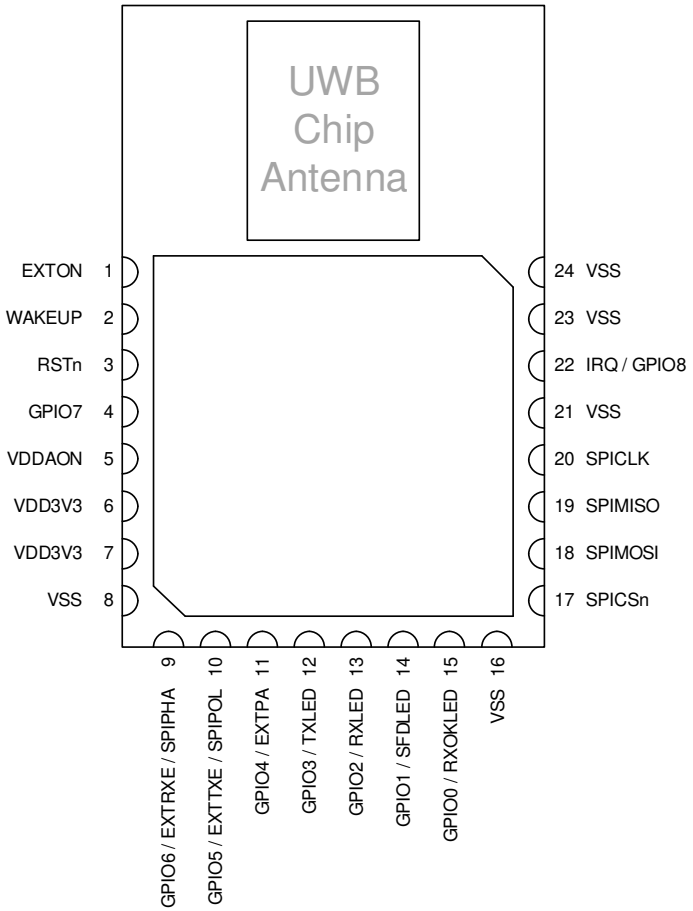


Figure 5: DWM1000 Pin Diagram

3.2 Pin Descriptions

Table 3: DWM1000 Pin functions

SIGNAL NAME	PIN	I/O (Default)	DESCRIPTION
Digital Interface			
SPICLK	20	DI	SPI clock
SPIMISO	19	DO (O–L)	SPI data output. Refer to DW1000 Datasheet for more details [2].
SPIMOSI	18	DI	SPI data input. Refer to DW1000 Datasheet for more details [2].
SPICSn	17	DI	SPI chip select. This is an active low enable input. The high-to-low transition on SPICSn signals the start of a new SPI transaction. SPICSn can also act as a wake-up signal to bring DW1000 out of either SLEEP or DEEPSLEEP states Refer to DW1000 Datasheet for more details [2].
WAKEUP	2	DIO	When asserted into its active high state, the WAKEUP pin brings the DW1000 out of SLEEP or DEEPSLEEP states into operational mode. If unused, this pin can be tied to ground.

SIGNAL NAME	PIN	I/O (Default)	DESCRIPTION
EXTON	1	DO (O-L)	External device enable. Asserted during wake up process and held active until device enters sleep mode. Can be used to control external DC-DC converters or other circuits that are not required when the device is in sleep mode so as to minimize power consumption. Refer to DW1000 Datasheet for more details [2].
IRQ / GPIO8	22	DIO (O-L)	Interrupt Request output from the DWM1000 to the host processor. By default IRQ is an active-high output but may be configured to be active low if required. For correct operation in SLEEP and DEEPSLEEP modes it should be configured for active high operation. This pin will float in SLEEP and DEEPSLEEP states and may cause spurious interrupts unless pulled low. When the IRQ functionality is not being used the pin may be reconfigured as a general purpose I/O line, GPIO8.
GPIO7	4	DIO (I)	Defaults to operate as a SYNC input – refer [2]. THIS FUNCTIONALITY IS NOT APPLICABLE TO THE DWM1000. This pin may be reconfigured as a general purpose I/O pin, GPIO7 under software control.
GPIO6 / SPIPHA	9	DIO (I)	General purpose I/O pin. On power-up it acts as the SPIPHA (SPI phase selection) pin for configuring the SPI mode of operation. Refer to Section 5.2.2 and the DW1000 Datasheet for more details [2]. After power-up, the pin will default to a General Purpose I/O pin.
GPIO5 / SPIPOL	10	DIO (I)	General purpose I/O pin. On power-up it acts as the SPIPOL (SPI polarity selection) pin for configuring the SPI operation mode. Refer to Section 5.2.2 and the DW1000 Datasheet for more details [2]. After power-up, the pin will default to a General Purpose I/O pin.
GPIO4	11	DIO (I)	General purpose I/O pin.
GPIO3 / TXLED	12	DIO (I)	General purpose I/O pin. It may be configured for use as a TXLED driving pin that can be used to light a LED following a transmission. Refer to the DW1000 User Manual [2] for details of LED use.
GPIO2 / RXLED	13	DIO (I)	General purpose I/O pin. It may be configured for use as a RXLED driving pin that can be used to light a LED during receive mode. Refer to the DW1000 User Manual [2] for details of LED use.
GPIO1 / SFDLED	14	DIO (I)	General purpose I/O pin. It may be configured for use as a SFDLED driving pin that can be used to light a LED when SFD (Start Frame Delimiter) is found by the receiver. Refer to the DW1000 User Manual [2] for details of LED use.
GPIO0 / RXOKLED	15	DIO (I)	General purpose I/O pin. It may be configured for use as a RXOKLED driving pin that can be used to light a LED on reception of a good frame. Refer to the DW1000 User Manual [2] for details of LED use.
RSTn	3	DIO (O-H)	Reset pin. Active Low Output. May be pulled low by external open drain driver to reset the DW1000. Refer to DW1000 Datasheet for more details [2].
Power Supplies			
VDDAON	5	P	External supply for the Always-On (AON) portion of the chip.
VDD3V3	6,7	P	3.3 V supply pins. Note that for programming the OTP in the DWM1000 module this voltage may be increased to a nominal value of 3.8 V for short periods.
Ground			
GND	8,16, 21,23,24	G	Common ground.

Table 4: Explanation of Abbreviations

ABBREVIATION	EXPLANATION
I	Input
IO	Input / Output
O	Output
G	Ground
P	Power Supply
PD	Power Decoupling
O-L	Defaults to output, low level after reset
O-H	Defaults to output, high level after reset
I	Defaults to input.
Note: Any signal with the suffix 'n' indicates an active low signal.	

4 ELECTRICAL SPECIFICATIONS

4.1 Nominal Operating Conditions

Table 5: DWM1000 Operating Conditions

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Operating temperature	-40		+85	˚C	
Supply voltage VDDAON, VDD3V3	2.8	3.3	3.6	V	Normal operation
Supply voltage VDD3V3 for programming OTP	3.7	3.8	3.9	V	Note that for programming the OTP in the DWM1000 the VDD3V3 voltage must be increased to 3.8 V nominal for short periods.
Voltage on GPIO0..7, WAKEUP, RSTn, SPICSn, SPIMOSI, SPICLK			3.6	V	Note that 3.6 V is the max voltage that may be applied to these pins

Note: Unit operation is guaranteed by design when operating within these ranges

4.2 DC Characteristics

T_{amb} = 25 ˚C, all supplies centred on typical values

Table 6: DWM1000 DC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Supply current DEEP SLEEP mode		200		nA	Total current drawn from all supplies.
Supply current SLEEP mode		550		nA	
Supply current IDLE mode		13.4		mA	
Supply current INIT mode		3.5		mA	
TX : 3.3 V supplies (VDDAON, VDD)			140	mA	Channel 5:TX Power: 9.3 dBm/500 MHz
RX : 3.3 V supplies (VDDAON, VDD)			160	mA	Channel 5
Digital input voltage high	0.7*VDD			V	
Digital input voltage low			0.3*VDD	V	
Digital output voltage high	0.7*VDD			V	Assumes 500 Ω load
Digital output voltage low			0.3*VDD	V	Assumes 500 Ω load
Digital Output Drive Current GPIOx, IRQ SPIMISO EXTON	 4 8 3	 6 10 4		mA	

4.3 Receiver AC Characteristics

T_{amb} = 25 ˚C, all supplies centred on nominal values

Table 7: DWM1000 Receiver AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Frequency range	3244		6999	MHz	
Channel bandwidth		500		MHz	Channel 1,2,3 and 5
In-band blocking level		30		dBc	Continuous wave interferer
Out-of-band blocking level		55		dBc	Continuous wave interferer

4.4 Receiver Sensitivity Characteristics

T_{amb} = 25 ˚C, all supplies centred on typical values. 20 byte payload. These sensitivity figures assume an antenna gain of 0 dBi and should be modified by the antenna characteristics quoted in Table 12 *depending on*

the orientation of the DWM1000.

Table 8: DWM1000 Typical Receiver Sensitivity Characteristics

Packet Error Rate	Data Rate	Receiver Sensitivity	Units	Condition/Note		
1%	110 kbps	-102	dBm/500 MHz	Preamble 2048	Carrier frequency offset ±10 ppm	All measurements performed on Channel 5, PRF 16 MHz Channel 2 is approximately 1 dB less sensitive
	850 kbps	-101	dBm/500 MHz	Preamble 1024		
	6.8 Mbps	-93	dBm/500 MHz	Preamble 256		
10%	110 kbps	-106	dBm/500 MHz	Preamble 2048		
	850 kbps	-102	dBm/500 MHz	Preamble 1024		
	6.8 Mbps	-94	dBm/500 MHz	Preamble 256		

4.5 Reference Clock AC Characteristics

T_{amb} = 25 ˚C, all supplies centred on typical values

4.5.1 Reference Frequency

Table 9: DWM1000 Reference Clock AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
On-board crystal oscillator reference frequency		38.4		MHz	
On-board crystal trimming range		±25		ppm	Internally trimmed to +/- 2 ppm under typical conditions.
On-board crystal frequency stability with temperature			±30*	ppm ppm	-40ºC to +85º
On-board crystal aging			±3	ppm/3year	@25ºC ±2ºC
Low Power RC Oscillator	5	12	15	kHz	

**By using the temperature monitoring capability of the DW1000 chip on the DWM1000 module it is possible to dynamically trim the crystal during run time to maintain the +/- 2ppm specification over the full temperature range of operation.*

4.6 Transmitter AC Characteristics

T_{amb} = 25 ˚C, all supplies centred on typical values

Table 10: DWM1000 Transmitter AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Frequency range	3244		6999	MHz	
Channel Bandwidths		500		MHz	Channel 1, 2, 3 and 5
Output power spectral density (programmable)		-39	-35	dBm/MHz	See DW1000 Datasheet [2]
Power level range		37		dB	
Coarse Power level step		3		dB	
Fine Power level step		0.5		dB	
Output power variation with temperature		0.05		dB/^{O}C	
Output power variation with voltage		2.73 3.34		dB/V	Channel 2 Channel 5

4.7 Temperature and Voltage Monitor Characteristics

Table 11: DWM1000 Temperature and Voltage Monitor Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Voltage Monitor Range	2.4		3.75	V	
Voltage Monitor Precision		20		mV	

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Voltage Monitor Accuracy		140		mV	
Temperature Monitor Range	-40		+100	°C	
Temperature Monitor Precision		0.9		°C	

4.8 Antenna Performance

The antenna used in the module is the Partron dielectric chip antenna, part number ACS5200HFAUWB, see [4] for full details.

Antenna radiation patterns, measured in an anechoic chamber for three planes, are shown in Figure 7. As the antenna is linearly polarised, in the Azimuth plane the vertically polarised field (Theta) is measured and the horizontally polarised field (Phi) is measured for elevation planes 1 and 2.

For these measurements, the DWM1000 module is mounted on a circuit board with dimensions shown in Figure 6.

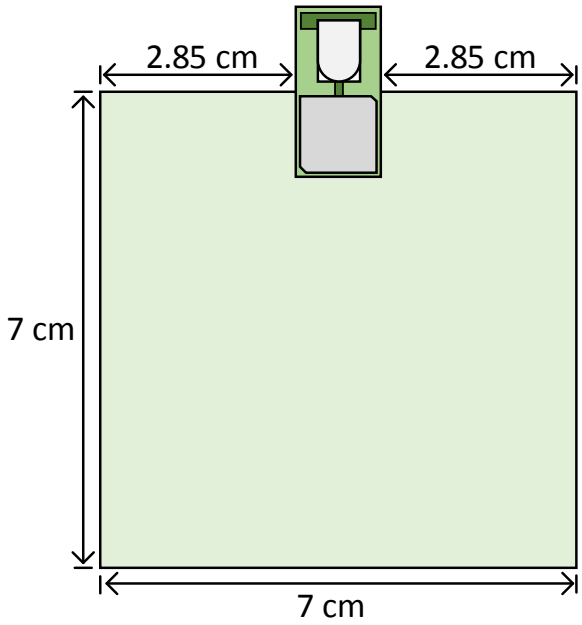


Figure 6. DWM1000 Circuit Board Mounting

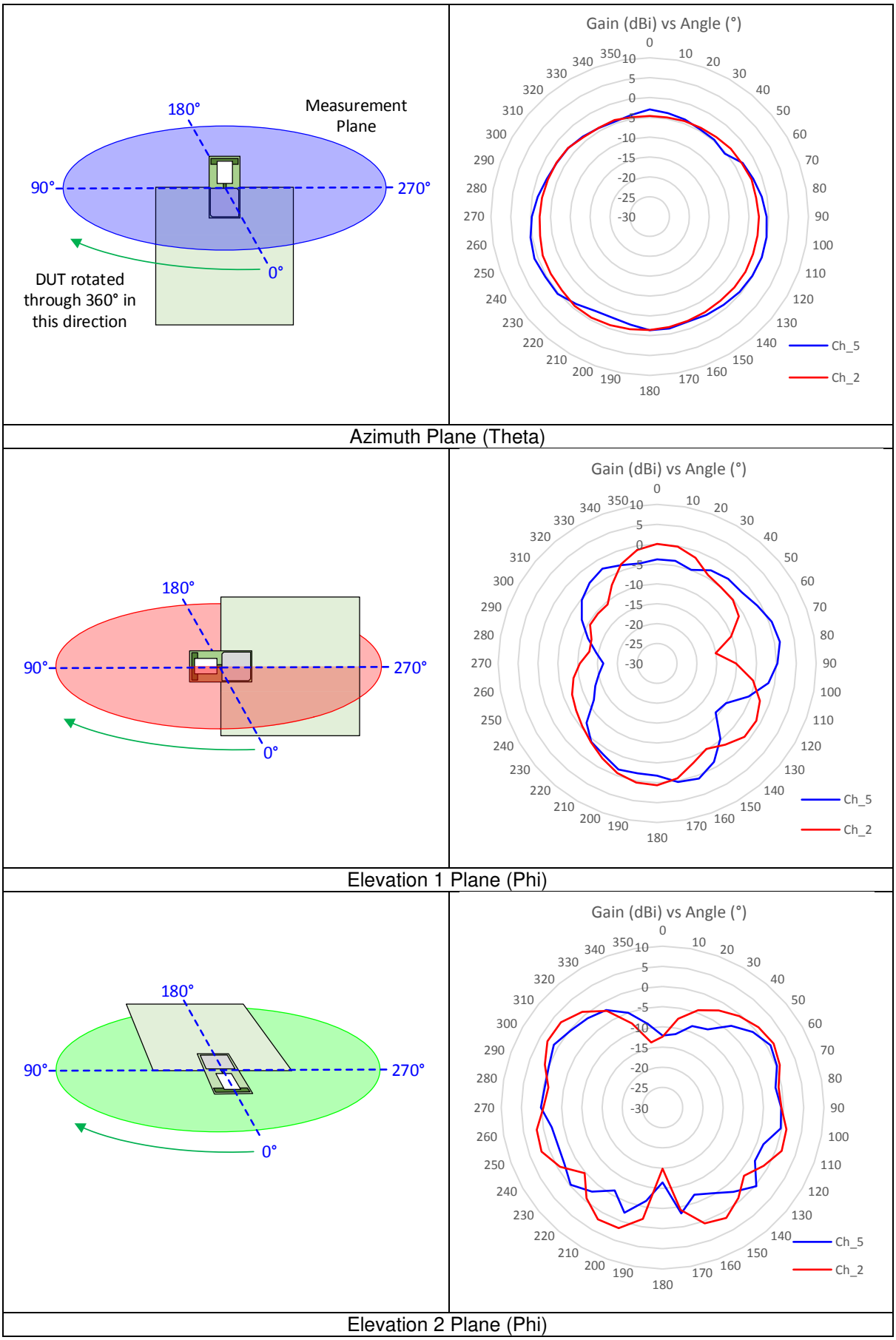


Figure 7. Measured Antenna Radiation Patterns

4.9 Absolute Maximum Ratings

Table 12: DWM1000 Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Voltage VDD3V3 / VDDAON	-0.3	4.0	V
Receiver Power		0	dBm
Temperature - Storage temperature	-40	+85	˚C
Temperature – Operating temperature	-40	+85	˚C
ESD (Human Body Model)		2000	V

Stresses beyond those listed in this table may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions beyond those indicated in the operating conditions of the specification is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5 APPLICATION INFORMATION

5.1 Application Board Layout Guidelines

When designing the PCB onto which DWM1000 will be soldered, the proximity of the DWM100 on-board ceramic monopole antenna to metal and other non-RF transparent materials needs to considered carefully. Two suggested placement schemes are shown below.

For best RF performance, ground copper should be flooded in all areas of the application board, except in the areas marked "Keep-Out Area", where there should be no metal either side, above or below (e.g. do not place battery under antenna).

The placement schemes in Figure 8 show an application board with no non-RF transparent material in the keep-out area, or an application board with the antenna projecting off of the board so that the keep out area is in free-space. In this second scheme it is still important not to place metal components above or below the antenna in a system implementation. It is also important to note that the ground plane on the application board affects the DWM1000 antenna radiation pattern. In Figure 8 below, d must be a minimum of 10 mm. This gives the most vertically polarized radiation pattern. As d is increased from 10 mm the degree of vertical polarization reduces.

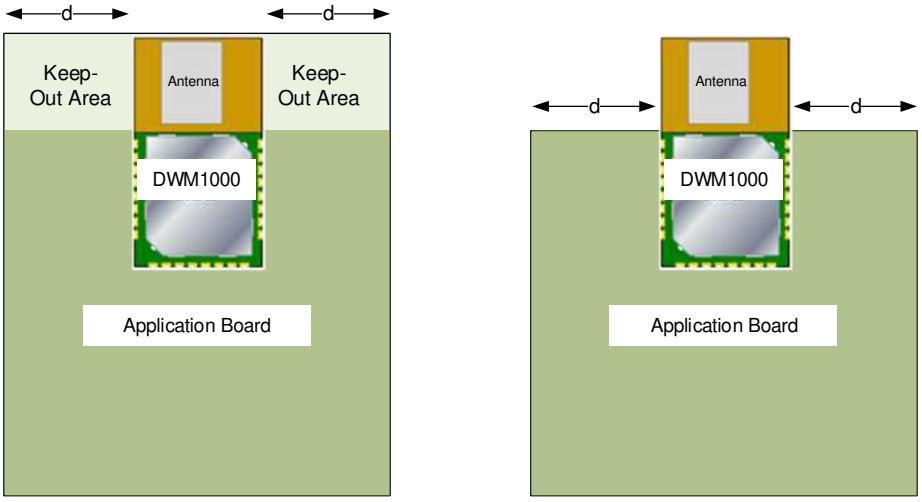


Figure 8: DWM1000 Application Board Keep-Out Areas

5.2 Application Circuit Diagram

A simple application circuit integrating the DWM1000 module need only power the device and connect the device to a host controller, see Figure 9.

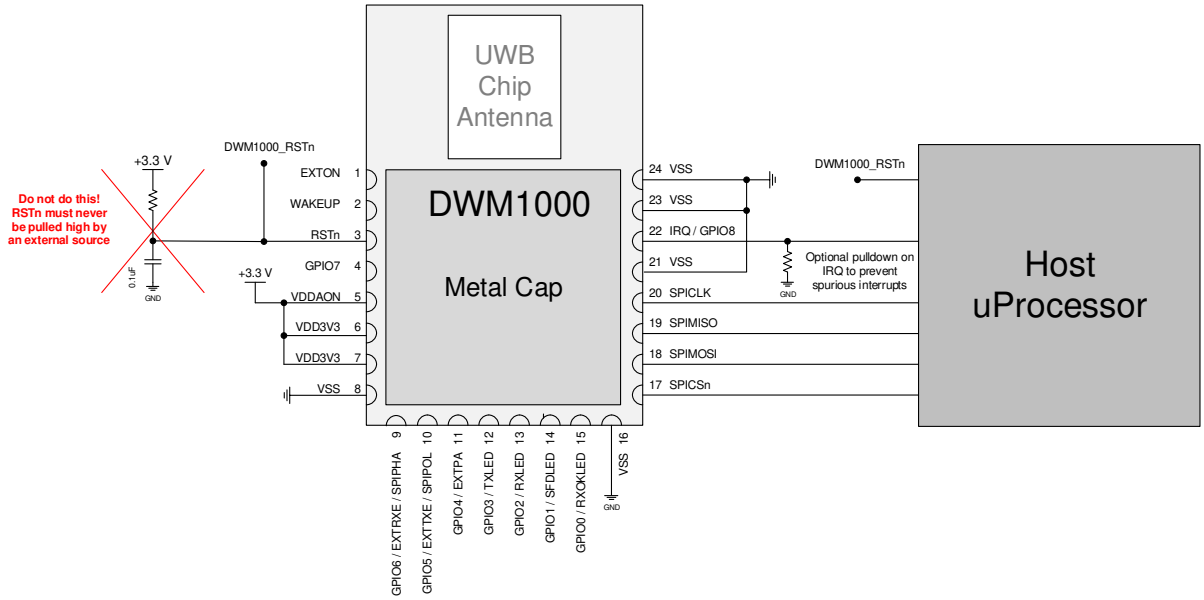


Figure 9: Example DWM1000 Application Circuit

5.2.1 SPI Bus

The SPI signal bus and mode configuration pins may need to be treated carefully if it is desirable to connect additional SPI devices to the SPI bus, or to configure the SPI for a non-default clock polarity of phase behaviour. Please see the DW1000 Datasheet [2] for a description of all SPI clock polarity and phase configurations, referred to as SPI modes.

The SPIMISO line may be connected to multiple slave SPI devices each of which is required to go open-drain when their respective SPICSn lines are de-asserted.

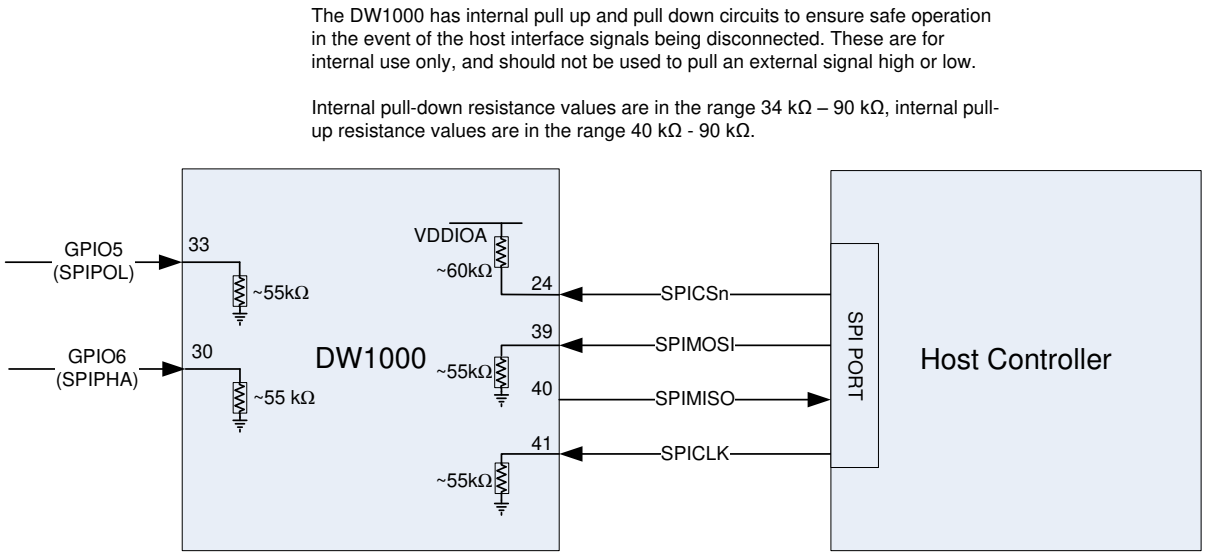


Figure 10: SPI Bus Connections

5.2.2 Configuring the SPI Mode

The SPI interface supports a number of different clock polarity and clock / data phase modes of operation. These modes are selected using GPIO5 & 6 as follows: -

Table 13: DW1000 SPI Mode Configuration

GPIO 5 (SPIPOL)	GPIO 6 (SPIPHA)	SPI Mode	Description (from the master / host point of view)
0	0	0	Data is sampled on the rising (first) edge of the clock and launched on the falling (second) edge.
0	1	1	Data is sampled on the falling (second) edge of the clock and launched on the rising (first) edge.
1	0	2	Data is sampled on the falling (first) edge of the clock and launched on the rising (second) edge.
1	1	3	Data is sampled on the rising (second) edge of the clock and launched on the falling (first) edge.
Note: The 0 on the GPIO pins can either be open circuit or a pull down to ground. The 1 on the GPIO pins is a pull up to VDDIO.			

GPIO 5 / 6 are sampled / latched on the rising edge of the RSTn pin to determine the SPI mode. They are internally pulled low to configure a default SPI mode 0 without the use of external components. If a mode other than 0 is required then they should be pulled up using an external resistor of value no greater than 10 kΩ to the VDDIO output supply.

If GPIO5 / 6 are also being used to control an external transmit / receive switch then external pull-up resistors of no less than 1 kΩ should be used so that the DW1000 can correctly drive these outputs in normal operation after the reset sequence / SPI configuration operation is complete.

The recommended range of resistance values to pull-up GPIO 5 / 6 is in the range of 1-10 kΩ. If it is required to pull-down GPIO 5 / 6, such as in the case where the signal is also pulled high at the input to an external IC, the resistor value chosen needs to take account of the DW1000 internal pull-down resistor values as well as those of any connected external pull-up resistors.

Refer to the DW1000 Data Sheet [2] and the DW1000 User Manual [3] for further details.

5.2.3 Powering down the DWM1000

The DWM1000 has a very low DEEPSLEEP current (typ. 200 nA – see Table 6). The recommended practise is to keep the DWM1000 powered up and use DEEPSLEEP mode when the device is inactive.

In situations where the DWM1000 must be power-cycled (the +3.3V supply in figure 10 turned off and then back on) it is important to note that when power is removed the supply voltage will decay towards 0V at a rate determined by the characteristics of the power source and the amount of decoupling capacitance in the system.

In this scenario, power should only be reapplied to the DWM1000 when: -

- VDDAON is above 2.3 V or:
- VDDAON has fallen below 100 mV

Reapplying power while VDDAON is between 100mV and 2.3V can lead to the DWM1000 powering up in an unknown state which can only be recovered by fully powering down the device until the voltage on VDDAON falls below 100 mV.

6 PACKAGE INFORMATION

6.1 Module Drawings

All measurements are given in millimetres.

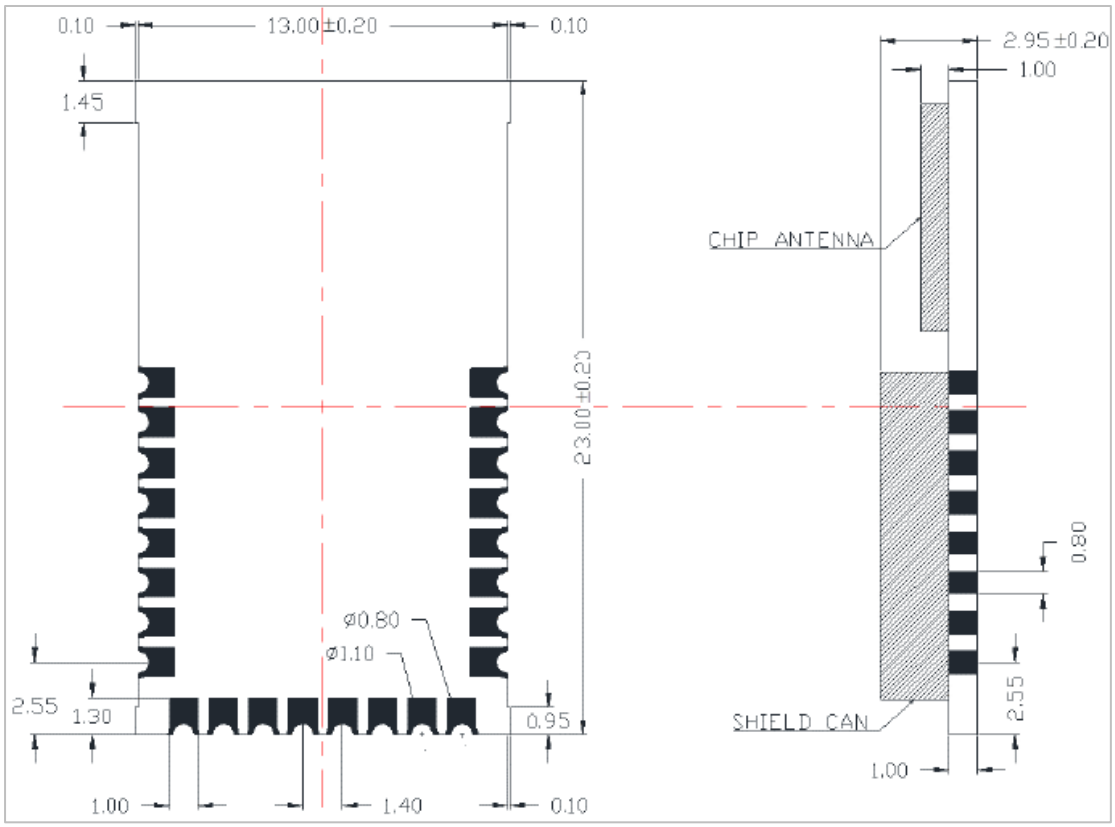


Figure 11: Module Package Size (units: mm)

6.2 Module Land Pattern

The diagram below shows the DWM1000 module land pattern.

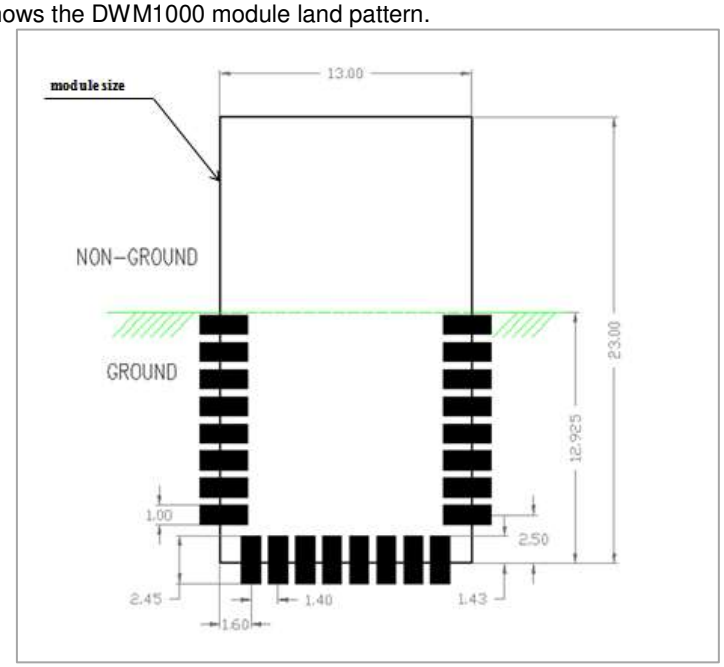
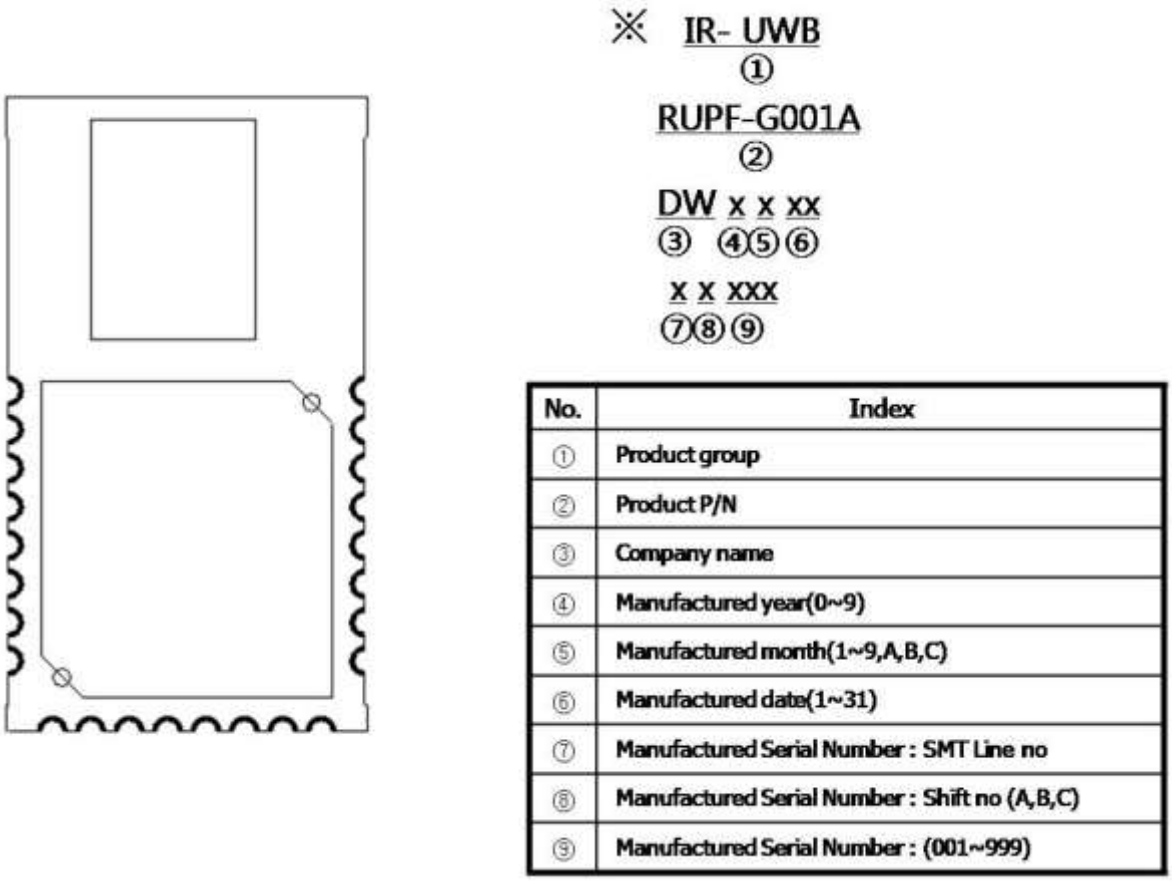


Figure 12: DWM1000 Module Land Pattern (units: mm)

Table 14: Module weight

Parameter	Min	Typ	Max	Units
Unit weight		1.4		g

6.3 Module Marking Information



No.	Index
①	Product group
②	Product P/N
③	Company name
④	Manufactured year(0~9)
⑤	Manufactured month(1~9,A,B,C)
⑥	Manufactured date(1~31)
⑦	Manufactured Serial Number : SMT Line no
⑧	Manufactured Serial Number : Shift no (A,B,C)
⑨	Manufactured Serial Number : (001~999)

Figure 13: DWM1000 Module Marking Information

6.4 Module Solder Profile

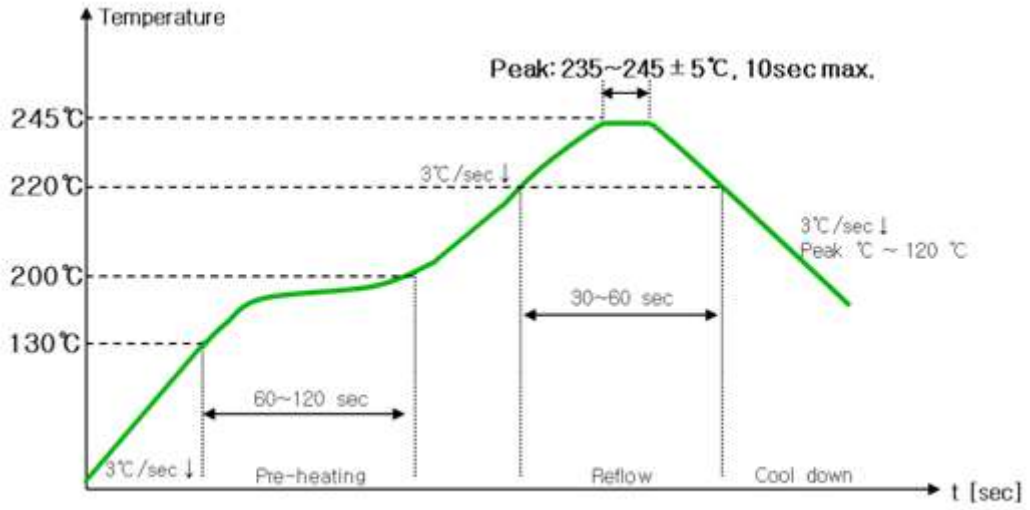
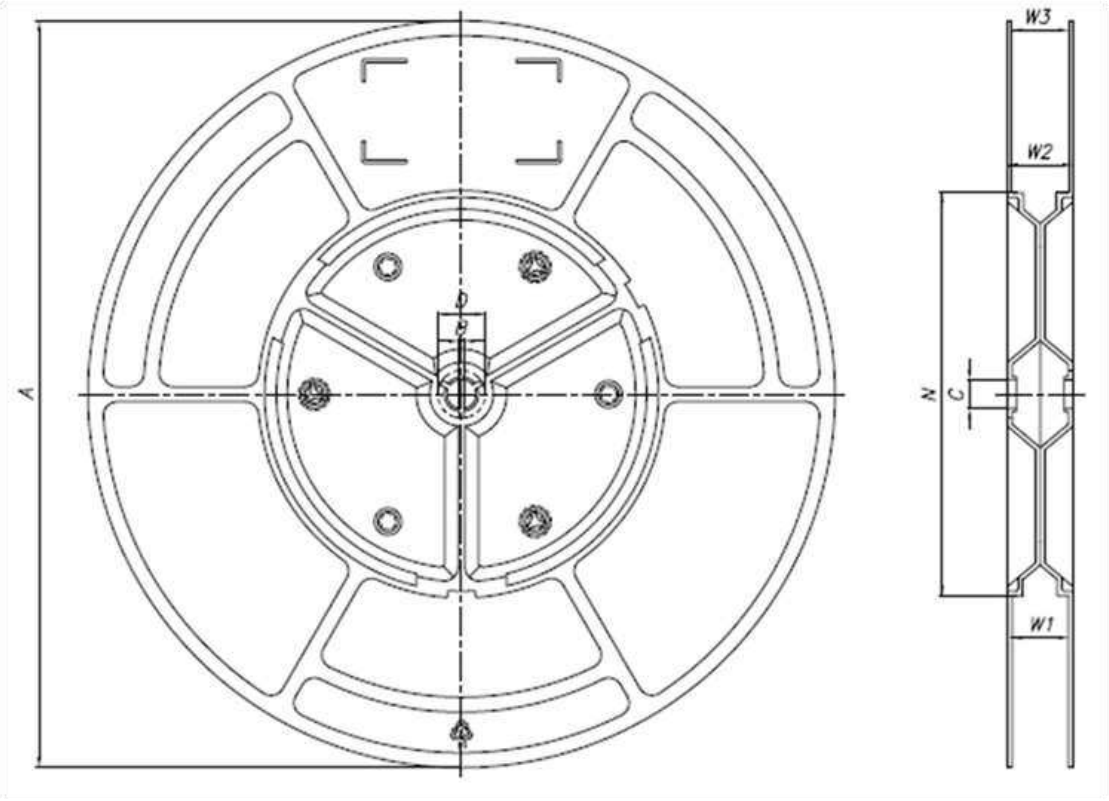


Figure 14: DWM1000 Module Solder Profile

7 ORDERING INFORMATION

7.1 Tape and Reel Information



ITEM	Length	Tolerence
A	330	±2
B	Min. 1.5	
C	13	±0.5
D	Min. 20.2	
W1	44.4	+3/-0
W2	48.4	±2
W3	45.65	±2

<Unit : mm>

Figure 15: Module Carrier Dimension (units: mm)

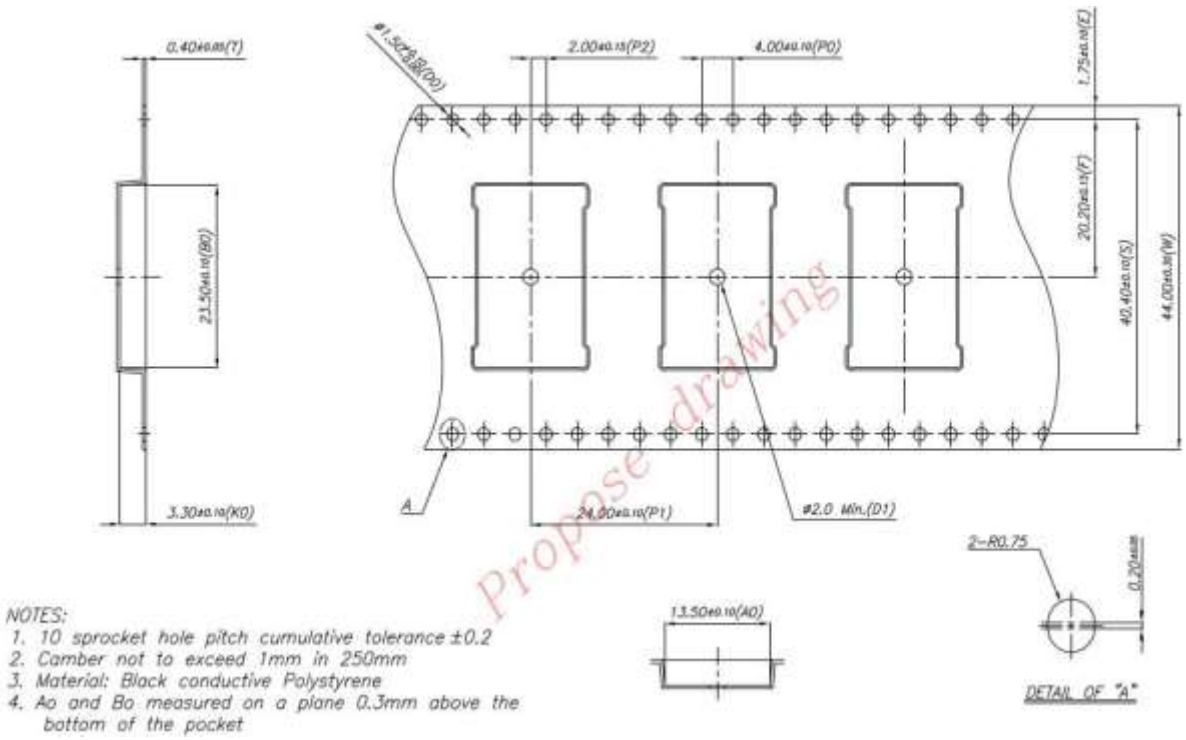


Figure 16: Module Tape Carrier Dimension (units: mm)

7.2 DWM1000 Packaging Information

7.2.1 Inner Box

Note 1) Recommendation: 72 hours floor time (30 degree C / 60 % RH)
Note 2) Recommendation: The time between opening and chip mount should be within 72 hours

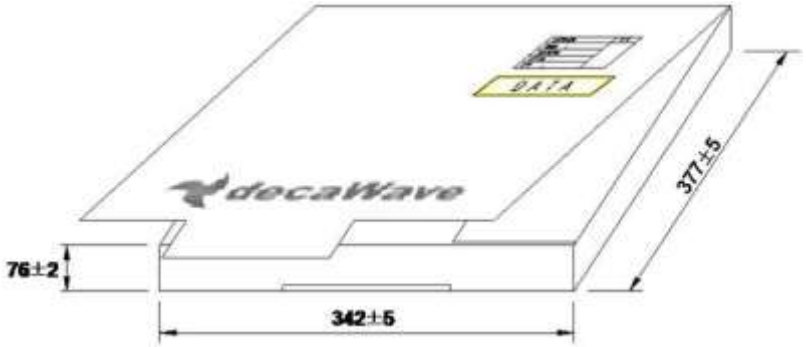


Figure 17: Module Inner Box (units: mm)

7.2.2 Outer Box

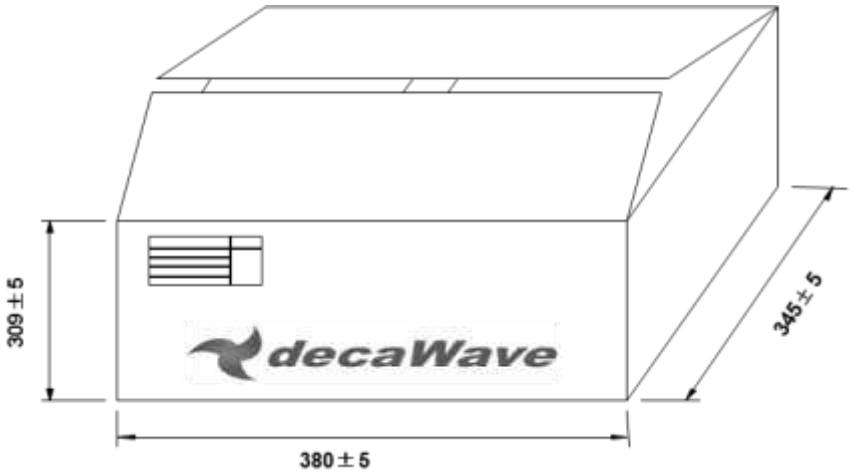


Figure 18: Module Outer Box: 4 Inner Box (Module Quantity – 2000 ea) (units: mm)