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AXEL LITE

Solo / Dual / Quad
ARM Cortex-A9 MPCore
CPU Module

LITE LINE

HARDWARE MANUAL

DAVE Embedded Systems www.dave.eu info@dave.eu

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1 Preface

1.1 About this manual

This Hardware Manual describes the **AXEL LITE** CPU module design and functions.
Precise specifications for the Freescale i.MX6 processor can be found in the CPU datasheets and/or reference manuals.

1.2 Copyrights/Trademarks

1.3 Standards

DAVE Embedded Systems is certified to ISO 9001 standards.

1.4 Disclaimers

DAVE Embedded Systems does not assume any responsibility about availability, supplying and support regarding all the products mentioned in this manual that are not strictly part of the **AXEL LITE** CPU module.
AXEL LITE CPU Modules are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. **DAVE Embedded Systems** customers who are using or selling these products for use in such applications do so at their own risk and agree to fully indemnify **DAVE Embedded Systems** for any damage resulting from such improper use or sale.

1.5 Warranty

AXEL LITE is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, **DAVE Embedded Systems** will at its discretion decide to repair

or replace defective products. Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed. The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.
DAVE Embedded Systems will not be responsible for any defects or damages to other products not supplied by **DAVE Embedded Systems** that are caused by a faulty **AXEL LITE** module.

1.6 Technical Support

We are committed to making our product easy to use and will help customers use our CPU modules in their systems. Technical support is delivered through email to our valued customers. Support requests can be sent to support-axel@dave.eu.
Software upgrades are available for download in the restricted access download area of **DAVE Embedded Systems** web site: http://www.dave.eu/reserved-area. An account is required to access this area and is provided to customers who purchase the development kit (please contact support-axel@dave.eu for account requests)..
Please refer to our Web site to http://www.dave.eu/products/axel-lite for the latest product documentation, utilities, drivers, Product Change Notifications, Board Support Packages, Application Notes, mechanical drawings and additional tools and software.

1.7 Related documents

Document	Location
DAVE Embedded Systems Developers Wiki	http://wiki.dave.eu/index.php/Main_Page
NXP i.MX 6Dual/6Quad Applications Processor Reference Manual	http://cache.freescale.com/files/32bit/doc/ref_manual/IMX6DQRM.pdf?fpsp=1&WT_TYPE=Reference%20Manuals&WT_VENDOR=FREESCALE&WT_FILE_FORMAT=pdf&WT_ASSET=Documentation

Tab. 1: Related documents

1.8 Conventions, Abbreviations, Acronyms

Abbreviation	Definition
i.MX 6 APRM	i.MX 6 Application Processor Reference Manual
IPU	Image Processing Unit
GPI	General purpose input
GPIO	General purpose input and output
GPO	General purpose output
PCB	Printed circuit board
RTC	Real time clock
SOM	System on module
TRM	Technical Reference Manual
XELK	Axel Embedded Linux Kit

Tab. 2: Abbreviations and acronyms used in this manual

Revision History

Version	Date	Notes
0.8.0	February 2014	First Draft
0.8.5	February 2014	First Revision
0.9.0	February 2014	First Release
0.9.1	May 2014	Minor fixes Added J7 pinout Completed Section 5 Added UART4 interface
0.9.2	August 2014	Fixed PGOOD signal description
0.9.3	November 2014	Minor fixes
0.9.4	October 2016	Minor fixes
0.9.5	October 2016	Minor fixes

2 Introduction

AXEL LITE is the new top-class Single - Dual - Quad Core ARM Cortex-A9 CPU module by DAVE Embedded Systems, based on the recent NXP i.MX6 application processor. Thanks to **AXEL LITE**, customers have the chance to save time and resources by using a compact solution that permits to reach scalable performances that perfectly fits the application requirements avoiding complexities on the carrier board. The use of this processor enables extensive system-level differentiation of new applications in many industry fields, where high-performance and extremely compact form factor (67,5 mm x 43 mm) are key factors. Smarter system designs are made possible, following the trends in functionalities and interfaces of the new, state-of-the-art embedded products.

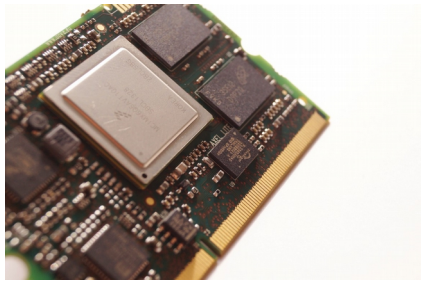


Fig. 1: AXEL-LITE- Powered by I.MX6 processor

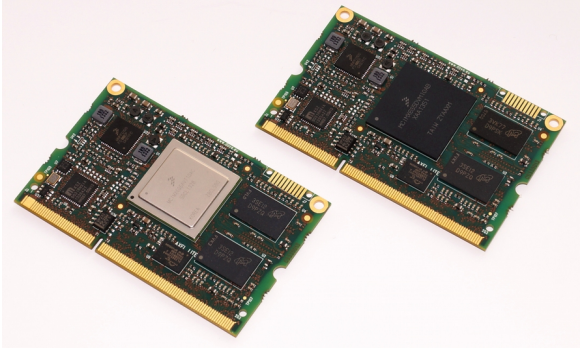


Fig. 2: AXEL-LITE – Solo / Dual / Quad core ARM Cortex A9

AXEL LITE enables designers to create smart products suitable for harsh mechanical and thermal environments, allowing the development of high computing and reliable solutions. Thanks to the tight integration between the ARM Core-based processing system, designers are able to share the application through the multi-core platform and/or to divide the task on different cores in order to match with specific application requirements (thanks to AMP is possible to create application where RTOS and Linux works together on different cores). **AXEL LITE** is designed in order to keep full compatibility

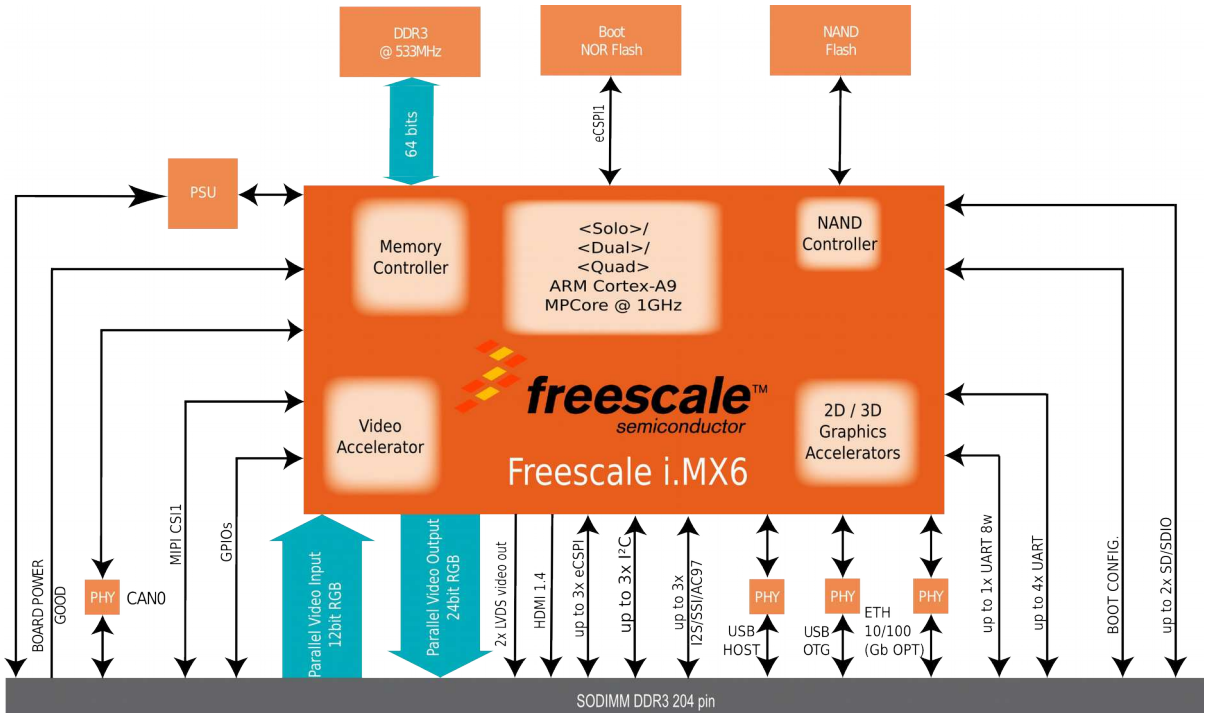
with the **LITE Line** CPU modules where quality and reliability are important factors.

2.1 Product Highlights

- Unmatched performances thanks to Solo / Dual / Quad Core @ 1.2 GHz
- All memories you need on-board
- Boot from NOR for safe applications
- Enabling massive computing applications thanks to wide range DDR3 RAM memory up to 2GB
- Single 3V3 Power Supply
- Reduced carrier complexity: SDIO, dual CAN, USB, Ethernet with on-board PHY, GPIOs
- Multiple video outputs available
- H264 Video encoding and decoding
- Multiple video inputs available

Fig. 3: AXEL LITE SOM (top view)

2.2 Block Diagram



2.3 Feature Summary

Feature	Specifications	Options
CPU	NXP i.MX6 S/D/Q ARM Cortex A9 MPCore @ 1.2 GHz	
Cache	L1: 32Kbyte instruction, 32Kbyte data L2: Unified data/instruction, 1 MByte	
RAM	Default: up to 2GB DDR3 (for 4GB support please contact our sales department) x64 data bus width @ 533 MHz	
Storage	Bootable SPI NOR 16, 32, 64 MB Flash NAND: all sizes, on request	
Expansion bus	One PCI Express 2.0 lane with integrated PHY (5.0 GT/s Endpoint/Root Complex operations)	

Tab. 3: CPU, Memories, Busses

Feature	Specifications	Options
Graphics Controller	16-/24-bit HD Display Port 1x HDMI 1.4 channel + DDC 1x TFT/RGB output port 2x LVDS output ports	
2D/3D Engines	GPU2D cores for raster (R2D, Vivante GC320) and vector (V2D, Vivante GC355) graphics acceleration GPU3D core (Vivante GC2000) for OpenGL/OpenGL ES/OpenVG/OpenCL API acceleration	
Video capture	1x RGB Parallel port 12 bit 1x MIPI CSI port	
Video processing	High performance, multi-standard VPU Up to 1080p60 H264 decode Up to 1080p30 H264 encode	
Coprocessors	Media Processing Engine with NEON™ & VFPv3-D32 Floating-Point Unit	
USB	1x 2.0 OTG port (PHY on board) 1x 2.0 Host port (PHY on board)	
UARTs	5x UART ports (up to 1x full, up to 4x four-wires)	
GPIO	Available lines, shared with other functions	

Feature	Specifications	Options
	(interrupts available)	
Networks	Default: Fast Ethernet 10/100 Mbps with integrated PHY (for Gigabit support please contact our sales department)	
CAN	2x CAN 2.0B ports (1x with integrated PHY)	
SD/MMC	up to 3x SD 3.0 /SDIO 3.0/MMC 4.x compliant controllers	
Serial buses	5x full-duplex SPI ports with four peripheral chip selects 3x master and slave I²C interfaces	
Audio	up to 3x I²S / SSI / AC97	
Timers	Enhanced Periodic Interrupt Timer General Purpose Timer	
Debug	JTAG IEEE 1149.1 Test Access Port CoreSight™ and Program Trace Macrocell (PTM)	

Tab. 4: Peripherals

Feature	Specifications	Options
Supply Voltage	Single 3.3V input, voltage regulation on board	
Active power consumption	See section 8.3 - Power consumption	
Dimensions	67.5mm x 43mm	
Operating temperature range	Commercial: 0°C / +70°C Industrial: -40°C / +85°C	
Connectors	SODIMM 204 pins	

Tab. 5: Electrical, Mechanical and Environmental Specifications

3 Design overview

The heart of **AXEL LITE** module is composed by the following components:

- NXP i.MX6 Solo / Dual / Quad core SoC application processor
- Power supply unit
- DDR memory banks
- NOR and NAND flash banks
- 1x 204 pin SODIMM connector with interfaces signals

This chapter shortly describes the main **AXEL LITE** components.

3.1 Freescale i.MX6 application processor

The i.MX6 Solo/Dual/Quad processors feature NXP's advanced implementation of the ARM® Cortex®-A9 MPCore, which operates at speeds up to 1.2 GHz. They include 2D and 3D graphics processors, 1080p video processing, and integrated power management. As a result, the i.MX6 devices are able to serve a wide range of applications including:

- Automotive driver assistance, driver information, and infotainment
- Multimedia-centric smart mobile devices
- Instrument clusters, and portable medical devices.
- E-Readers, smartbooks, tablets
- Intelligent industrial motor control, industrial networking, and machine vision
- IP and Smart camera
- Human-machine interfaces
- Medical diagnostics and imaging
- Digital signage

- Video and night vision equipment
- Multimedia-focused products
- Entertainment and gaming appliances

The i.MX6 application processor is composed of the following major functional blocks:

- ARM Cortex-A9 MPCore 2x/4x CPU Processor, featuring:
  - 1 Megabyte unified L2 cache shared by all CPU cores
  - NEON MPE co-processor
  - General Interrupt Controller (GIC) with 128 interrupt support
  - Snoop Control Unit (SCU)
  - External memories interconnect
- Hardware accelerators, including:
  - VPU -Video Processing Unit
  - Two IPUv3H -Image Processing Unit (version 3H)
  - 2D/3D/Vector graphics accelerators
- Connectivity peripherals, including
  - PCIe
  - SATA
  - SD/SDIO/MMC
  - Serial buses: USB, UART, I²C, SPI, ...

AXEL LITE can mount three versions of the i.MX6 processor. The following table shows a **comparison** between the processor models, highlighting the differences:

Processor	# cores	Clock	L2 cache	DDR3	Graphics acceleration	IPU	VPU	SATA-II
i.MX6 Solo	1	800 MHz 1 GHz	512 KB	32 bit @ 400 MHz	*3D*: Vivante GC880 *2D*: Vivante GC320 *Vector*: N.A.	1x	1x	N.A.
i.MX6 Dual	2	850 MHz 1 GHz 1.2 GHz	1 MB	64 bit @ 533 MHz	*3D*: Vivante GC2000 *2D*: Vivante GC320 *Vector*: Vivante GC335	2x	2x	Yes
i.MX6 Quad	4	850 MHz 1 GHz 1.2 GHz	1MB	64 bit @ 533 MHz	*3D*: Vivante GC2000 *2D*: Vivante GC320 *Vector*: Vivante GC335	2x	2x	Yes

Tab. 6: i.MX6 comparison

3.2 DDR3 memory bank

DDR3 SDRAM memory bank is composed by 4x 16-bit width chips resulting in a 64-bit combined width bank.
The following table reports the SDRAM specifications:

CPU connection	Multi-mode DDR controller (MMDC)
Size min	512 MB
Size max	2 GB (for 4GB support please contact our sales department)
Width	64 bit
Speed	533 MHz

Tab. 7: DDR3 specifications

3.3 NOR flash bank

NOR flash is a Serial Peripheral Interface (SPI) device. This device is connected to the eCSPI channel 1. Specific models of the **AXEL LITE** SOM provide the SPI NOR as boot memory.

The following table reports the NOR flash specifications:

CPU connection	eCSPI channel 1

Size min	16 MByte
Size max	64 MByte
Chip select	ECSPI1_SS0
Bootable	Yes

Tab. 8: NOR flash specifications

For **AXEL LITE** models that have the NOR flash bank populated, the eCSPI channel 1 is mapped by design on the following multiplexed pins:

NOR signal	Function	I.MX6 signal	I.MX6 ball #
NOR_CS0n	Chip select	EIM_EB2	E22
NOR_DQ0/MOSI	Serial Input	EIM_D18	D24
NOR_DQ1/MISO	Serial Output	EIM_D17	F21
NOR_SCLQ	Serial clock	EIM_D16	C25

Tab. 9: eCSPI1 pin mapping

3.4 NAND flash bank

On board main storage memory is a 8-bit wide NAND flash connected to the CPU's Raw NAND flash controller. Optionally, it can act as boot peripheral.
The following table reports the NAND flash specifications:

CPU connection	Raw NAND flash controller
Page size	512 byte, 2 kbyte or 4 kbyte
Size min	128 MByte
Size max	2 GByte
Width	8 bit
Chip select	NANDF_CS0
Bootable	Yes

Tab. 10: NAND flash specifications

3.5 Memory Map

For detailed information, please refer to chapter 2 “Memory Maps” of the i.MX Applications Processor Reference Manual.

3.6 Power supply unit

AXEL LITE, as the other **LITE Line** CPU modules, embeds all the elements required for powering the unit, therefore power sequencing is self-contained and simplified. Nevertheless, power must be provided from carrier board, and therefore users should be aware of the ranges power supply can assume as well as all other parameters. For detailed information, please refer to Section 5.1 Power Supply Unit (PSU) and recommended power-up sequence.

3.7 CPU module connectors

All interface signals **AXEL LITE** provides are routed through SODIMM DDR3 204 pin (named J2). The dedicated carrier board must mount the mating connector and connect the desired peripheral interfaces according to **AXEL LITE** pinout specifications.

For mechanical information, please refer to Section 4 (Mechanical specifications). For pinout and peripherals information, please refer to Sections 6 (Pinout table) and 7 (Peripheral interfaces).

4 Mechanical specifications

This chapter describes the mechanical characteristics of the **AXEL LITE** module.

> *Mechanical drawings are available in DXF format from the Axel page on DAVE Embedded Systems website (http://www.dave.eu/products/axel-lite)*

4.1 Board Layout

The following figure shows the physical dimensions of the **AXEL LITE** module:

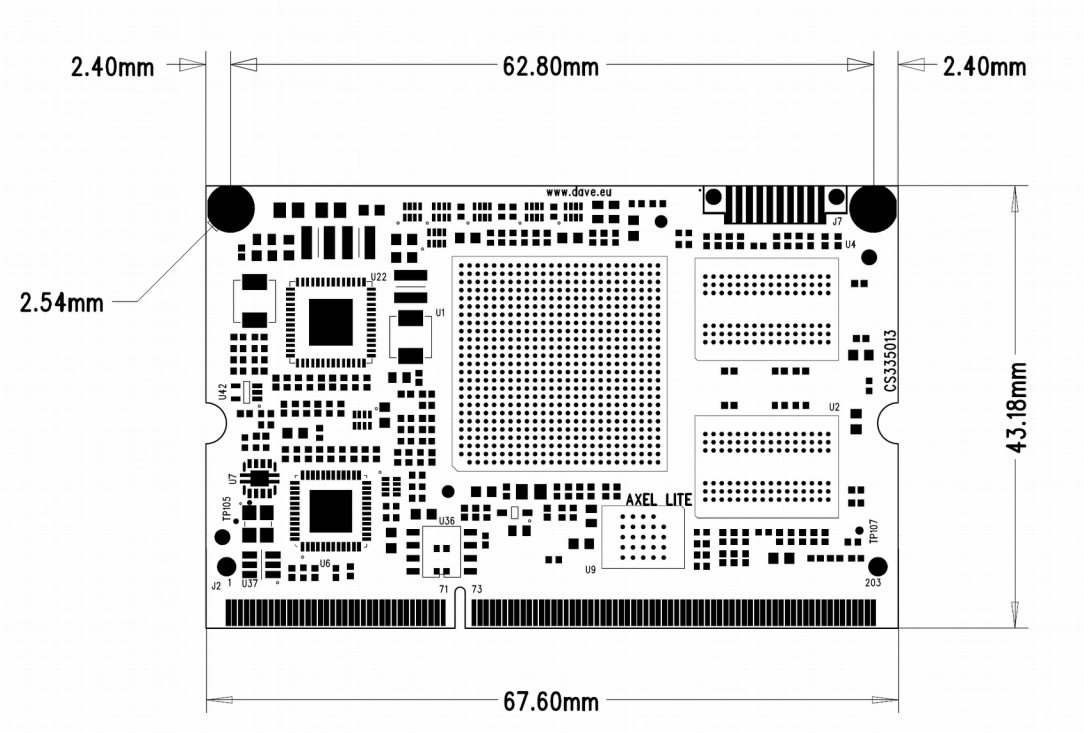


Fig. 4: Board layout - Top view

- Board width: 43.18 mm

- Board height: 67.6 mm
- Maximum components height is 3.4 mm
- PCB thickness is 1.0 mm

4.2 Connectors

The following figure shows the **AXEL LITE** connectors layout:

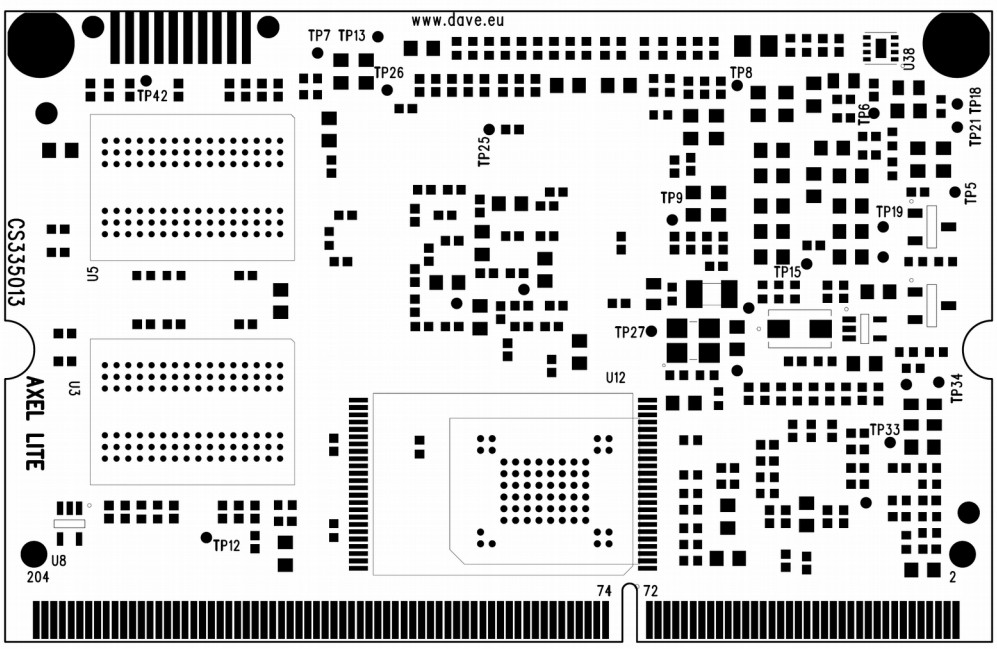


Fig. 5: Board layout - Bottom view

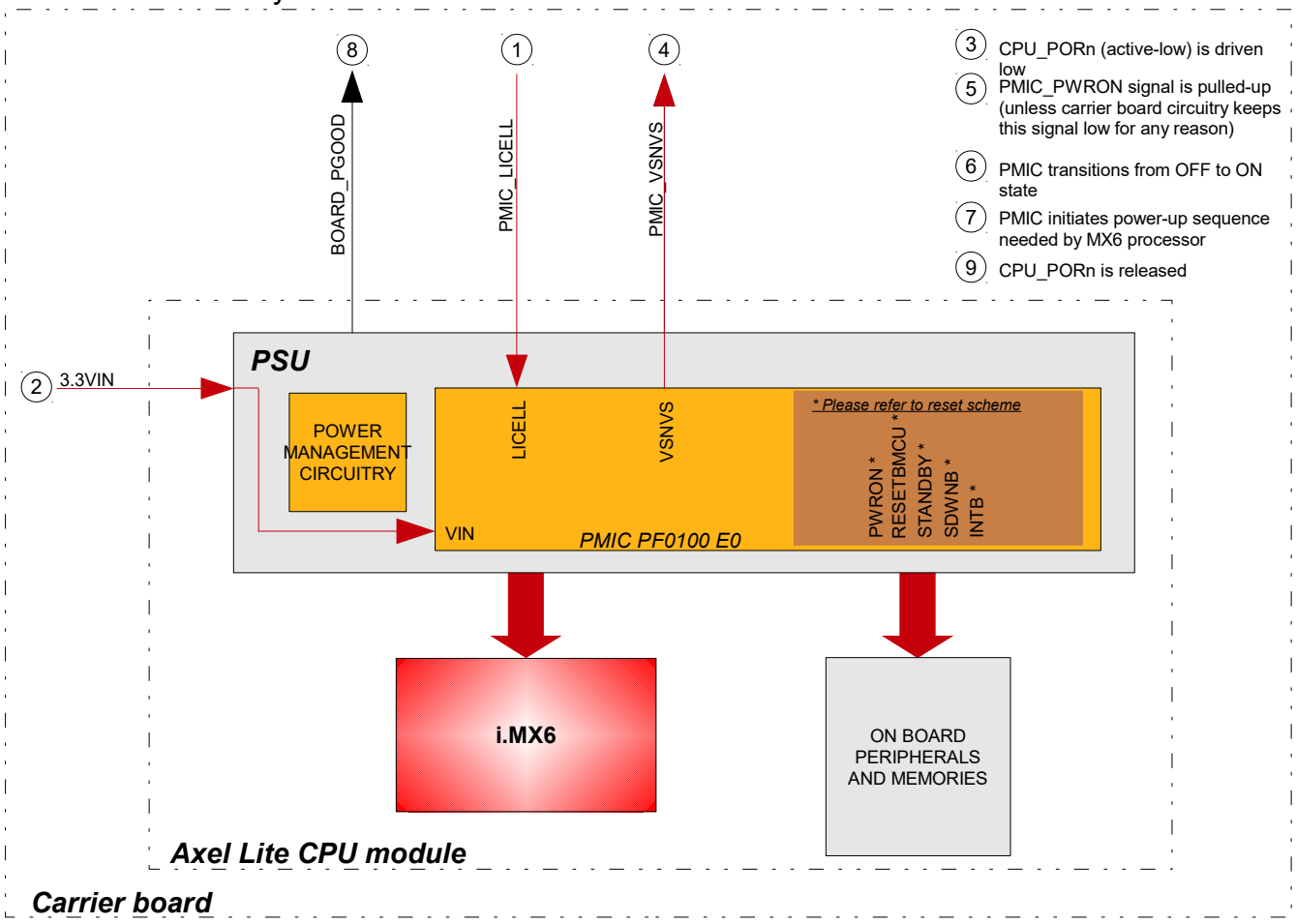
The following table reports connectors specifications:

Part number	Standard SO-DIMM 204-pin (DDR3)
Mating connectors	DDR3 SO-DIMM SOCKET Part number : TE Connectivity 2013289-1

5 Power, reset and control

5.1 Power Supply Unit (PSU) and recommended power-up sequence

Implementing correct power-up sequence for i.MX6 processors is not a trivial task because several power rails are involved. **AXEL LITE** SOM simplifies this task by embedding all the required circuitry. The following picture shows a simplified block diagram of PSU/voltage monitoring circuitry:



The PSU is composed of two main blocks:

- power management integrated circuit (PMIC, NXP PF0100E0 - on request this part is available in automotive grade)
- additional generic power management circuitry that completes PMIC functionalities.

The PSU:

- generates the proper power-up sequence required by i.MX processor and surrounding memories and peripherals
- synchronizes the powering up of carrier board in order to prevent back power
- provides some spare regulated voltages that can be used to power carrier board devices

5.1.1 Power-up sequence

The typical power-up sequence is the following:

1. (optional) PMIC_LICELL is powered
2. 3.3VIN main power supply rail is powered
3. CPU_PORn (active-low) is driven low
4. PMIC activates PMIC_VSNVS power output
5. PMIC_PWRON signal is pulled-up (unless carrier board circuitry keeps this signal low for any reason)
6. PMIC transitions from OFF to ON state
7. PMIC initiates power-up sequence needed by MX6 processor
8. BOARD_PGOOD signal is raised; this active-high signal indicates that SoM's I/O is powered. This signal can be used to manage carrier board power up sequence in order to prevent back powering (from SoM to carrier board or vice versa)
9. CPU_PORn is released.

5.1.2 Power rails and related signals

The following list describes in detail power rails and power related signals. **Please note that PMIC regulators output voltages can be changed only if explicitly allowed.**

- 3.3VIN: this is external main power rail. Voltage range is 3.3V ±5%
- PMIC_CELL: PMIC's coin cell supply input/output
- BOARD_PGOOD: this output signal is used to indicate when carrier board's circuitry interfacing **AXEL LITE**'s I/Os has to be powered up

For further details, please refer to the PMIC documentation: *http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MMPF0100%7CPF0100*