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TDA7512F

FM car-radio tuner IC with intelligent selectivity system (ISS)

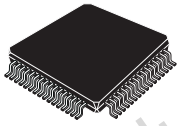
Features

FM part

- RF AGC generation by RF and IF detection
- I/Q mixer for 1st FM IF 10.7 MHz with image rejection
- 2 programmable IF-gain stages
- Mixer for 2nd IF 450 kHz
- Internal 450 kHz bandpass filter with three bandwidths controlled by ISS
- Fully integrated FM-demodulator with noise cancellation

Additional features

- VCO for world tuning range
- High performance fast PLL for RDS-system
- IF counter with search stop signal
- Quality detector for level, deviation, adjacent channel and multipath
- Quality detection informations as analog signals external available
- ISS (intelligent selectivity system) for cancellation of adjacent channel and noise influences



LQFP64

- Adjacent channel mute
- Fully electronic alignment
- All functions I^2C bus controlled

Description

The TDA7512F is a high performance tuner circuit for FM car-radio. It contains mixer, IF amplifier, demodulator, quality detection, ISS filter and PLL synthesizer with IF counter on a single chip. Use of BiCMOS technology allows the implementation of several tuning functions and a minimum of external components.

Table 1. Device summary

Order code	Package	Packing
E-TDA7512F	LQFP64	Tray
E-TDA7512FTR	LQFP64	Tape and reel

Contents

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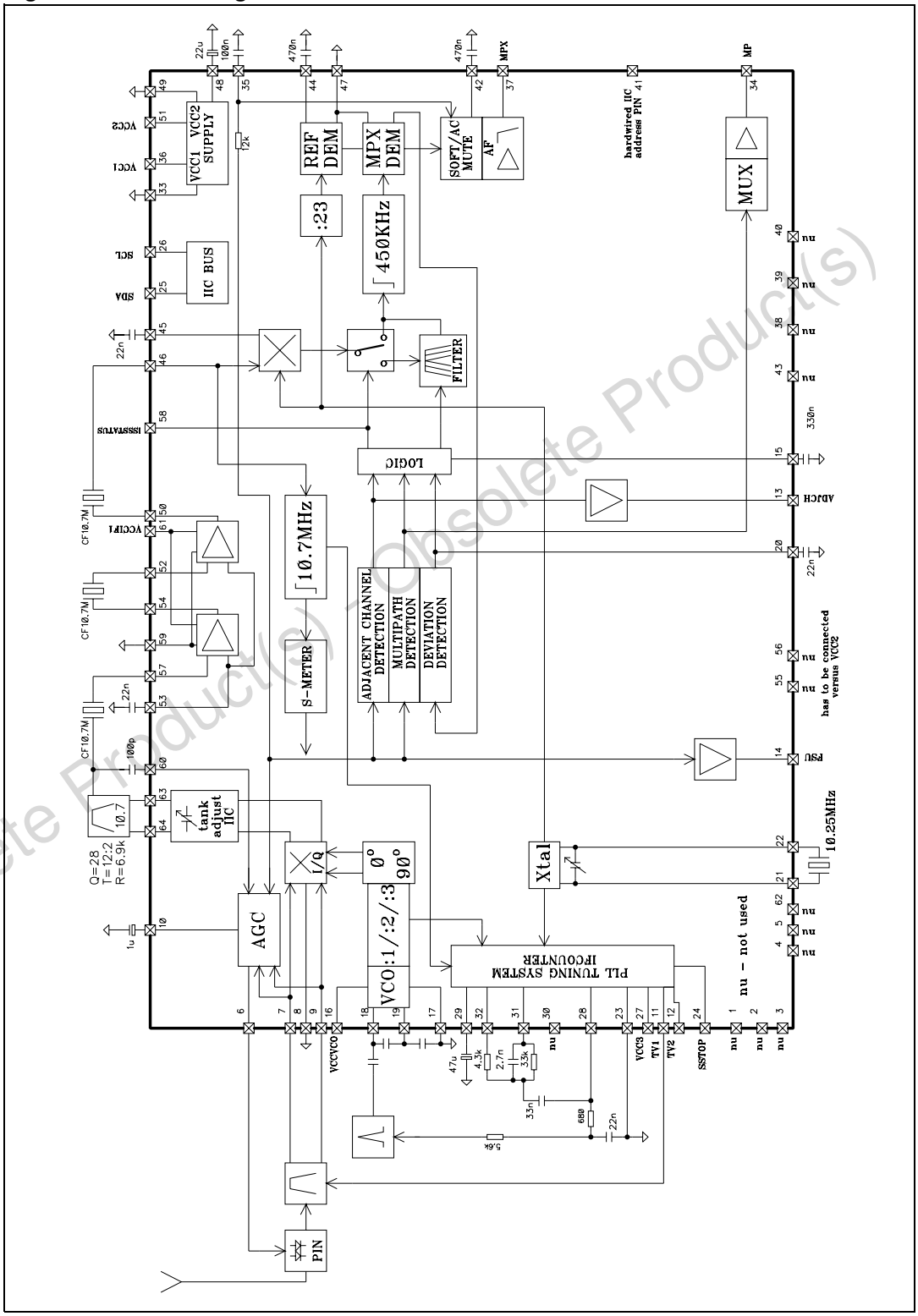
1 Block diagram

Figure 1. Block Diagram



2 Pin description

Figure 2. Pin connection (top view)

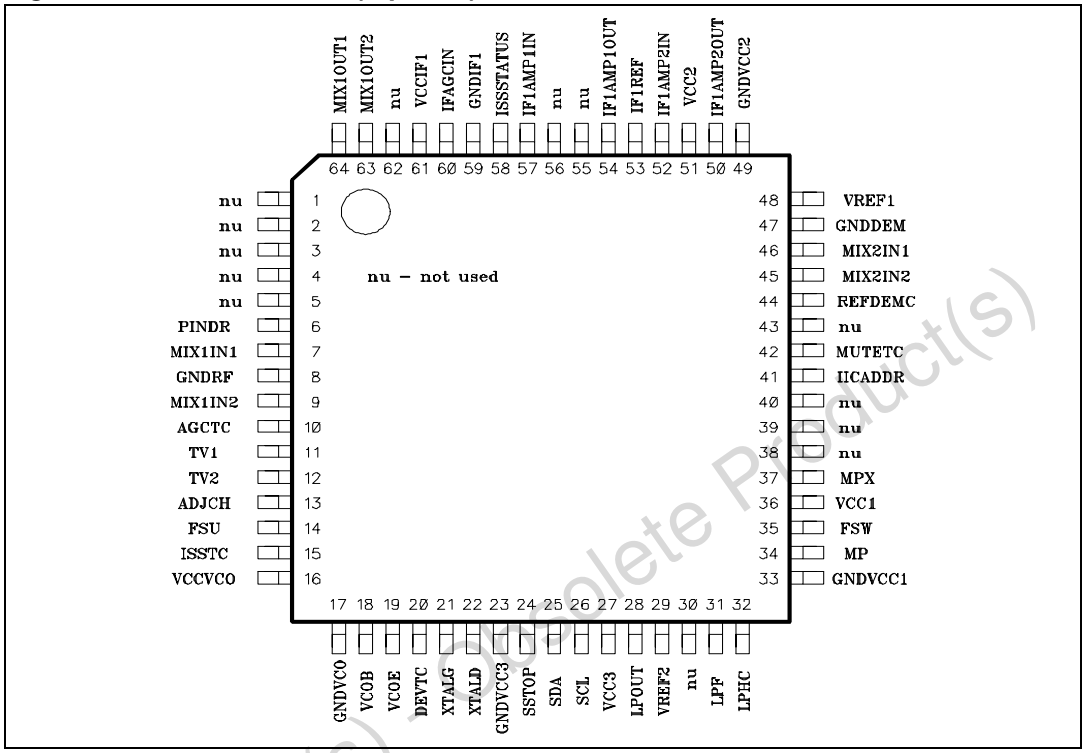


Table 2. Pin description

Pin #	Pin name	Function
1	nu	not used - to be left open
2	nu	not used - to be left open
3	nu	not used - to be left open
4	nu	not used - to be left open
5	nu	not used - to be left open
6	PINDR	PIN Diode Driver Output
7	MIX1IN1	Input1 Mixer1
8	GNDRF	RF Ground
9	MIX1IN2	Input2 Mixer1
10	AGCTC	AGC Time Constant
11	TV1	Tuning Voltage Preselection1
12	TV2	Tuning Voltage Preselection2
13	ADJCH	Ident. Adjacent Channel Output
14	FSU	Unweighted Fieldstrength Output
15	ISSTC	Time Constant for ISS Filter Switch

Table 2. Pin description (continued)

Pin #	Pin name	Function
16	VCCVCO	VCO Supply
17	GNDVCO	VCO Ground
18	VCOB	VCO Input Base
19	VCOE	VCO Output Emitter
20	DEVTC	Deviation Detector Time Constant
21	XTALG	Xtal Oscillator to MOS Gate
22	XTALD	Xtal Oscillator to MOS Drain
23	GNDVCC3	VCC3 Ground
24	SSTOP	Search Stop Output
25	SDA	I^2C-Bus Data
26	SCL	I^2C-Bus Clock
27	VCC3	Supply Tuning Voltage
28	LPOUT	Op Amp Output to PLL Loop Filters
29	VREF2	Voltage Reference for PLL Op Amp
30	nu	not used - to be left open
31	LPF	Op Amp Input to PLL Loop Filter
32	LPHC	High Current PLL Loop Filter Input
33	GNDVCC1	Digital Ground
34	MP	Ident. Multipath Output
35	FSW	Weighted Fieldstrength Output
36	VCC1	Digital Supply
37	MPX	MPX Output
38	nu	not used - to be left open
39	nu	not used - to be left open
40	nu	not used - to be left open
41	IICADDR	Hardwired IIC-Address PIN
42	MUTETC	Softmute Time Constant
43	nu	not used - to be left open
44	REFDEMC	Demodulator Reference
45	MIX2IN2	MIX2 Input1
46	MIX2IN1	MIX2 Input2
47	GNDDEM	Ground Demodulator
48	VREF1	Reference 5V
49	GNDVCC2	Analog Ground
50	IF1AMP2OUT	IF1 Amplifier2 Output

Table 2. Pin description (continued)

Pin #	Pin name	Function
51	VCC2	Analog Supply
52	IF1AMP2IN	IF1 Amplifier2 Input
53	IF1REF	IF1 Amplifier Reference
54	IF1AMP1OUT	IF1 Amplifier1 Output
55	nc	not used - has to be connected versus VCC2
56	nc	not used - has to be connected versus VCC2
57	IF1AMP1IN	IF1 Amplifier1 Input
58	ISSSTATUS	ISS Filter Status
59	GNDIF1	IF1 Ground
60	IFAGCIN	IF AGC Input
61	VCCIF1	IF1 Supply
62	nu	not used - to be left open
63	MIX1OUT2	MIX Tank 10.7MHz
64	MIX1OUT1	MIX Tank 10.7MHz

3 Electrical specifications

3.1 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j\text{-}amb)}$	Thermal resistance junction-to-ambient	68 max.	°C/W

3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Supply voltage	10.5	V
T_{amb}	Ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature	-55 to +150	°C

3.3 Electrical characteristics

T_{amb} = +25 °C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1} = V_{CCIF1}$ = 8.5 V, f_{RF} = 98 MHz, dev. = 40 kHz, f_{MOD} = 1 kHz, f_{IF1} = 10.7 MHz, f_{IF2} = 450 kHz, f_{Xtal} = 10.25 MHz, in application circuit, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply						
V_{CC1}	Digital supply voltage	-	7.5	8.5	10	V
V_{CC2}	Analog supply voltage	-	7.5	8.5	10	V
V_{CC3}	Analog tuning voltage	-	7.5	8.5	10	V
V_{CCVCO}	VCO supply voltage	-	7.5	8.5	10	V
V_{CCMIX1}	MIX1 supply voltage	-	7.5	8.5	10	V
V_{CCIF1}	IF1 supply voltage	-	7.5	8.5	10	V
I_{CC1}	Supply current	-	-	7.5	-	mA
I_{CC2}	Supply current	VCO:3	-	70	-	mA
I_{CC3}	Supply current	-	-	2	-	mA
I_{CCVCO}	Supply current	-	-	9	-	mA
I_{CCMIX1}	Supply current	-	-	8	-	mA
I_{CCIF1}	Supply current	-	-	6	-	mA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Reference voltages						
V_{REF1}	Internal reference voltage	I_{REF1} = 0 mA	-	5	-	V
V_{REF2}	Internal reference voltage	I_{REF2} = 0 mA	-	2.5	-	V
Wide band RF AGC						
V_{7-9}	Lower threshold start	V_{10} = 2.5 V	-	85	-	dBµV
V_{7-9}	Upper threshold start	V_{10} = 2.5 V	-	96	-	dBµV
Narrow band IF & keying AGC						
V_{60}	Lower threshold start	KAGC = off, V_{7-9} = 0 mV_{RMS}	-	86	-	dBµV
V_{60}	Upper threshold start	KAGC = off, V_{7-9} = 0 mV_{RMS}	-	98	-	dBµV
V_{60}	Lower threshold start with KAGC	KAGC = max, V_{7-9} = 0 mV_{RMS}, Δf_{IF} = 300 kHz	-	98	-	dBµV
V_{35}	Start point KAGC	KAGC = max, V_{7-9} = 0 mV_{RMS}, Δf_{IF} = 300 kHz f_{IF1} generate FSW level at V_{35}	-	3.6	-	V
D	Control range KAGC	ΔV_{35}= +0.4 V	-	16	-	dB
R_{IN}	Input resistance	-	-	10	-	kΩ
C_{IN}	Input capacitance	-	-	2.5	-	pF
AGC time constant output						
V_{10}	Max. AGC output voltage	V_{7-9} = 0 mV_{RMS}	-		V_{REF1} +V_{BE}	V
V_{10}	Min. AGC output voltage	V_{7-9} = 50 mV_{RMS}	-		0.5	V
I_{10}	Min. AGC charge current	V_{7-9} = 0 mV_{RMS},; V_{10} = 2.5 V	-	-12.5	-	µA
I_{10}	Max. AGC discharge current	V_{7-9} = 50 mV_{RMS},; V_{10} = 2.5 V	-	1.25	-	mA
AGC pin diode driver output						
I_6	AGC OUT, current min.	V_{7-9} = 0 mV_{RMS}, V_6 = 2.5 V	-	50	-	µA
I_6	AGC OUT, current max.	V_{7-9} = 50 mV_{RMS}, V_6 = 2.5 V	-	-20	-	mA
I/Q mixer 1 (10.7MHz)						
R_{IN}	Input resistance	differential	-	10	-	kΩ
C_{IN}	Input capacitance	differential	-	4	-	pF
R_{OUT}	Output resistance	differential	100		-	kΩ
$V_{7,9}$	Input dc bias	-	-	3.2	-	V
g_m	Conversion transconductance	-	-	17	-	mS
F	Noise figure	400 Ω generator resistance	-	3	-	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
CP_{1dB}	1dB compression point	referred to diff. mixer input	-	100	-	dBµV
IIP3	3rd order intermodulation	-	-	122	-	dBµV
IQG	I/Q gain adjust	G	-1	-	+1	%
IQP	I/Q phase adjust	PH	-7	-	+8	DEG
IRR	Image rejection ratio	ratio wanted/image	30	40	-	dB
IRR	Image rejection ratio	with gain and phase adjust	40	46	-	dB
IF1 Amplifier1,2 (10.7 MHz)						
$G1_{min}$	Min. gain	IFG, referred to 330 Ω	-	9	-	dB
$G1_{max}$	Max. gain	IFG, referred to 330 Ω	-	15	-	dB
$G2_{min}$	Min. gain	IFG, referred to 330 Ω	-	9	-	dB
$G2_{max}$	Max. gain	IFG, referred to 330 Ω	-	11	-	dB
R_{IN}	Input resistance	-	-	330	-	Ω
R_{OUT}	Output resistance	-	-	330	-	Ω
CP_{1dB}	1dB compression point	referred to 330 Ω input	-	105	-	dBµV
IIP3	3rd order Intermodulation	referred to 330 Ω input	-	126	-	dBµV
Mixer 2 (450 kHz)						
R_{IN}	Input impedance	-	-	330	-	W
V_{46}	Max. input voltage	-	-	900	-	mV_{RMS}
V_{48}	Limiting sensitivity	S/N = 20dB	-	25	-	µV
G	Mixer gain	-	-	18	-	dB
Limiter 1 (450 kHz)						
$G_{Limiter}$	Gain	-	-	80	-	dB
Demodulator, audio output						
THD	Total harmonic distortion	Dev.= 75 kHz, V_{46} = 10 mV_{RMS}	-	-	0.1	%
V_{MPX}	MPX output signal	Dev.= 75 kHz	-	500	-	mV_{RMS}
R_{OUT}	Output resistance	-	-	50	-	Ω
$\|\Delta V\|_{min}$	DC offset fine adjust	DEM, MENA = 1	-	8.5	-	mV
$\|\Delta V\|_{max}$	DC offset fine adjust	DEM, MENA = 1	-	264	-	mV
S/N	Signal to noise	Dev.= 40 kHz,V_{46} = 10 mV_{RMS}	-	76	-	dB
Quality detection						
S-meter, unweighted fieldstrength						
V_{46}	Min. input voltage MIX2	-	-	10	-	µV
V_{14}	Fieldstrength output	V_{46} = 0 V_{RMS}	-	0.1	-	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{14}	Fieldstrength output	V_{46} = 1 V_{RMS}	-	4.9	-	V
ΔV_{14}	voltage per decade	SMSL = 0	-	1	-	V
ΔV_{14}	voltage per decade	SMSL = 1	-	1.5	-	V
ΔV_{14}	S-meter offset	SL, SMSL=1	-15		15	dB
R_{OUT}	Output resistance	-	-	200	-	W
TK	Temp coeff.	-	-	0	-	ppm/K
S-meter, weighted fieldstrength						
V_{35}	Fieldstrength output	V_{46} = 0 V_{RMS}	-	2.5	-	V
V_{35}	Fieldstrength output	V_{46} = 1 V_{RMS}	-	4.9	-	V
R_{OUT}	Output resistance	-	-	12	-	kΩ
Adjacent channel gain						
G_{min}	Gain minimum	ACG=0	-	32	-	dB
G_{max}	Gain maximum	ACG=1	-	38	-	dB
Adjacent channel filter						
f_{HP}	-3dB frequency highpass	ACF=0	-	100	-	kHz
f_{BP}	Centre frequency	ACF=1	-	100	-	kHz
f_{-20dB}	Attenuation 20dB	-	-	70	-	kHz
Adjacent channel output						
V_{13}	Output voltage low	-	-	0.1	-	V
V_{13}	Output voltage high	-	-	4.9	-	V
R_{OUT}	Output resistance	-	-	4	-	kΩ
Multipath channel gain						
G_{min}	Gain minimum	MPG=0	-	12	-	dB
G_{max}	Gain maximum	MPG=1	-	23	-	dB
Multipath bandpass filter						
f_{Lower}	Centre frequency low	MPF=0	-	19	-	kHz
f_{Upper}	Centre frequency up	MPF=1	-	31	-	kHz
Q	Quality factor	-	5		10	-
Multipath output						
V_{34}	Output voltage low	-	-	0.1	-	V
V_{34}	Output voltage high	-	-	4.9	-	V
R_{OUT}	Output resistance	-	-	2.5	-	kΩ

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ISS (intelligent selectivity system)						
Filter 450 kHz						
f_{centre}	Centre frequency	f_{REF_intern} = 450 kHz	-	450	-	kHz
BW 3dB	Bandwidth, -3dB	ISS80 = 1	-	80	-	kHz
BW 20dB	Bandwidth, -20dB	ISS80 = 1	-	150	-	kHz
BW 3dB	Bandwidth, -3dB	ISS80 = 0	-	120	-	kHz
BW 20dB	Bandwidth, -20dB	ISS80 = 0	-	250	-	kHz
BW 3dB	Bandwidth weather band	ISS30 = 1	-	30	-	kHz
BW 20dB	-20dB weather band	ISS30 = 1	-	80	-	kHz
Adjacent channel ISS filter threshold						
V_{NTH}	Internal low threshold	ACNTH	-	0	-	V
V_{NTH}	Internal high threshold	ACNTH	-	0.3	-	V
V_{WTH}	Internal low threshold	ACWTH	-	0.25	-	V
V_{WTH}	Internal high threshold	ACWTH	-	0.95	-	V
Multipath threshold						
V_{THMP}	Internal low threshold	MPTH	-	0.50	-	V
V_{THMP}	Internal high threshold	MPTH	-	1.25	-	V
ISS filter time constant						
I_{15}	Charge current low mid	TISS, ISSCTL = 1	-	-74	-	µA
I_{15}	Charge current high mid	TISS, ISSCTL = 1	-	-60	-	µA
I_{15}	Charge current low narrow	TISS, ISSCTL = 1	-	-124	-	µA
I_{15}	Charge current high narrow	TISS, ISSCTL = 1	-	-110	-	µA
I_{15}	Discharge current low	TISS, ISSCTL = 0	-	1	-	µA
I_{15}	Discharge current high	TISS, ISSCTL = 0	-	15	-	µA
V_{15}	Low voltage	ISSCTL = 0	-	0.1	-	V
V_{15}	High voltage	ISSCTL = 1	-	4.9	-	V
ISS filter switch threshold						
V_{15}	Threshold ISS on	ISSCTL = 0	-	3	-	V
V_{15}	Threshold ISS off	ISSCTL = 0	-	1	-	V
V_{15}	Threshold ISS narrow on	ISSCTL = 0	-	4	-	V
V_{15}	Threshold ISS narrow off	ISSCTL = 0	-	2	-	V
I_{20}	Charge current low	TDEV	-	-20	-	µA
I_{20}	Charge current high	TDEV	-	-34	-	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{20}	Discharge current low	TDEV	-	6	-	µA
I_{20}	Discharge current high	TDEV	-	20	-	µA
DEV_{WTH}	Internal low threshold	DWTH	-	30	-	kHz
DEV_{WTH}	Internal high threshold	DWTH	-	75	-	kHz
$RATIO_{min}$	Referred to threshold	DTH	-	1	-	-
$RATIO_{max}$	Referred to threshold	DTH	-	1.5	-	-
Softmute						
V_{ANT}	Upper startpoint	SMTH, SMD, SLOPE = 0	-	10	-	dBµV
V_{ANT}	lower startpoint	SMTH, SMD, SLOPE = 0	-	3	-	dBµV
a_{SMmin}	Min. softmute depth	SMD, SLOPE = 0, $SMTH_{Upper}$	-	18	-	dB
a_{SMmax}	Max. softmute depth	SMD, SLOPE = 0, $SMTH_{Upper}$	-	36	-	dB
$a_{SMTHISS}$	Mute depth threshold for ISS filter on	SMCTH	0.2	-	2	dB
V_{ACTH}	Internal AC mute threshold	ACM	60	-	340	mV
a_{SMAC}	AC mute depth	ACMD	4	-	10	dB
I_{42}	Charge current	-	-	-47.5	-	µA
I_{42}	Discharge current	-	-	2.5	-	µA
S/N over all						
S/N	Signal to noise	V_{ANT_min} = 60 dBµV, dev.= 40 kHz,LP=15 kHz deemphasis t = 50 µs	66	-	-	dB
Additional parameters						
Output of Tuning Voltages (TV1,TV2)						
V_{OUT}	Output voltage	TVO	0.5	-	V_{CC3}-0.5	V
R_{OUT}	Output impedance	-	-	20	-	kΩ
Xtal reference oscillator						
f_{LO}	Reference frequency	C_{Load} = 15 pF	-	10.25	-	MHz
C_{Step}	Min. cap step	XTAL	-	0.75	-	pF
C_{max}	Max. cap	XTAL	-	23.25	-	pF
$\Delta f/f$	Deviation versus VCC2	ΔV_{CC2} = 1 V	-	1.5	-	ppm/V
$\Delta f/f$	Deviation versus temp	-40°C < T < +85 °C	-	0.2	-	ppm/K
I^2C bus interface						
f_{SCL}	Clock frequency	-	-	-	400	kHz
V_{IL}	Input low voltage	-	-	-	-	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage	-	3	-	-	V
I_{IN}	Input current	-	-5	-	5	µA
V_O	Output acknowledge voltage	I_O = 1.6 mA	-	-	0.4	V
Loop filter input/output						
$-I_{IN}$	Input leakage current	V_{IN} = GND, PD_{OUT} = Tristate	-0.1	-	0.1	µA
I_{IN}	Input leakage current	V_{IN} = VREF1 PD_{OUT} = Tristate	-0.1	-	0.1	µA
V_{OL}	Output voltage Low	I_{OUT} = -0.2 mA	-	0.05	0.5	V
V_{OH}	Output voltage High	I_{OUT} = 0.2 mA	V_{CC3}-0.5	V_{CC3}-0.05	-	V
I_{OUT}	Output current, sink	V_{OUT} = 1 V to V_{CC3}-1 V	-	-	10	mA
I_{OUT}	Output current, source	V_{OUT} = 1 V to V_{CC3}-1 V	-10	-	-	mA
Voltage controlled oscillator (VCO)						
f_{VCOmin}	Minimum VCO frequency	-	160	-	-	MHz
f_{VCOmax}	Maximum VCO frequency	-	-	-	260	MHz
C/N	Carrier to Noise	f_{VCO}= 200 MHz, Δf=1 kHz, B=1 Hz, closed loop	-	80	-	dBc
SSTOP output (open collector)						
V_{24}	Output voltage low	I_{24} = -200 µA	-	0.2	0.5	V
V_{24}	Output voltage high	-	-	-	5	V
$-I_{24}$	Output leakage current	V_{24} = 5 V	-0.1	-	0.1	µA
I_{24}	Output current, sink	V_{24} = 0.5 - 5 V	-	-	1	mA
ISSSTATUS output (open drain)						
V_{58}	Output voltage low, ISS-Filter “ON”	I_{24} = -200 µA	-	0.2	0.5	V
V_{58}	Output voltage high, ISS-Filter “OFF”	-	-	-	5	V
$-I_{58}$	Output leakage current	V_{24} = 5 V	-0.1	-	0.1	µA
I_{58}	Output current, sink	V_{24} = 0.5 - 5 V	-	-	300	µA

4 Functional description

4.1 Mixer 1, AGC and 1.IF

FM quadrature I/Q-mixer converts RF to IF1 of 10.7MHz. The mixer provides inherent image rejection and wide dynamic range with low noise and large input signal performance. The mixer1 tank can be adjusted by software (IF1T). For accurate image rejection the gain- and phase-error generated as well in mixer as VCO stage can be compensated by software (G,PH)

It is capable of tuning the US FM, US weather, Europe FM, Japan FM and East Europe FM bands

- US FM = 87.9 to 107.9 MHz
- US weather = 162.4 to 162.55 MHz
- Europe FM = 87.5 to 108 MHz
- Japan FM = 76 to 91 MHz
- East Europe FM = 65.8 to 74 MHz

The AGC operates on different sensitivities and bandwidths in order to improve the input sensitivity and dynamic range. AGC thresholds are programmable by software (RFAGC,IFAGC,KAGC). The output signal is a controlled current for double pin diode attenuator. Two 10.7 MHz programmable amplifiers (IFG1, IFG2) correct the IF ceramic insertion loss and the costumer level plan application.

4.2 Mixer 2, limiter and demodulator

In this 2. mixer stage the first 10.7 MHz IF is converted into the second 450 kHz IF. A multi-stage limiter generates signals for the complete integrated demodulator without external tank. MPX output DC offset versus noise DC level is correctable by software (DEM).

4.3 Quality detection and ISS

4.3.1 Fieldstrength

Parallel to mixer 2 input a 10.7 MHz limiter generates a signal for digital IF counter and a fieldstrength output signal. This internal unweighted fieldstrength is used for keying AGC, adjacent channel and multipath detection and is available at PIN14 (FSU) after +6dB buffer stage. The behaviour of this output signal can be corrected for DC offset (SL) and slope (SMSL). The internal generated unweighted fieldstrength is filtered at PIN35 and used for softmute function and generation of ISS filter switching signal for weak input level (sm).

4.3.2 Adjacent channel detector

The input of the adjacent channel detector is AC coupled from internal unweighted fieldstrength. A programmable highpass or bandpass (ACF) and amplifier (ACG) as well as rectifier determines the influences. This voltage is compared with adjustable comparator1 thresholds (ACWTH, ACNTH). The output signal of this comparator generates a DC level at PIN15 by programmable time constant. Time control (TISS) for a present adjacent channel is made by charge and discharge current after comparator1 in an external capacitance. The

charge current is fixed and the discharge current is controlled by I^2C Bus. This level produces digital signals (ac, ac+) in an additional comparator4. The adjacent channel information is available as analog output signal after rectifier and +8 dB output buffer.

4.3.3 Multipath detector

The input of the multipath detector is AC coupled from internal unweighted fieldstrength. A programmable bandpass (MPF) and amplifier (MPG) as well as rectifier determines the influences. This voltage is compared with an adjustable comparator2 thresholds (MPTH). The output signal of this comparator 2 is used for the "Milano" effect. In this case the adjacent channel detection is switched off. The "Milano" effect is selectable by I^2C bus (MPOFF). The multipath information is available as analog output signal after rectifier and +8 dB output buffer.

4.3.4 450 kHz IF narrow bandpass filter (ISS filter)

The device gets an additional second IF narrow bandpass filter for suppression of noise and adjacent channel signal influences. This narrow filter has three switchable bandwidthes, narrow range of 80 kHz, mid range of 120 kHz and 30 kHz for weather band information.

Without ISS filter the IF bandwidth (wide range) is defined only by ceramic filter chain. The filter is switched in after mixer 2 before 450 kHz limiter stage. The centre frequency is matching to the demodulator center frequency.

4.3.5 Deviation detector

In order to avoid distortion in audio output signal the narrow ISS filter is switched OFF for present overdeviation. Hence the demodulator output signal is detected.

A lowpass filtering and peak rectifier generates a signal that is defined by software controlled current (TDEV) in an external capacitance. This value is compared with a programmable comparator3 thresholds (DWTH, DTH) and generates two digital signals (dev, dev+). For weak signal condition deviation threshold is proportinal to FSU.

4.3.6 ISS switch logic

All digital signals coming from adjacent channel detector, deviation detector and softmute are acting via switching matrix on ISS filter switch. The IF bandpass switch mode is controlled by software (ISSON, ISS30, ISS80, CTLOFF).

The switch ON of the IF bandpass is also available by external manipulation of the voltage at PIN15.

Two application modes are available (APPM). The conditions are described in table 34.

4.4 Soft Mute control

The external fieldstrength signal at PIN 35 is the reference for mute control. The startpoint and mute depth are programmable (SMTH, SMD) in a wide range. The time constant is defined by external capacitance. Additional adjacent channel mute function is supported.

A highpass filter with -3 dB threshold frequency of 100 kHz, amplifier and peak rectifier generates an adjacent noise signal from MPX output with the same time constant for

softmute. This value is compared with comparator5 thresholds (ACM). For present strong adjacent channel the MPX signal is additional attenuated (ACMD).

4.5 PLL and IF counter section

4.5.1 PLL frequency synthesizer block

This part contains a frequency synthesizer and a loop filter for the radio tuning system. Only one VCO is required to build a complete PLL system for FM world tuning . For auto search stop operation an IF counter system is available.

The counter works in a two stages configuration. The first stage is a swallow counter with a two modulus (32/33) precounter. The second stage is an 11-bit programmable counter.

The circuit receives the scaling factors for the programmable counters and the values of the reference frequencies via an I^2C bus interface.The reference frequency is generated by an adjustable internal (XTAL) oscillator followed by the reference divider. The main reference and step-frequencies are free selectable (RC, PC).

Output signals of the phase detector are switching the programmable current sources. The loop filter integrates their currents to a DC voltage.

The values of the current sources are programmable by 6 bits also received via the I^2C Bus (A, B, CURRH).

To minimize the noise induced by the digital part of the system, a special guard configuration is implemented. The loop gain can be set for different conditions by setting the current values of the chargepump generator.

4.5.2 Frequency generation for phase comparison

The RF signals applies a two modulus counter (32/33) pre-scaler, which is controlled by a 5-bit A-divider. The 5-bit register (PC0 to PC4) controls this divider. In parallel the output of the prescaler connects to an 11-bit B-divider. The 11-bit PC register (PC5 to PC15) controls this divider

Dividing range:

$f_{VCO} = [33 \times A + (B + 1 - A) \times 32] \times f_{REF}$

$f_{VCO} = (32 \times B + A + 32) \times f_{REF}$

Important: For correct operation: $A \leq 32$; $B \geq A$

4.5.3 Three state phase comparator

The phase comparator generates a phase error signal according to phase difference between f_{SYN} and f_{REF}. This phase error signal drives the charge pump current generator.

4.5.4 Charge pump current generator

This system generators signed pulses of current. The phase error signal decides the duration and polarity of those pulses. The current absolute values are programmable by A register for high current and B register for low current.

4.5.5 Inlock detector

Switching the chargepump in low current mode can be done either via software or automatically by the inlock detector, by setting bit LDENA to "1".

After reaching a phase difference about lower than 40nsec the chargepump is forced in low current mode. A new PLL divider alternation by I^2C-Bus will switch the chargepump in the high current mode.

4.5.6 Low noise CMOS op-amp

An internal voltage divider at pin VREF2 connects the positive input of the low noise op-amp. The charge pump output connects the negative input. This internal amplifier in cooperation with external components can provide an active filter.

While the high current mode is activated LPHC output is switched on.

4.5.7 IF counter block

The aim of IF counter is to measure the intermediate frequency of the tuner. The input signal is the 10.7MHz IF level after limiter.

The grade of integration is adjustable by eight different measuring cycle times. The tolerance of the accepted count value is adjustable, to reach an optimum compromise for search speed and precision of the evaluation.

4.5.8 Sampling timer

A sampling timer generates the gate signal for the main counter. The basically sampling time are in FM mode 6.25kHz (t_{TIM}=160μs).

This is followed by an asynchronous divider to generate several sampling times.

4.5.9 Intermediate frequency main counter

This counter is a 11 - 21-bit synchronous autoreload down counter. Five bits (CF) are programmable to have the possibility for an adjust to the centre frequency of the IF-filter. The counter length is automatic adjusted to the chosen sampling time.

At the start the counter will be loaded with a defined value which is an equivalent to the divider value (t_{Sample} x f_{IF}).

If a correct frequency is applied to the IF counter frequency input at the end of the sampling time the main counter is changing its state from 0h to 1FFFFFh.

This is detected by a control logic and an external search stop output is changing from LOW to HIGH. The frequency range inside which a successful count result is adjustable by the EW bits.

$$t_{CNT} = \frac{CF + 1696 + 1}{f_{IF}}$$

Counter result succeeded:

$t_{TIM} \geq t_{CNT} - t_{ERR}$

$t_{TIM} \leq t_{CNT} + t_{ERR}$

Counter result failed:

$t_{TIM} > t_{CNT} + t_{ERR}$

$t_{TIM} < t_{CNT} - t_{ERR}$

t_{TIM} = IF timer cycle time (sampling time)

t_{CNT} = IF counter cycle time

t_{ERR} = discrimination window (controlled by the EW registers)

The IF counter is only started by inlock information from the PLL part. It is enabled by software (IFENA).

4.5.10 Adjustment of the measurement sequence time

The precision of the measurements is adjustable by controlling the discrimination window. This is adjustable by programming the control registers EW.

The measurement time per cycle is adjustable by setting the registers IFS.

4.5.11 Adjust of the frequency value

The center frequency of the discrimination window is adjustable by the control registers CF.

4.6 I²C bus interface

The TDA7512F supports the I²C bus protocol. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device that controls the transfer is a master and device being controlled is the slave. The master will always initiate data transfer and provide the clock to transmit or receive operations.

4.6.1 Data transition

Data transition on the SDA line must only occur when the clock SCL is LOW. SDA transitions while SCL is HIGH will be interpreted as START or STOP condition.

4.6.2 Start condition

A start condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This "START" condition must precede any command and initiate a data transfer onto the bus.

The device continuously monitors the SDA and SCL lines for a valid START and will not response to any command if this condition has not been met.

4.6.3 Stop condition

A STOP condition is defined by a LOW to HIGH transition of the SDA while the SCL line is at a stable HIGH level. This condition terminates the communication between the devices and forces the bus-interface of the device into the initial condition.

4.6.4 Acknowledge

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line to LOW level to indicate it receive the eight bits of data.

4.6.5 Data transfer

During data transfer the device samples the SDA line on the leading edge of the SCL clock. Therefore, for proper device operation the SDA line must be stable during the SCL LOW to HIGH transition.

4.6.6 Device addressing

To start the communication between two devices, the bus master must initiate a start instruction sequence, followed by an eight bit word corresponding to the address of the device it is addressing.

The most significant 6 bits of the slave address are the device type identifier.

The TDA7512F device type is fixed as "110001".

The next significant bit is used to address a particular device of the previous defined type connected to the bus.

The state of the hardwired PIN 41 defines the state of this address bit. So up to two devices could be connected on the same bus. When PIN 41 is connected to VCC2 the address bit “1” is selected. When PIN 41 is left open the address bit “0” is selected. Therefor a double FM tuner concept is possible.

The last bit of the start instruction defines the type of operation to be performed:

- When set to "1", a read operation is selected
- When set to "0", a write operation is selected

The TDA7512F connected to the bus will compare their own hardwired address with the slave address being transmitted, after detecting a START condition. After this comparison, the TDA7512F will generate an "acknowledge" on the SDA line and will do either a read or a write operation according to the state of R/W bit.

4.6.7 Write operation

Following a START condition the master sends a slave address word with the R/W bit set to "0". The device will generate an "acknowledge" after this first transmission and will wait for a second word (the word address field). This 8-bit address field provides an access to any of the 32 internal addresses.

Upon receipt of the word address the TDA7512F slave device will respond with an "acknowledge". At this time, all the following words transmitted to the TDA7512F will be considered as Data.

The internal address will be automatically incremented. After each word receipt the TDA7512F will answer with an "acknowledge".

4.6.8 Read operation

If the master sends a slave address word with the R/W bit set to "1", the TDA7512F will transit one 8-bit data word. This data word includes the following informations:

bit0 (ISS filter, 1 = ON, 0 = OFF)

bit1 (ISS filter bandwidth, 1 = 80kHz, 0 = 120kHz)

bit2 (MPOUT,1 = multipath present, 0 = no multipath)

bit3 (1 = PLL is locked in , 0 = PLL is locked out).

bit4 (fieldstrength indicator, 1 = lower as softmute threshold, 0 = higher as softmute threshold)

bit5 (adjacent channel indicator, 1 = adjacent channel present, 0 = no adjacent channel)

bit6 (deviation indicator, 1 = strong overdeviation present, 0 = no strong overdeviation)

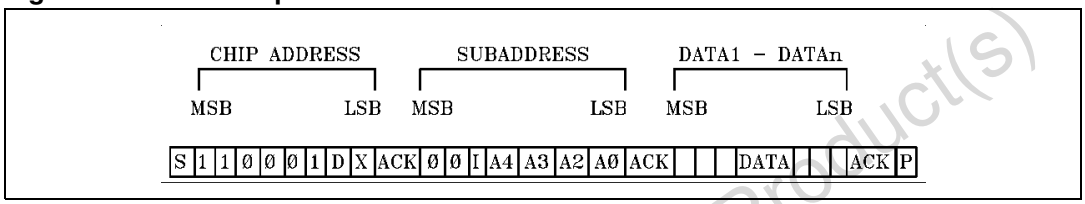
bit7 (deviation indicator, 1 = overdeviation present, 0 = no overdeviation)

5 Software specification

The interface protocol comprises:

- start condition (S)
- chip address byte
- subaddress byte
- sequence of data (N bytes + Acknowledge)
- stop condition (P)

Figure 3. Interface protocol



S = Start

P = Stop

ACK = Acknowledge

D = Device Address

X = R/W bit

I = Pagemode

A = Subaddress

5.1 Address organization

Table 6. Address organization

Function	Addr	7	6	5	4	3	2	1	0
CHARGEPUMP	0	LDENA	CURRH	B1	B0	A3	A2	A1	A0
PLL COUNTER	1	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
	2	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
TV1	3	TV1O7	TV1O6	TV1O5	TV1O4	TV1O3	TV1O2	TV1O1	TV1O0
TV2	4	TV2O7	TV2O6	TV2O5	TV2O4	TV2O3	TV2O2	TV2O1	TV2O0
IFC CTRL 1	5	LM	CASF	-	-	IFENA	IFS2	IFS1	IFS0
IFC CTRL 2	6	EW2	EW1	EW0	CF4	CF3	CF2	CF1	CF0
not valid	7	-	-	-	-	-	-	-	-
QUALITYISS	8	TISS2	TISS1	TISS0	TVWB	ISS30	ISS80	ISSON	CTLOFF
QUALITY AC	9	ACNTH1	ACNTH0	ACWTH2	ACWTH1	ACWTH0	ACG	ACF	-
QUALITY MP	10	MPAC	APPM2	APPM1	MPTH1	MPTH0	MPG	MPF	MPOFF

Table 6. Address organization (continued)

Function	Addr	7	6	5	4	3	2	1	0
QUALITYDEV	11	BWCTL	DTH1	DTH0	DWTH1	DWTH0	TDEV2	TDEV1	TDEV0
MUTE1	12	MENA	SMD3	SMD2	SMD1	SMD0	SMTH2	SMTH1	SMTH0
MUTE2	13	F100K	ACM3	ACM2	ACM1	ACM0	ACMD1	ACMD0	SMCTH
VCO/PLLREF	14	-	-	RC2	RC1	RC0	VCOD2	VCOD1	VCOD0
FMAGC	15	-	KAGC2	KAGC1	KAGC0	IFAGC1	IFAGC0	RFAGC1	RFAGC0
not valid	16	-	-	-	-	-	-	-	-
DEM ADJ	17	DNB1	DNB0	DEM5	DEM4	DEM3	DEM2	DEM1	DEM0
LEVEL	18	ODSW	-	SMSL	SL4	SL3	SL2	SL1	SL0
IF1/XTAL	19	XTAL4	XTAL3	XTAL2	XTAL1	XTAL0	IFG11	IFG10	IFG2
TANK ADJ	20	IF1T3	IF1T2	IF1T1	IF1T0	-	-	-	-
I/Q ADJ	21	ODCUR	-	G1	G0	PH3	PH2	PH1	PH0
TESTCTRL1	22	-	ISSIN	TOUT	TIN	CLKSEP	TEST3	TEST2	TEST1
TESTCTRL2	23	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
TESTCTRL3	24	-	TINACM	TINMP	TINAC	OUT11	OUT10	OUT9	OUT8
TESTCTRL4	25	-	-	-	OUT16	OUT15	OUT14	OUT13	OUT12

5.2 Control register function

Table 7. Control register function

Register Name	Function
A	Charge pump high current
ACF	Adjacent channel filter select
ACG	Adjacent channel filter gain
ACM	Threshold for startpoint adjacent channel mute
ACMD	Adjacent channel mute depth
ACNTH	Adjacent channel narrow band threshold
ACWTH	Adjacent channel wide band threshold
APPM	Application mode quality detection
B	Charge pump low current
BWCTL	ISS filter fixed bandwith (ISS80) in automatic control
CASF	Check alternative station frequency
CF	Center frequency IF counter
CLKSEP	Clock separation (only for testing)
CTLOFF	Switch off automatic control of ISS filter
CURRH	Set current high charge pump