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TDA7590

Digital signal processing IC for speech and audio applications

Features

- 24-bit, fixed point, 120 MIPS DSP core
- Large on-board memory (128KW-24 bit)
- Host access to internal RAM through expansion port
- Access to external RAM (16Mw) through expansion port
- Integrated stereo, 18-bit Sigma-DELTA A/D and 20-bit D/A converters
- Programmable CODEC sample rate up to 48 kHz
- On-board PLL for core clock and converters
- External Flash/SRAM memory bank management
- I^2C and SCI serial interface for external control
- 2 enhanced synchronous serial interface (ESSI)
- JTAG interface
- Host interface
- 144-pin TQFP, 0.50 mm pitch
- Automotive temperature range (from -40 °C to +85 °C)

Applications

- Real time digital speech and audio processing:
  - speech recognition
  - speech synthesis
  - speech compression
  - echo canceling
  - noise canceling
  - MP3 decoding

TQFP144

Description

The TDA7590 is a high performances, fully programmable 24-bit, 120 MIPS. Digital signal processor (DSP), designed to support several speech and audio applications, as automatic speech recognition, speech synthesis, MP3 decoding, echo and noise cancellation.

Nevertheless, the embedded CODECs bandwidth and the generic processing engine allow to proceed also full-band audio signals. The large amount of on-chip memory (128 Kwords), together with the 16 Mwords external memory addressable and the 32 general purpose I/O pins permit to build a DSP-system avoiding the usage of an additional microcontroller.

The presence of serial and parallel interfaces allows easy connection with external devices including CODECs, DSPs, microprocessors and personal computers.

In particular, the debug/JTAG interface permits the on-chip emulation of the firmware developed. Further, the presence of the timers and watchdog block makes TDA7590 suitable for PWM processing and allows the integration of a system watchdog.

Table 1. Device summary

Order code	Package	Packing
E-TDA7590	TQFP144 (20x20x1.0 exposed pad down)(1)	Tray
E-TDA7590TR		Tape and reel

1. In ECOPACK® package (see *Section 8: Package information on page 22*).

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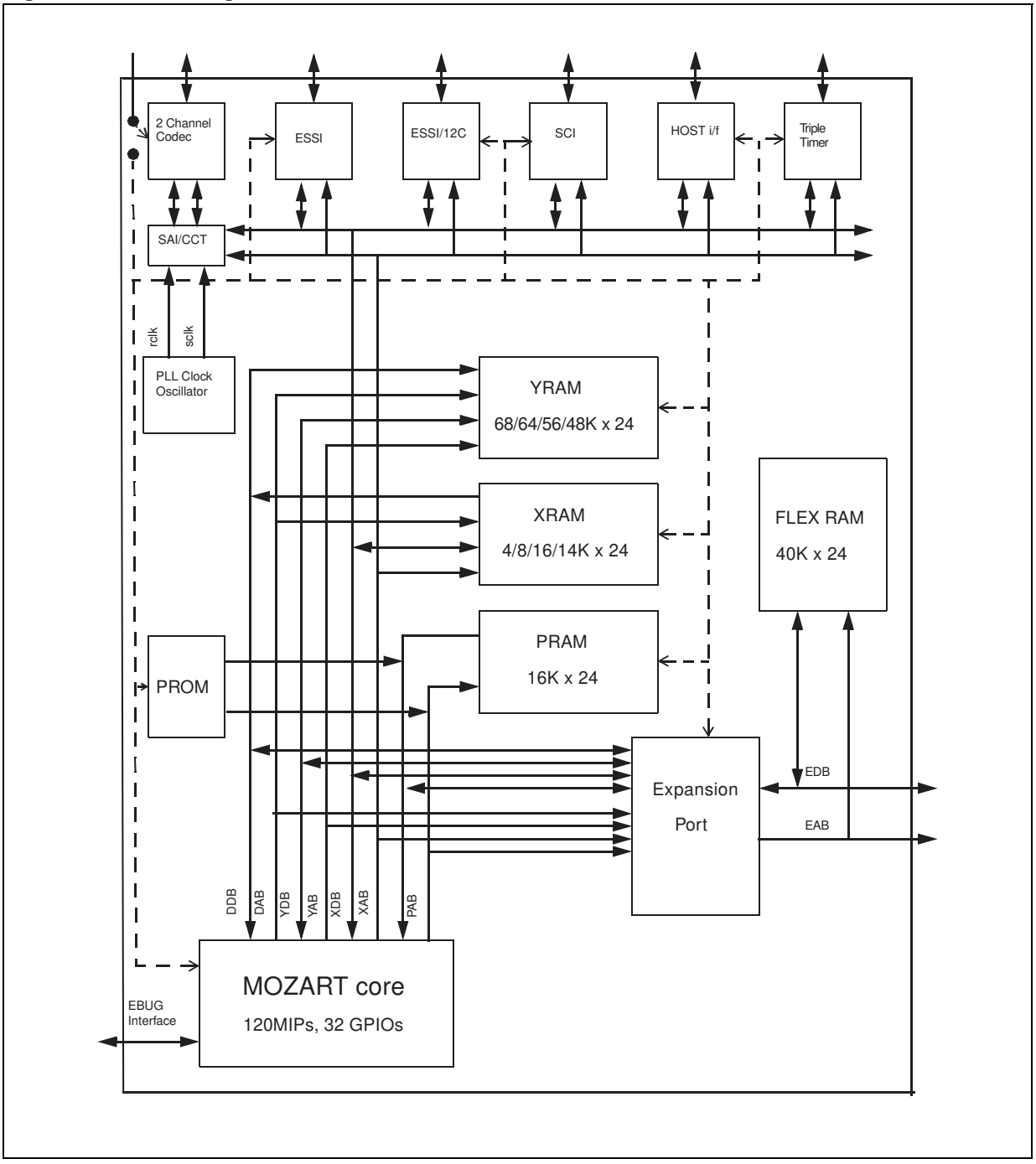
1 Block diagram

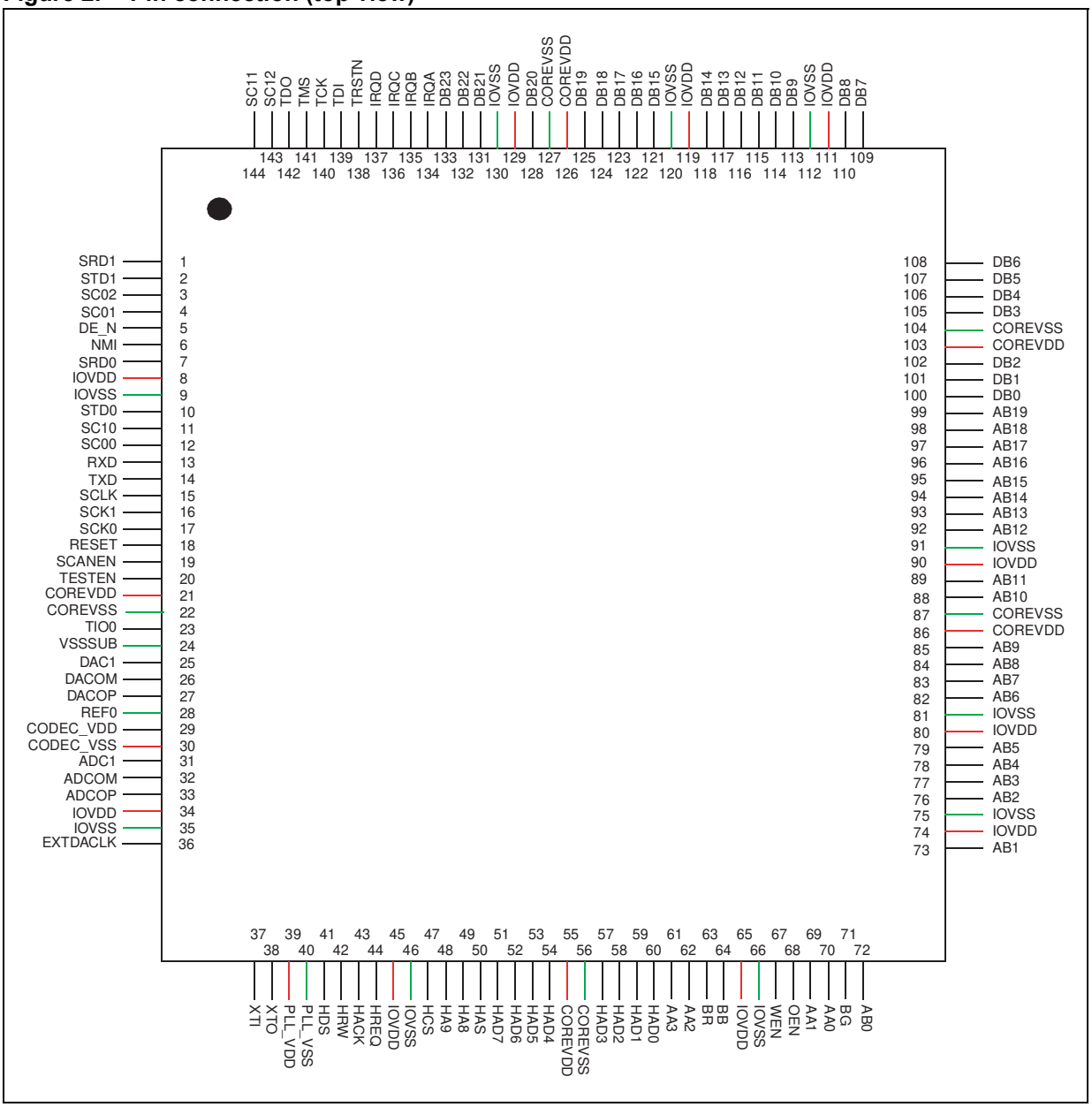
Figure 1. Block diagram



2 Pin description

2.1 Pin connection

Figure 2. Pin connection (top view)



2.2 Pin function

Table 2. Pin function

N°	Name	Type	Description
1	SRD1/TI02	I/O	Serial receive data. Serial input data for receiver. Timer 2 input/output.
2	STD1	I/O	Serial transmit data. Serial output data from transmitter.
3	SC02	I/O	Serial control 2.Transmitter frame sync only in asynchronous mode, transmitter and receiver frame sync in synchronous mode.
4	SC01	I/O	Serial control 1. Receive frame sync in asynchronous mode, output from transmitter 2 or serial flag 1 in synchronous mode.
5	DE_N	I/O	Test data output (input/output). Debug request input and acknowledge output.
6	NMI_N	I	Non-maskable interrupt/ PINIT. Used to enable the PLL during RESET and as a non-maskable interrupt at all other times.
7	SRD0	I/O	Serial receive data. Serial input data for receiver.
8	IOVDD	I	IO power supply.
9	IOVSS	I	IO ground.
10	STD0	I/O	Serial Transmit Data. Serial output data from transmitter.
11	SC10/SCL	I/O	ESSI1 serial control 0. Receive clock in asynchronous mode, output from transmitter or serial flag in synchronous mode. I^2C SCL serial clock line.
12	SC00	I/O	Serial control 0. Receive clock in asynchronous mode, output from transmitter 1 or serial flag 0 in synchronous mode.
13	RXD	I/O	SCI receive data. Receives byte-oriented serial data.
14	TXD	I/O	SCI read enable. Transmits serial data from SCI transmit shift register.
15	SCLK	I/O	SCI serial clock. Input or output clock from which data is transferred in synchronous mode and from which the transmit and/or receive baud rate is derived in asynchronous mode.
16	SCK1/TI01	I/O	Serial clock. Serial bit clock for transmitter only in asynchronous mode, serial bit clock for both receiver and transmitter in synchronous mode. Timer 1 input/output.
17	SCK0	I/O	Serial clock. Serial bit clock for transmitter only in asynchronous mode, serial bit clock for both receiver and transmitter in synchronous mode.
18	RESETN	I	System reset. A low level applied to RESET_N input initializes the IC.
19	SCANEN	I	SCAN enable. When active with TESTEN also active, controls the shifting of the internal scan chains.
20	TESTEN	I	Test enable. When active, puts the chip into test mode and muxes the XTI clock to all flip-flops. When SCANEN is also active, the scan chain shifting is enabled.
21	COREVSS	I	Core ground.
22	COREVDD	I	Core power supply.
23	TIO0	I/O	Timer 0 input/output.
24	VSSSUB	I	Analog substrate isolation.

Table 2. Pin function (continued)

N°	Name	Type	Description
25	DAC1	O	DAC1 left single analog output.
26	DAC0M	O	DAC0 negative right differential analog output.
27	DAC0P	O	DAC0 positive right differential analog output.
28	CODEC_VSS	I	Voltage ground.
29	REF0	I	Codec power supply.
30	CODEC_VDD	I	Codec reference.
31	ADC1	I	ADC1 left single analog input.
32	ADC0M	I	DAC0 negative right differential analog inputs.
33	ADC0P	I	DAC0 positive right differential analog inputs.
36	EXTDACLK	I	External DAC clock. Optional external clock source from which LRCLK and SCLK can be generated.
37	XTI	I	Crystal oscillator input. External clock input or crystal connection.
38	XTO	O	Crystal oscillator output. Crystal oscillator output drive.
39	PLL_VDD	I	PLL power supply.
40	PLL_VSS	I	PLL ground input.
41	HDS	I/O	Host data strobe. Polarity programmable Host data strobe input for single strobe mode. Polarity programmable Host write strobe input for double strobe mode.
42	HRW	I/O	Host read/write. Host read/write for single strobe bus mode. Polarity programmable Host read data strobe for double strobe mode.
43	HACK	I/O	Host acknowledge. Polarity programmable host interrupt acknowledge for single host request mode. Polarity programmable host receive request interrupt for double host request mode.
44	HREQ	I/O	Host request. Polarity programmable host request interrupt for single host request mode. Polarity programmable host transfer request interrupt for double host request mode.
45	IOVDD	I	IO power supply.
46	IOVSS	I	IO ground.
47	HCS	I/O	Host chip select. Polarity programmable host chip select for non-multiplexed mode. Host address Line 10 for multiplexed mode.
48	HA9	I/O	Host address 9. Address line 9 in multiplexed mode otherwise address line 2 in non-multiplexed mode.
49	HA8	I/O	Host address 8. Address line 8 in multiplexed mode otherwise address line 1 in non-multiplexed mode.
50	HAS	I/O	Host address strobe. Address strobe for multiplexed bus or Address 0 for non multiplexed.
51	HAD[7]	I/O	Host 8-bit data line 7. Host data bus and/or address lines when in multiplexed mode.

Table 2. Pin function (continued)

N°	Name	Type	Description
52	HAD[6]	I/O	Host 8-bit data line 6. Host data bus and/or address lines when in multiplexed mode.
53	HAD[5]	I/O	Host 8-bit data line 5. Host data bus and/or address lines when in multiplexed mode.
54	HAD[4]	I/O	Host 8-bit data line 4. Host data bus and/or address lines when in multiplexed mode.
55	COREVDD	I	Core power supply.
56	COREVSS	I	Core ground.
57	HAD[3]	I/O	Host 8-bit data line 3. Host data bus and/or address lines when in multiplexed mode.
58	HAD[2]	I/O	Host 8-bit data line 2. Host data bus and/or address lines when in multiplexed mode.
59	HAD[1]	I/O	Host 8-bit data line 1. Host data bus and/or address lines when in multiplexed mode.
60	HAD[0]	I/O	Host 8-bit data line 0. Host data bus and/or address lines when in multiplexed mode.
61	AA[3]	O	Address attributes line 3.Port A address attributes/chip select pins with programmable polarity.
62	AA[2]	O	Address attributes line 2.Port A address attributes/chip select pins with programmable polarity.
63	BR_N	O	Bus request. Asserted when port A requires bus mastership to perform off-chip accesses.
64	BB_N	I/O	Bus busy. Asserted by port A when bus_busy_in_n is negated and BG_N is asserted.
65	IOVDD	I	IO power supply.
66	IOVSS	I	IO ground.
67	WEN_N	O	Write enable.
68	OEN_N	O	Output enable.
69	AA[1]	O	Address attributes line 1.Port A address attributes/chip select pins with programmable polarity.
70	AA[0]	O	Address attributes line 0.Port A address attributes/chip select pins with programmable polarity.
71	BG_N	I	Bus grant. When asserted, Port A becomes the bus master elect. Bus mastership is attained when bus busy is negated by the current bus master.
72	AB[0]	O	Address bus line 0. Port A external address bus.
73	AB[1]	O	Address bus line 1. Port A external address bus.
74	IOVDD	I	IO power supply.
75	IOVSS	I	IO ground.
76	AB[2]	O	Address bus line 2. Port A external address bus.

Table 2. Pin function (continued)

N°	Name	Type	Description
77	AB[3]	O	Address bus line 3. Port A external address bus.
78	AB[4]	O	Address bus line 4. Port A external address bus.
79	AB[5]	O	Address bus line 5. Port A external address bus.
80	IOVDD	I	IO power supply.
81	IOVSS	I	IO ground.
82	AB[6]	O	Address bus line 6. Port A external address bus.
83	AB[7]	O	Address bus line 7. Port A external address bus.
84	AB[8]	O	Address bus line 8. Port A external address bus.
85	AB[9]	O	Address bus line 9. Port A external address bus.
86	COREVDD	I	Core power supply.
87	COREVSS	I	Core ground.
88	AB[10]	O	Address bus line 10. Port A external address bus.
89	AB[11]	O	Address bus line 11. Port A external address bus.
90	IOVDD	I	IO power supply.
91	IOVSS	I	IO ground.
92	AB[12]	O	Address bus line 12. Port A external address bus.
93	AB[13]	O	Address bus line 13. Port A external address bus.
94	AB[14]	O	Address bus line 14. Port A external address bus.
95	AB[15]	O	Address bus line 15. Port A external address bus.
96	AB[16]	O	Address bus line 16. Port A external address bus.
97	AB[17]	O	Address bus line 17. Port A external address bus.
98	AB[18]	O	Address bus line 18. Port A external address bus.
99	AB[19]	O	Address bus line 19. Port A external address bus.
100	DB[0]	I/O	Address bus 0. Port A external data bus.
101	DB[1]	I/O	Address bus 1. Port A external data bus.
102	DB[2]	I/O	Address bus 2. Port A external data bus.
103	COREVDD	I	Core power supply.
104	COREVSS	I	Core ground.
105	DB[3]	I/O	Data bus line 3. Port A external data bus.
106	DB[4]	I/O	Data bus line 4. Port A external data bus.
107	DB[5]	I/O	Data bus line 5. Port A external data bus.
108	DB[6]	I/O	Data bus line 6. Port A external data bus.
109	DB[7]	I/O	Data bus line 7. Port A external data bus.
110	DB[8]	I/O	Data bus line 8. Port A external data bus.
111	IOVDD	I	IO Power Supply.

Table 2. Pin function (continued)

N°	Name	Type	Description
112	IOVSS	I	IO Ground.
113	DB[9]	I/O	Data Bus line 9. Port A external data bus.
114	DB[10]	I/O	Data bus line 10. Port A external data bus.
115	DB[11]	I/O	Data bus line 11. Port A external data bus.
116	DB[12]	I/O	Data bus line 12. Port A external data bus.
117	DB[13]	I/O	Data bus line 13. Port A external data bus.
118	DB[14]	I/O	Data bus line 14. Port A external data bus.
119	IOVDD	I	IO power supply.
120	IOVSS	I	IO Ground.
121	DB[15]	I/O	Data bus line 15. port a external data bus.
122	DB[16]	I/O	Data bus line 16. Port A external data bus.
123	DB[17]	I/O	Data bus line 17. Port A external data bus.
124	DB[18]	I/O	Data bus line 18. Port A external data bus.
125	DB[19]	I/O	Data bus line 19. Port A external data bus.
126	COREVDD	I	Core power supply.
127	COREVSS	I	Core ground.
128	DB[20]	I/O	Data bus line 20. Port A external data bus.
129	IOVDD	I	IO power supply.
130	IOVSS	I	IO ground.
131	DB[21]	I/O	Data bus line 21. Port A external data bus.
132	DB[22]	I/O	Data bus line 22. Port A external data bus.
133	DB[23]	I/O	Data bus line 23. Port A external data bus.
134	IRQA	I	Interrupt request line/ Mode control. Used as mode control during RESET and as interrupt request line at all other times.
135	IRQB	I	Interrupt request line/ Mode control. Used as mode control during RESET and as interrupt request line at all other times.
136	IRQC	I	Interrupt request line/ Mode control. Used as mode control during RESET and as interrupt request line at all other times.
137	IRQD	I	Interrupt request line/ Mode control. Used as mode control during RESET and as interrupt request line at all other times.
138	TRSTN	I	Test reset. JTAG output pin for serial data out from debug interface.
139	TDI	I	Test data input. JTAG input pin for serial data input for debug interface.
140	TCK	I	Test clock. JTAG input pin for clocking debug interface.
141	TMS	I	Test mode select. JTAG input pin for control of TAP Controller of debug interface.
142	TDO	O	Test data output. JTAG output pin for serial data out from debug interface.

Table 2. Pin function (continued)

N°	Name	Type	Description
143	SC12	I/O	Serial control 2.Transmitter frame sync only in asynchronous mode, transmitter and receiver frame sync in synchronous mode.
144	SC11/SDA	I/O	Serial control 1. Receive frame sync in asynchronous mode, output from transmitter 2 or serial flag 1 in synchronous mode. I^2C SDA. Serial data line.

2.3 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\text{-}j\text{-}pins}$	Thermal resistance junction to pins	32	°C/W

3 Key parameters

3.1 Power consumption

Power consumption depends on application running and DSP clock frequency.

Supply current values are measured and guaranteed at testing level by adopting the benchmarking program reported in Appendix 1.

Table 4. Key parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
General					
fosc	Crystal frequency			16	MHz
CORE_VDD	Operating voltage	1.62	1.8	1.98	V
CODEC_VDD	Operating voltage	3.0	3.3	3.6	V
IOVDD	Operating voltage	3.0	3.3	3.6	V
PLL_VDD	Operating voltage	3.0	3.3	3.6	V
IDD_1.8V	Supply current			150	mA
IDD_3.3V	Supply current			50	mA
Tamb	Operating temperature	-40		85	°C
DSP core					
fdsp	DSP clock frequency			120	MHz
ADC single ended					
Vpp	Maximum input range at ADC1			1.4	V
THD/S	Total harmonics distortion to signal		-71		dB
(THD+N)/S	(THD + Noise) to signal		-70		dB
DR	Dynamic range		75		dB
ICL	Interchannel Isolation		-100		dB
ADC differential					
Vpp	Maximum input range at ADC0M-ADC0P			2.8	V
THD/S	Total harmonics distortion to signal		-65		dB
(THD+N)/S	(THD + Noise) to signal		-65		dB
DR	Dynamic range		84		dB
ICL	Interchannel isolation		-100		dB
DAC single ended					
Vpp	Maximum input range at ADC1			1.4	V
THD/S	Total harmonics distortion to signal		-64		dB
(THD+N)	(THD + Noise) to signal		-60		dB

Table 4. Key parameters (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
DR	Dynamic range		89		dB
ICL	Interchannel isolation		-100		dB
DAC differential					
Vpp	Maximum input range at ADC1			2.8	V
THD/S	Total harmonics distortion to signal		-58		dB
(THD+N)/S	(THD + Noise) to signal		-57		dB
DR	Dynamic range		90		dB
ICL	Interchannel Isolation		-85		dB

3.1.1 CODEC (ADC/DAC) test description

Reported typical values (table 3. - ADC and DAC sections) have been measured at Lab level during product evaluation phase. General definitions and procedures are separately defined in following dedicated paragraphs.

Total harmonic distortion with noise to signal (THD+N)/S

THD+N is defined as the ratio of the total power of the second power and higher harmonic with noise components to the power of the fundamental for that signal. For THD+N measurement, choose the DSP analyzer in digital analyzer with THD ratio as measurement option. Measure the THD+N value at -3 dB amplitude of the input signal. First measure the THD+N value at 1Vrms which is 0 dB reference and then measure the value at -3 dB reference.

Dynamic range (DR)

DR is defined as the level of THD+N measured when the input sine wave amplitude is so small that no harmonics apart from the fundamental tone are present in the output signal. This way THD+N becomes practically the ratio between the whole signal and noise floor, being a different way to express SNR. As a convention, at which no harmonics should be present in the output signal, it is fixed at -40dB of the full scale amplitude.

Crosstalk or interchannel isolation

A disturbance, caused by electromagnetic interference, along a circuit or a cable pair. An electric signal disrupts another signal in an adjacent circuit and can cause it to become confused and cross over each other. Crosstalk is measured by applying a signal -3dB amplitude of input signal at one channel (A) and no signal at an other channel (B), measuring the effect on this channel (B) because of the channel (A).

Total harmonic distortion to signal (THD)/S

THD is defined as the ratio of the sum of only those components of the output signal which are harmonic of system input, after having removed the fundamental tone corresponding to the pure sine wave as input and the input signal.This measurement is done by using the Harmonic analyzer which can isolate up to 15th harmonic components on the acquired signal and report the sum of all of them, centering the fundamental tone on the frequency provided by the input signal generator. These measurements are performed at -3dB reference amplitude of input signal.

4 Electrical specification

4.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
PLL_VDD	3.3V PLL power supply voltage	-0.5 to 4	V
CODEC_VDD	3.3V CODEC analog power supply	-0.5 to 4	V
IOVDD	3.3V IO power supply	-0.5 to 4	V
CORE_VDD	1.8V CORE power supply	-0.5 to 2.2	V
IO_MAX	Input or output voltage	-0.5 to (IOVDD +0.5)	V

4.2 Electrical characteristics for I/O pins

Table 6. Recommended DC operating conditions

Symbol	Parameter	Value	Unit
IOVDD	IO power supply voltage	3 to 3.6(1)	V
T_j	Operating junction temperature	-40 to 105	°C

1. All the specification are valid only within these recommended operating conditions.

Table 7. General interface electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Iil	Low level input current without pull-up device				1	µA
Iih	High level input current without pull-down device				1	µA
Ioz	Tri-state output leakage without pull up/down device				1	µA
IozFT	Five Volt tolerant tri-state output leakage without pull up/down device				1	µA
I latch-up	I/O latch-up current	V < 0V, V < Vdd	200			mA
Vesd	Electrostatic protection (HBM)	leakage < 1mA	2000			V
Vil	Low level input voltage(1))				0.8	V
Vih	High level input voltage(1)		2			V
Vhyst	Schmitt trigger hysteresis(1)		0.4			V
Vol	Low level output voltage (1) (2) (3)	Iol = XmA			0.15	V
Voh	High level output voltage (1) (2) (3)	Ioh = -XmA	IOVDD - 0.15			V

1. TTL specifications only apply to the supply voltage range Vdd = 3.15V to 3.6V.
2. Takes into account 200mV voltage drop in both supply lines.
3. X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

5 24 bit DSP core

The DSP core is a general purpose 24-bit DSP. The main feature of the DSP core are listed below:

- 120 MHz operating frequency (120 MIPS)
- Fully pipelined 24 x 24 bit parallel multiplier-accumulator
- Saturation/limiting logic
- 56-bit parallel barrel shifter
- Linear, reverse carry and modulo addressing modes
- 24-bit address buses for program, X and Y data spaces and DMA
- Memory-expandible hardware stack
- Nested zero-overhead DO loops
- Fast interrupts
- Powerful JTAG emulation port
- Software wait and stop low power standby modes
- Program address tracing support
- Two 24-bit data moves in parallel with arithmetic operations
- External interrupts including non-maskable interrupt
- Interrupts may be independently masked and prioritized
- Bit-manipulation instructions can access any register or memory location
- On board support for DMA controller

6 Memories

128 K x 24-bit RAM divided into 4 areas, program RAM(PRAM), X data RAM(XRAM), Y data RAM(YRAM) and flexible allocation RAM(FLEX) as follows:

- 16 kB PRAM
- 40 kB FLEX RAM. FLEX RAM is accessed through the expansion port by the DSP core.
- External access to the FLEX RAM is also supported.
- 72 kB RAM is allocated as XRAM and YRAM. Four configurations are supported:
  - 4 kB XRAM and 68 kB YRAM
  - 8 kB XRAM and 64 kB YRAM
  - 16 kB XRAM and 56 kB YRAM
  - 24 kB XRAM and 48 kB YRAM

7 DSP peripherals

7.1 Serial audio interface (SAI)

The SAI is used to communicate between the CODEC and the DSPs.

In addition, digital audio can be directly input for processing. There is only one SAI found on the chip that can be accessed by either the DSP or the DMA controller. The main features of this block are listed below:

- Slave operating modes, all clock lines can be inputs or outputs
- Transmit and receive interrupt logic triggers on left/right data pairs
- Receive and transmit data registers have two locations to hold left and right data

7.2 Serial communication interface (SCI)

The serial communication interface provides a full duplex port for serial communication to other DSPs, microprocessors, and peripherals like modems.

The interface supports the following features:

- No additional logic for connection to other TTL level peripherals
- Asynchronous bit rates and protocols "High speed“ synchronous data transmission.
- Asynchronous protocol includes Multidrop mode for master/slave operation with wake-up on Idle line and wake-up on address bit capability, permitting the SCI to share a single line with multiple peripherals
- Transmit and receive logic can operate asynchronously from each other.
- A programmable baud-rate generator which provide the transmit and receive clocks or functions as a general purpose timer.

7.3 I^2C interface

The inter integrated-circuit bus is a simple bi-directional two-wire bus used for efficient inter IC control. All I^2C bus compatible devices incorporate an on-chip interface which allows them to communicate directly with each other via the I^2C bus.

Every component connected to the I^2C bus has it s own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and/or transmitter depending on it s functionality.

7.4 Host interface (HI)

The host interface is a system-on-chip module that permits connection to the data bus of a host processor. The HI is capable of driving 16 programmable external pins which can be configured as an 8 bit parallel port for direct connection to a host processor.

The key features of the host interface are:

- 8 bit parallel port "Full-duplex" dedicated host register bank
- Dedicated Mozart™ core DSP register core bank.
- Register banks map directly into Mozart X memory space
- 3 transfer modes:
  - host command
  - Host to Mozart core DSP
  - Mozart core DSP to host
- Access protocols:
  - Software polled
  - Interrupt
  - DMA access by the Mozart core DSP core
- 2+ wait states clock cycles per transfer
- Supported instructions:
  - Data transfer between Mozart core and external host using Mozart MOVE instruction
  - Simple I/O service routine with bit addressing instructions
  - IO service using fast interrupts with MOVEP instructions.

7.5 ESSI

The ESSI peripheral enables serial-port communication between the DSP core and external devices including Codecs, DSP, microprocessors. The ESSI is capable of driving 12 programmable external pins which can be configured as GPIO ports C and D or ESSI pins.

The key features of the ESSI are:

- Independent receiver and transmitter
- Synchronous or asynchronous channel modes synchronous. Receiver and transmitter use same clock/sync asynchronous. Receiver and transmitter may use separate clock/sync up to one transmitter enabled in asynchronous channel mode.
- Up to three transmitters enabled in synchronous channel mode.
- Normal mode. One word per period.
- Network mode. Up to 32 words per period.

7.6 EOC

The Salieri extended on-chip memory interface provides access to 40 kB of on-chip memory. The Mozart core will treat this memory as if it were external. Access by off-chip expansion bus masters is permitted. All accesses to the extended on-chip RAM are controlled by the extended on-chip memory control register. This register determines which combinations of the Address attribute pins should be interpreted as accesses to the 40 kB of RAM.

7.7 Timers and watchdog block

The timers and watchdog block consists of a common 21-bit prescaler and three independent and identical general-purpose 24-bit timer/event counters, each with its own register set.

Each timer has the following capabilities:

- Uses internal or external clocking.
- Interrupts the Mozart after a specified number of events (clocks).
- Signals an external device after counting internal events.
- Triggers DMA transfers after a specified number of events (clocks) occurs.
- Connects to the external world through designated pins TIO[0-2] for timers 0-2.

When TIO is configured as an

- Input: timer functions as an external event counter. Timer measures external pulse width/signal period.
- Output: timer functions as a:
  - Timer
  - Watchdog timer
  - Pulse-width modulator.

7.8 PLL

The PLL generates the following clocks:

- DCLK: DSP core clock
- DACLK: ADC and DAC clock
- LRCLK: left/right clock for the SAI and the CODEC
- SCLK: shift serial clock for the SAI and the CODEC

7.9 CODEC cell

The main features of the CODEC cell are listed below:

- 20 bits stereo DAC, and 18 bits ADC
- I^2S format
- Oversampling ratio: 512
- Sampling rates of 8 kHz to 48 kHz

The analog interface is in the form of differential signals for each channel. The interface on the digital side has the form of an SAI interface and can interface directly to an SAI channel and then to the DSP core.

DCLK can be supplied either by the internal PLL or by external, to allow synchronization with external anal digital sources.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

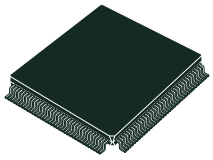
ECOPACK® is an ST trademark.

Figure 3. TQFP144 mechanical data and package dimensions

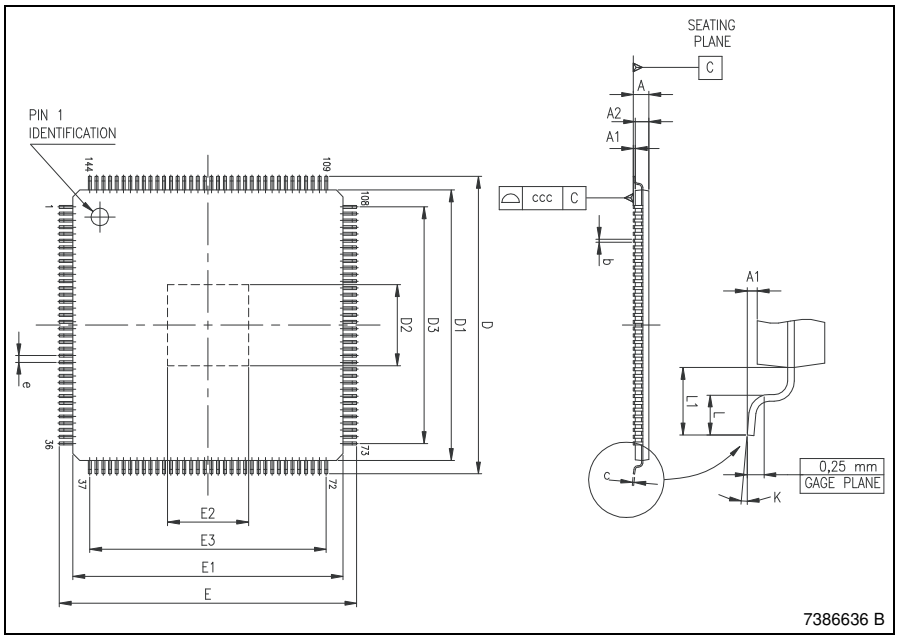
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.003		0.008
D	21.80	22.00	22.20	0.858	0.866	0.874
D1	19.80	20.00	20.20	0.779	0.787	0.795
D2	2.00			0.079		
D3		17.50			0.689	
E	21.80	22.00	22.20	0.858	0.866	0.874
E1	19.80	20.00	20.20	0.779	0.787	0.795
E2	2.00			0.079		
E3		17.50			0.689	
e		0.50			0.020	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.0393	
K	0° (min.), 3.5° (typ.), 7°(max.)					
ccc			0.08			0.03

Note 1: Exact shape of each corner is optional.

OUTLINE AND MECHANICAL DATA



TQFP144
(20x20x1.0mm exposed pad down)



9 Appendix 1

9.1 Benchmarking program

```
;********************************* FILE HEADER *********************************
;
;Title:      Salieri CODEC/SAI Functionality Test
;
;File Name:  full_func.asm
;
;Author:     --
;
;Language:   DSP2420 Core Assembler
;
;Project:    Salieri
;
;Description:        CODEC + TIMER + HI gpios + ESSI + SCI
;
;
;
;
;
;
;;
;*******************************************************************************
;********************************** Equates ************************************
;*******************************************************************************

Npts          equ     20
Ntaps         equ     4


;-------------------------------------------------------------------------
;             EQUATES for I/O Port Programming
;-------------------------------------------------------------------------

;             Register Addresses
M_HDR         EQU     $FFFFC9         ; PS- Host port GPIO data Register
M_HDDR        EQU     $FFFFC8         ; PS- Host port GPIO direction Register
M_PCRC        EQU     $FFFFBF         ; Port C Control Register
M_PRRC        EQU     $FFFFBE         ; Port C Direction Register
M_PDRC        EQU     $FFFFBD         ; Port C GPIO Data Register
M_PCRD        EQU     $FFFFAF         ; Port D Control register
M_PRRD        EQU     $FFFFAE         ; Port D Direction Data Register
M_PDRD        EQU     $FFFFAD         ; Port D GPIO Data Register
M_PCRE        EQU     $FFFF9F         ; Port E Control register
M_PRRE        EQU     $FFFF9E         ; Port E Direction Register
M_PDRE        EQU     $FFFF9D         ; Port E Data Register
M_OGDB        EQU     $FFFFFC         ; OnCE GDB Register

;-------------------------------------------------------------------------
;             EQUATES for Exception Processing
;-------------------------------------------------------------------------
; Register Addresses
IPR_C         EQU     $FFFFFF         ; Interrupt Priority Register Core
```

```
IPR_P        EQU     $FFFFFE        ; Interrupt Priority Register Peripheral

; SAI interrupt Vectors
SAI_ROF      EQU     $070           ; Receiver Overflow
SAI_TUF      EQU     $072           ; Transmitter Underflow
SAI_RDR      EQU     $074           ; Receiver Data Ready
SAI_TDE      EQU     $076           ; Transmitter Data Empty
; Timer interrupt Vector
Timer0_tcf   equ     $24            ; Timer0 Compare
Timer0_tof   equ     $26            ; Timer0 Overflow
Timer1_tcf   equ     $28            ; Timer1 Compare
Timer1_tof   equ     $2A            ; Timer1 Overflow
Timer2_tcf   equ     $2C            ; Timer2 Compare
Timer2_tof   equ     $2E            ; Timer2 Overflow
; SCI Interrupt Vectors
SCI_REC      EQU     $000050        ; SCI receive data
SCI_REC_E    EQU     $000052        ; SCI receive data with exception status
SCI_TRANS    EQU     $000054        ; SCI transmit data
SCI_IDLE     EQU     $000056        ; SCI idle line
SCI_TIMER    EQU     $000058        ; SCI timer
;;; Bit Definition for SCI_SSR
FRAMING      EQU     6


RESET        EQU     $000000        ; Reset address location

;------------------------------------------------------------------------
;            EQUATES for SAI (y memory)
;------------------------------------------------------------------------
SAI_RCS      EQU     $FFFFFF        ; SAI Receive Control/Status Register
SAI_RX2      EQU     $FFFFFE        ; SAI Channel 2 Receiver Data
SAI_RX1      EQU     $FFFFFD        ; SAI Channel 1 Receiver Data
SAI_RX0      EQU     $FFFFFC        ; SAI Channel 0 Receiver Data
SAI_TCS      EQU     $FFFFFB        ; SAI Transmit Control/Status Register
SAI_TX2      EQU     $FFFFFA        ; SAI Channel 2 Transmitter Data
SAI_TX1      EQU     $FFFFF9        ; SAI Channel 1 Transmitter Data
SAI_TX0      EQU     $FFFFF8        ; SAI Channel 0 Transmitter Data

;;; Bit Definitions for M_RCS
ROFCL        EQU     16             ; Receiver Data Overflow Clear
RDR          EQU     15             ; Receiver Data Ready
ROFL         EQU     14             ; Receiver Data Overflow
;Reserved
RXIE         EQU     12             ; Receiver Interrupt Enable
RDWJ         EQU     11             ; Receiver Data Word Justification
RREL         EQU     10             ; Receiver Relative Timing
RCKP         EQU     9              ; Receiver Clock Polarity
RLRS         EQU     8              ; Receiver Left Right Selection
RDIR         EQU     7              ; Receiver Data Shift Direction
RWL1         EQU     6              ; Receiver Word Length Control 1
RWL0         EQU     5              ; Receiver Word Length Control 0
;Reserved
RMME         EQU     3              ; Receiver Master Mode Enable
R2EN         EQU     2              ; Receiver 2 enable
R1EN         EQU     1              ; Receiver 1 enable
R0EN         EQU     0              ; Receiver 0 enable
```

```
;;; Bit Definitions for M_TCS
TUFCL       EQU     16          ; Transmitter Data Overflow Clear
TDE         EQU     15          ; Transmitter Data Ready
TUFL        EQU     14          ; Transmitter Data Overflow
;Reserved
TXIE        EQU     12          ; Transmitter Interrupt Enable
TDWE        EQU     11          ; Transmitter Data Word Justification
TREL        EQU     10          ; Transmitter Relative Timing
TCKP        EQU     9           ; Transmitter Clock Polarity
TLRS        EQU     8           ; Transmitter Left Right Selection
TDIR        EQU     7           ; Transmitter Data Shift Direction
TWL1        EQU     6           ; Transmitter Word Length Control 1
TWL0        EQU     5           ; Transmitter Word Length Control 0
;Reserved
TMME        EQU     3           ; Transmitter Master Mode Enable
T2EN        EQU     2           ; Transmitter 2 enable
T1EN        EQU     1           ; Transmitter 1 enable
T0EN        EQU     0           ; Transmitter 0 enable


;------------------------------------------------------------------------
;           EQUATES for CODEC
;------------------------------------------------------------------------
CODEC_CSR   EQU     $FFFFCB     ; CODEC Control Register Address

;;; Bit Definitions for CODEC
GADCL_0     EQU     0           ; ADC Left  Gain Bit 0
GADCL_1     EQU     1           ; ADC Left  Gain Bit 1
GADCL_2     EQU     2           ; ADC Left  Gain Bit 2
GADCR_0     EQU     3           ; ADC Right Gain Bit 0
GADCR_1     EQU     4           ; ADC Right Gain Bit 1
GADCR_2     EQU     5           ; ADC Right Gain Bit 2
GDACL_0     EQU     6           ; DAC Left  Gain Bit 0
GDACL_1     EQU     7           ; DAC Left  Gain Bit 1
GDACL_2     EQU     8           ; DAC Left  Gain Bit 2
GDACR_0     EQU     9           ; DAC Right Gain Bit 0
GDACR_1     EQU     10          ; DAC Right Gain Bit 1
GDACR_2     EQU     11          ; DAC Right Gain Bit 2
MUTEDAC     EQU     12          ; Mute DAC - Active Hi, Reset Val = 1
PDNDAC      EQU     13          ; Power down DAC - Active Hi, Reset Val = 0
PDNADC      EQU     14          ; Power down ADC - Active Hi, Reset Val = 0
N_RST       EQU     15          ; Asynchronoue Reset - Active Lo, Reset Val = 1

;------------------------------------------------------------------------
;           EQUATES for PLL
;------------------------------------------------------------------------
PLL_CSR     EQU     $FFFFD7     ; PLL Control/Status Register
PLL_FCR     EQU     $FFFFD6     ; PLL Fractional Register
PLL_CLKCTL  EQU     $FFFFD5     ; PLL Clock Control Register

;;; Bit Definitions for PLL_CSR
IDF0        EQU     0           ; Input Divide Factor 0
IDF1        EQU     1           ; Input Divide Factor 1
IDF2        EQU     2           ; Input Divide Factor 2
IDF3        EQU     3           ; Input Divide Factor 3
IDF4        EQU     4           ; Input Divide Factor 4
; Reserved
```