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# LPC3220/30/40/50

16/32-bit ARM microcontrollers; hardware floating-point coprocessor, USB On-The-Go, and EMC memory interface

Rev. 2.1 — 24 June 2014

Product data sheet

## 1. General description

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The LPC3220/30/40/50 embedded microcontrollers were designed for low power, high performance applications. NXP achieved their performance goals using a 90 nanometer process to implement an ARM926EJ-S CPU core with a vector floating point co-processor and a large set of standard peripherals including USB On-The-Go. The LPC3220/30/40/50 operates at CPU frequencies of up to 266 MHz.

The NXP implementation uses a ARM926EJ-S CPU core with a Harvard architecture, 5-stage pipeline, and an integral Memory Management Unit (MMU). The MMU provides the virtual memory capabilities needed to support the multi-programming demands of modern operating systems. The ARM926EJ-S also has a hardware based set of DSP instruction extensions, which includes single cycle MAC operations, and hardware based native Jazelle Java Byte-code execution. The NXP implementation has a 32 kB instruction cache and a 32 kB data cache.

For low power consumption, the LPC3220/30/40/50 takes advantage of NXP's advanced technology development to optimize intrinsic power and uses software controlled architectural enhancements to optimize application based power management.

The LPC3220/30/40/50 also includes 256 kB of on-chip static RAM, a NAND flash interface, an Ethernet MAC, an LCD controller that supports STN and TFT panels, and an external bus interface that supports SDR and DDR SDRAM as well as static devices. In addition, the LPC3220/30/40/50 includes a USB 2.0 full-speed interface, seven UARTs, two I<sup>2</sup>C-bus interfaces, two SPI/SSP ports, two I<sup>2</sup>S-bus interfaces, two single output PWMs, a motor control PWM, six general purpose timers with capture inputs and compare outputs, a Secure Digital (SD) interface, and a 10-bit Analog-to-Digital Converter (ADC) with a touch screen sense option.

For additional documentation, see [Section 15 "References"](#).

## 2. Features and benefits

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- ARM926EJ-S processor, running at CPU clock speeds up to 266 MHz.
- Vector Floating Point (VFP) coprocessor.
- 32 kB instruction cache and 32 kB data cache.
- Up to 256 kB of Internal SRAM (IRAM).
- Selectable boot-up from various external devices: NAND flash, SPI memory, USB, UART, or static memory.



- Multi-layer AHB system that provides a separate bus for each AHB master, including both an instruction and data bus for the CPU, two data busses for the DMA controller, and another bus for the USB controller, one for the LCD, and a final one for the Ethernet MAC. There are no arbitration delays in the system unless two masters attempt to access the same slave at the same time.
- External memory controller for DDR and SDR SDRAM as well as for static devices.
- Two NAND flash controllers: One for single-level NAND flash devices and the other for multi-level NAND flash devices.
- Master Interrupt Controller (MIC) and two Slave Interrupt Controllers (SIC), supporting 74 interrupt sources.
- Eight channel General Purpose DMA (GPDMA) controller on the AHB that can be used with the SD card port, the high-speed UARTs, I<sup>2</sup>S-bus interfaces, and SPI interfaces, as well as memory-to-memory transfers.
- Serial interfaces:
  - ◆ 10/100 Ethernet MAC with dedicated DMA Controller.
  - ◆ USB interface supporting either device, host (OHCI compliant), or On-The-Go (OTG) with an integral DMA controller and dedicated PLL to generate the required 48 MHz USB clock.
  - ◆ Four standard UARTs with fractional baud rate generation and 64 byte FIFOs. One of the standard UARTs supports IrDA.
  - ◆ Three additional high-speed UARTs intended for on-board communications that support baud rates up to 921 600 when using a 13 MHz main oscillator. All high-speed UARTs provide 64 byte FIFOs.
  - ◆ Two SPI controllers.
  - ◆ Two SSP controllers.
  - ◆ Two I<sup>2</sup>C-bus interfaces with standard open-drain pins. The I<sup>2</sup>C-bus interfaces support single master, slave, and multi-master I<sup>2</sup>C-bus configurations.
  - ◆ Two I<sup>2</sup>S-bus interfaces, each with separate input and output channels. Each channel can be operated independently on three pins, or both input and output channels can be used with only four pins and a shared clock.
- Additional peripherals:
  - ◆ LCD controller supporting both STN and TFT panels, with dedicated DMA controller. Programmable display resolution up to 1024 × 768.
  - ◆ Secure Digital (SD) memory card interface, which conforms to the *SD Memory Card Specification Version 1.01*.
  - ◆ General Purpose (GP) input, output, and I/O pins. Includes 12 GP input pins, 24 GP output pins, and 51 GP I/O pins.
  - ◆ 10-bit, 400 kHz Analog-to-Digital Converter (ADC) with input multiplexing from three pins. Optionally, the ADC can operate as a touch screen controller.
  - ◆ Real-Time Clock (RTC) with separate power pin and dedicated 32 kHz oscillator. NXP implemented the RTC in an independent on-chip power domain so it can remain active while the rest of the chip is not powered. The RTC also includes a 32-byte scratch pad memory.
  - ◆ 32-bit general purpose high-speed timer with a 16-bit pre-scaler. This timer includes one external capture input pin and a capture connection to the RTC clock. Interrupts may be generated using three match registers.

- ◆ Six enhanced timer/counters which are architecturally identical except for the peripheral base address. Two capture inputs and two match outputs are pinned out to four timers. Timer 1 brings out a third match output, timers 2 and 3 bring out all four match outputs, timer 4 has one match output, and timer 5 has no inputs or outputs.
- ◆ 32-bit millisecond timer driven from the RTC clock. This timer can generate interrupts using two match registers.
- ◆ WatchDog timer clocked by the peripheral clock.
- ◆ Two single-output PWM blocks.
- ◆ Motor control PWM.
- ◆ Keyboard scanner function allows automatic scanning of an up to 8 × 8 key matrix.
- ◆ Up to 18 external interrupts.
- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation Trace Buffer (ETB) with 2048 × 24 bit RAM allows trace via JTAG.
- Stop mode saves power while allowing many peripheral functions to restart CPU activity.
- On-chip crystal oscillator.
- An on-chip PLL allows CPU operation up to the maximum CPU rate without the requirement for a high frequency crystal. Another PLL allows operation from the 32 kHz RTC clock rather than the external crystal.
- Boundary scan for simplified board testing.
- User-accessible unique serial ID number for each chip.
- TFBGA296 package with a 15 mm × 15 mm × 0.7 mm body.

### 3. Applications

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- Consumer
- Medical
- Industrial
- Network control

## 4. Ordering information

**Table 1. Ordering information**

Type number <sup>[1]</sup>	Package		
	Name	Description	Version
LPC3220FET296/01 <sup>[2]</sup>	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3230FET296/01 <sup>[2]</sup>	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3240FET296/01 <sup>[2]</sup>	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3250FET296/01 <sup>[2]</sup>	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1

[1] F = -40 °C to +85 °C temperature range. Note that Revision "A" parts with and without the /01 suffix are identical. For example, LPC3220FET296 Revision "A" is identical to LPC3220FET296/01 Revision "A".

[2] Available starting with Revision "A".

### 4.1 Ordering options

**Table 2. Part options**

Type number	SRAM (kB)	10/100 Ethernet	LCD controller	Temperature range (°C)	Package
LPC3220FET296/01	128	0	0	-40 to +85	TFBGA296
LPC3230FET296/01	256	0	1	-40 to +85	TFBGA296
LPC3240FET296/01	256	1	0	-40 to +85	TFBGA296
LPC3250FET296/01	256	1	1	-40 to +85	TFBGA296

5. Block diagram

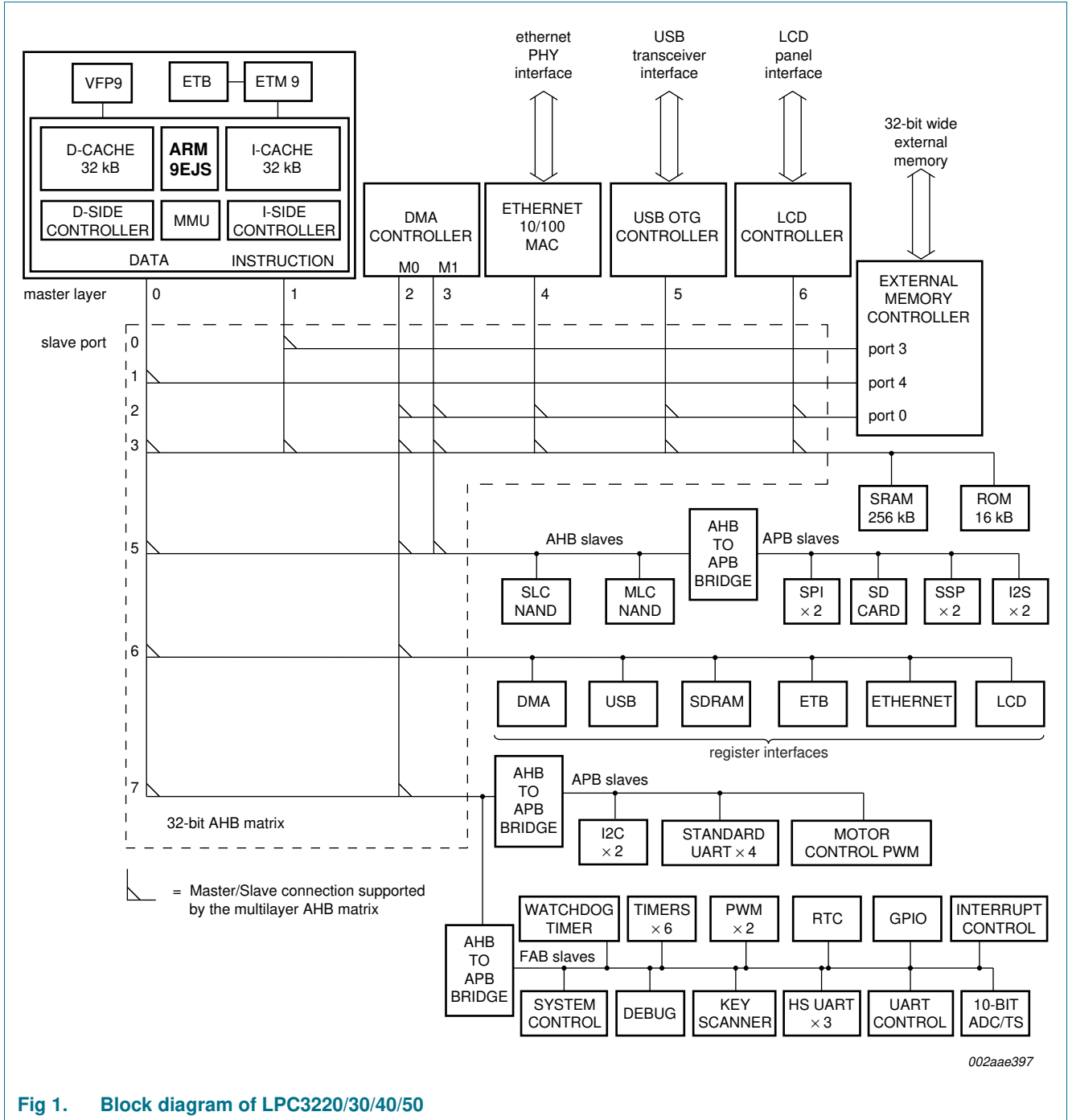


Fig 1. Block diagram of LPC3220/30/40/50

## 6. Pinning information

### 6.1 Pinning

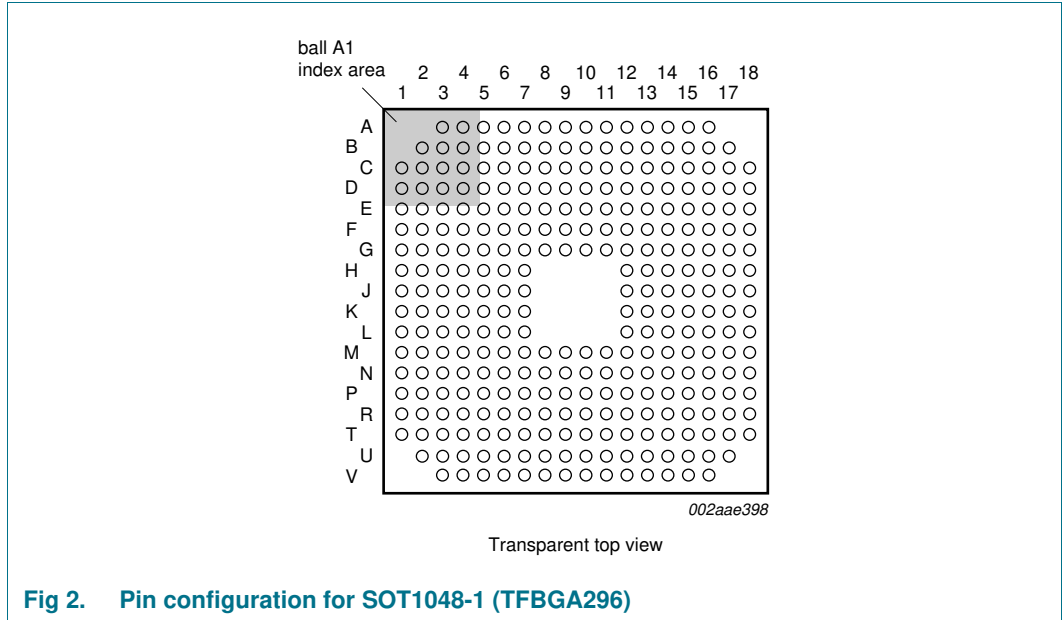


Fig 2. Pin configuration for SOT1048-1 (TFBGA296)

Table 3. Pin allocation table (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
<b>Row A</b>					
				A3	I2C2_SCL
A4	I2S1TX_CLK/MAT3[0]	A5	I2C1_SCL	A6	MS_BS/MAT2[1]
A7	MS_DIO1/MAT0[1]	A8	MS_DIO0/MAT0[0]	A9	SPI2_DATIO/MOSI1/LCDVD[20] <sup>[1]</sup>
A10	SPI2_DATIN/MISO1/LCDVD[21] <sup>[1]</sup> /GPI_27	A11	GPIO_1	A12	GPIO_0
A13	GPO_21/U4_TX/LCDVD[3] <sup>[1]</sup>	A14	GPO_15/MCOA1/LCDDFP <sup>[1]</sup>	A15	GPO_7/LCDVD[2] <sup>[1]</sup>
A16	GPO_6/LCDVD[18] <sup>[1]</sup>				
<b>Row B</b>					
		B2	GPO_20	B3	GPO_5
B4	I2S1TX_WS/CAP3[0]	B5	P0[0]/I2S1RX_CLK	B6	I2C1_SDA
B7	MS_SCLK/MAT2[0]	B8	MS_DIO2/MAT0[2]	B9	SPI1_DATIO/MOSI0/MCI2
B10	SPI2_CLK/SCK1/LCDVD[23] <sup>[1]</sup>	B11	GPIO_4/SSEL1/LCDVD[22] <sup>[1]</sup>	B12	GPO_12/MCOA2/LCDDLE <sup>[1]</sup>
B13	GPO_13/MCOB1/LCDDCLK <sup>[1]</sup>	B14	GPO_2/MAT1[0]/LCDVD[0] <sup>[1]</sup>	B15	GPI_19/U4_RX
B16	GPI_8/KEY_COL6/SPI2_BUSY/ENET_RX_DV <sup>[2]</sup>	B17	n.c.		
<b>Row C</b>					
C1	FLASH_RD	C2	GPO_19	C3	GPO_0/TST_CLK1
C4	USB_ATX_INT	C5	USB_SE0_VM/U5_TX	C6	TST_CLK2
C7	GPI_6/HSTIM_CAP/ENET_RXD2 <sup>[2]</sup>	C8	MS_DIO3/MAT0[3]	C9	SPI1_CLK/SCK0

Table 3. Pin allocation table (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
C10	SPI1_DATIN/MISO0/GPI_25/MCI1	C11	GPIO_3/KEY_ROW7/ENET_MDIO <sup>[2]</sup>	C12	GPO_9/LCDVD[9] <sup>[1]</sup>
C13	GPO_8/LCDVD[8] <sup>[1]</sup>	C14	GPI_2/CAP2[0]/ENET_RXD3 <sup>[2]</sup>	C15	GPI_1/ <u>SERVICE</u>
C16	GPI_0/I2S1RX_SDA	C17	KEY_ROW4/ENET_TXD0 <sup>[2]</sup>	C18	KEY_ROW5/ENET_TXD1 <sup>[2]</sup>
<b>Row D</b>					
D1	FLASH_RDY	D2	FLASH_ALE	D3	GPO_14
D4	GPO_1	D5	USB_DAT_VP/U5_RX	D6	<u>USB_OE_TP</u>
D7	P0[1]/I2S1RX_WS	D8	GPO_4	D9	GPIO_2/KEY_ROW6/ENET_MDC <sup>[2]</sup>
D10	GPO_16/MCOB0/LCDENAB <sup>[1]</sup> /LCDM <sup>[1]</sup>	D11	GPO_18/MCOA0/LCDLP <sup>[1]</sup>	D12	GPO_3/LCDVD[1] <sup>[1]</sup>
D13	GPI_7/CAP4[0]/ <u>MCABORT</u>	D14	PWM_OUT1/LCDVD[16] <sup>[1]</sup>	D15	PWM_OUT2/INTSTAT/LCDVD[19] <sup>[1]</sup>
D16	KEY_ROW3/ENET_TX_EN <sup>[2]</sup>	D17	KEY_COL2/ENET_RX_ER <sup>[2]</sup>	D18	KEY_COL3/ENET_CRSD <sup>[2]</sup>
<b>Row E</b>					
E1	FLASH_IO[3]	E2	FLASH_IO[7]	E3	<u>FLASH_CE</u>
E4	I2C2_SDA	E5	USB_I2C_SCL	E6	USB_I2C_SDA
E7	I2S1TX_SDA/MAT3[1]	E8	GPO_11	E9	GPIO_5/SSEL0/MCI0
E10	GPO_22/U7_HRTS/LCDVD[14] <sup>[1]</sup>	E11	GPO_10/MCOB2/LCDPWR <sup>[1]</sup>	E12	GPI_9/KEY_COL7/ENET_COL <sup>[2]</sup>
E13	GPI_4/SPI1_BUSY	E14	KEY_ROW1/ENET_TXD2 <sup>[2]</sup>	E15	KEY_ROW0/ENET_TX_ER <sup>[2]</sup>
E16	KEY_COL1/ENET_RX_CLK <sup>[2]</sup> /ENET_REF_CLK <sup>[2]</sup>	E17	U7_RX/CAP0[0]/LCDVD[10] <sup>[1]</sup> /GPI_23	E18	U7_TX/MAT1[1]/LCDVD[11] <sup>[1]</sup>
<b>Row F</b>					
F1	FLASH_IO[2]	F2	<u>FLASH_WR</u>	F3	FLASH_CLE
F4	GPI_3	F5	VSS_IOC	F6	VSS_IOB
F7	VDD_IOC	F8	VDD_IOB	F9	VDD_IOD
F10	VSS_IOD	F11	VSS_IOD	F12	VSS_IOD
F13	VDD_IOD	F14	KEY_ROW2/ENET_TXD3 <sup>[2]</sup>	F15	KEY_COL0/ENET_TX_CLK <sup>[2]</sup>
F16	KEY_COL5/ENET_RXD1 <sup>[2]</sup>	F17	U6_IRRX/GPI_21	F18	U5_RX/GPI_20
<b>Row G</b>					
G1	<u>EMC_DYCS1</u>	G2	FLASH_IO[5]	G3	FLASH_IO[6]
G4	<u>RESOUT</u>	G5	VSS_IOC	G6	VDD_IOC
G7	VDD_CORE	G8	VSS_CORE	G9	VDD_CORE
G10	VSS_CORE	G11	VDD_CORE	G12	VSS_CORE
G13	U7_HCTS/CAP0[1]/LCDCLKIN <sup>[1]</sup> /GPI_22	G14	DBGEN	G15	KEY_COL4/ENET_RXD0 <sup>[2]</sup>
G16	U6_IRTX	G17	SYSCLKEN/LCDVD[15] <sup>[1]</sup>	G18	JTAG_TMS
<b>Row H</b>					
H1	<u>EMC_OE</u>	H2	FLASH_IO[0]	H3	FLASH_IO[1]
H4	FLASH_IO[4]	H5	VSS_IOC	H6	VDD_IOC
H7	VSS_CORE				
				H12	VSS_IOD
H13	VDD_IOA	H14	JTAG_TCK	H15	U5_TX



Table 3. Pin allocation table (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
H16	HIGHCORE/LCDVD[17] <a href="#">[1]</a>	H17	JTAG_NTRST	H18	JTAG_RTCK
<b>Row J</b>					
J1	EMC_A[20]/P1[20]	J2	EMC_A[21]/P1[21]	J3	EMC_A[22]/P1[22]
J4	EMC_A[23]/P1[23]	J5	VDD_IOC	J6	VDD_EMCC
J7	VDD_CORE				
				J12	VDD_CORE
J13	VDD_IOA	J14	U3_RX/GPI_18	J15	JTAG_TDO
J16	JTAG_TDI	J17	U3_TX	J18	U2_HCTS/U3_CTS/GPI_16
<b>Row K</b>					
K1	EMC_A[19]/P1[19]	K2	EMC_A[18]/P1[18]	K3	EMC_A[16]/P1[16]
K4	EMC_A[17]/P1[17]	K5	VSS_EMCC	K6	VDD_EMCC
K7	VDD_EMCC				
				K12	VSS_CORE
K13	VSS_IOA	K14	VDD_RTC	K15	U1_RX/CAP1[0]/GPI_15
K16	U1_TX	K17	U2_TX/U3_DTR	K18	U2_RX/U3_DSR/GPI_17
<b>Row L</b>					
L1	EMC_A[15]/P1[15]	L2	EMC_CKE1	L3	EMC_A[0]/P1[0]
L4	EMC_A[1]/P1[1]	L5	VSS_EMCC	L6	VDD_EMCC
L7	VSS_CORE				
				L12	VDD_COREFXD
L13	VDD_RTCCORE	L14	VSS_RTCCORE	L15	P0[4]/I2S0RX_WS/LCDVD[6] <a href="#">[1]</a>
L16	P0[5]/I2S0TX_SDA/LCDVD[7] <a href="#">[1]</a>	L17	P0[6]/I2S0TX_CLK/LCDVD[12] <a href="#">[1]</a>	L18	P0[7]/I2S0TX_WS/LCDVD[13] <a href="#">[1]</a>
<b>Row M</b>					
M1	EMC_A[2]/P1[2]	M2	EMC_A[3]/P1[3]	M3	EMC_A[4]/P1[4]
M4	EMC_A[8]/P1[8]	M5	VSS_EMCC	M6	VDD_EMCC
M7	VDD_CORE	M8	VDD_EMCC	M9	VSS_CORE
M10	VSS_CORE	M11	VDD_CORE	M12	VSS_CORE
M13	VDD_COREFXD	M14	RESET	M15	ONSW
M16	GPO_23/U2_HRTS/U3_RTS	M17	P0[2]/I2S0RX_SDA/LCDVD[4] <a href="#">[1]</a>	M18	P0[3]/I2S0RX_CLK/LCDVD[5] <a href="#">[1]</a>
<b>Row N</b>					
N1	EMC_A[5]/P1[5]	N2	EMC_A[6]/P1[6]	N3	EMC_A[7]/P1[7]
N4	EMC_A[12]/P1[12]	N5	VSS_EMCC	N6	VSS_EMCC
N7	VDD_EMCC	N8	VDD_EMCC	N9	VDD_EMCC
N10	VDD_EMCC	N11	VDD_EMCC	N12	VDD_AD
N13	VDD_AD	N14	VDD_FUSE	N15	VDD_RTCOSC
N16	GPI_5/U3_DCD	N17	GPI_28/U3_RI	N18	GPO_17
<b>Row P</b>					
P1	EMC_A[9]/P1[9]	P2	EMC_A[10]/P1[10]	P3	EMC_A[11]/P1[11]
P4	EMC_DQM[1]	P5	EMC_DQM[3]	P6	VSS_EMCC

Table 3. Pin allocation table (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
P7	VSS_EMC	P8	VSS_EMC	P9	VSS_EMC
P10	VSS_EMC	P11	VSS_EMC	P12	EMC_BLS[3]
P13	VSS_AD	P14	VSS_OSC	P15	VDD_PLLUSB
P16	RTCX_IN	P17	RTCX_OUT	P18	VSS_RTCOSC
<b>Row R</b>					
R1	EMC_A[13]/P1[13]	R2	EMC_A[14]/P1[14]	R3	EMC_DQM[0]
R4	EMC_WR	R5	EMC_CAS	R6	EMC_DYCS0
R7	EMC_D[1]	R8	EMC_D[7]	R9	EMC_D[17]/EMC_DQS1
R10	EMC_D[24]/P2[5]	R11	EMC_CS1	R12	EMC_BLS[2]
R13	TS_XP	R14	PLL397_LOOP	R15	SYSX_OUT
R16	VSS_PLLUSB	R17	VDD_PLLHCLK	R18	VSS_PLLHCLK
<b>Row T</b>					
T1	EMC_DQM[2]	T2	EMC_RAS	T3	EMC_CLK
T4	EMC_CLKIN	T5	EMC_D[2]	T6	EMC_D[6]
T7	EMC_D[11]	T8	EMC_D[14]	T9	EMC_D[20]/P2[1]
T10	EMC_D[23]/P2[4]	T11	EMC_D[27]/P2[8]	T12	EMC_CS2
T13	EMC_BLS[1]	T14	ADIN1/TS_XM	T15	VSS_PLL397
T16	VDD_PLL397	T17	SYSX_IN	T18	VDD_OSC
<b>Row U</b>					
		U2	n.c.	U3	EMC_CKE0
U4	EMC_D[0]	U5	EMC_D[3]	U6	EMC_D[9]
U7	EMC_D[12]	U8	EMC_D[15]	U9	EMC_D[19]/P2[0]
U10	EMC_D[22]/P2[3]	U11	EMC_D[26]/P2[7]	U12	EMC_D[30]/P2[11]
U13	EMC_CS0	U14	EMC_BLS[0]	U15	ADIN0/TS_YM
U16	TS_YP	U17	n.c.		
<b>Row V</b>					
				V3	EMC_D[4]
V4	EMC_D[5]	V5	EMC_D[8]	V6	EMC_D[10]
V7	EMC_D[13]	V8	EMC_D[16]/EMC_DQS0	V9	EMC_D[18]/EMC_CLK
V10	EMC_D[21]/P2[2]	V11	EMC_D[25]/P2[6]	V12	EMC_D[28]/P2[9]
V13	EMC_D[29]/P2[10]	V14	EMC_D[31]/P2[12]	V15	EMC_CS3
V16	ADIN2/TS_AUX_IN				

[1] LCD on LPC3230 and LPC3250 only.

[2] Ethernet on LPC3240 and LPC3250 only.

## 6.2 Pin description

Table 4. Pin description

Symbol	Pin	Power supply domain	Type	Description
ADIN0/TS_YM	U15	VDD_AD	analog in	ADC input 0/touch screen Y minus
ADIN1/TS_XM	T14	VDD_AD	analog in	ADC input 0/touch screen X minus
ADIN2/TS_AUX_IN	V16	VDD_AD	analog in	ADC input 2/touch screen AUX input
DBGEN	G14	VDD_IOD	I: PD	Device test input LOW = JTAG in-circuit debug available; normal operation. HIGH = I/O cell boundary scan test; for board assembly BSDL test.
EMC_A[0]/P1[0]	L3	VDD_EMC	I/O	EMC address bit 0
			I/O	Port 1 GPIO bit 0
EMC_A[1]/P1[1]	L4	VDD_EMC	I/O	EMC address bit 1
			I/O	Port 1 GPIO bit 1
EMC_A[2]/P1[2]	M1	VDD_EMC	I/O	EMC address bit 2
			I/O	Port 1 GPIO bit 2
EMC_A[3]/P1[3]	M2	VDD_EMC	I/O	EMC address bit 3
			I/O	Port 1 GPIO bit 3
EMC_A[4]/P1[4]	M3	VDD_EMC	I/O	EMC address bit 4
			I/O	Port 1 GPIO bit 4
EMC_A[5]/P1[5]	N1	VDD_EMC	I/O	EMC address bit 5
			I/O	Port 1 GPIO bit 5
EMC_A[6]/P1[6]	N2	VDD_EMC	I/O	EMC address bit 6
			I/O	Port 1 GPIO bit 6
EMC_A[7]/P1[7]	N3	VDD_EMC	I/O	EMC address bit 7
			I/O	Port 1 GPIO bit 7
EMC_A[8]/P1[8]	M4	VDD_EMC	I/O	EMC address bit 8
			I/O	Port 1 GPIO bit 8
EMC_A[9]/P1[9]	P1	VDD_EMC	I/O	EMC address bit 9
			I/O	Port 1 GPIO bit 9
EMC_A[10]/P1[10]	P2	VDD_EMC	I/O	EMC address bit 10
			I/O	Port 1 GPIO bit 10
EMC_A[11]/P1[11]	P3	VDD_EMC	I/O	EMC address bit 11
			I/O	Port 1 GPIO bit 11
EMC_A[12]/P1[12]	N4	VDD_EMC	I/O	EMC address bit 12
			I/O	Port 1 GPIO bit 12
EMC_A[13]/P1[13]	R1	VDD_EMC	I/O	EMC address bit 13
			I/O	Port 1 GPIO bit 13
EMC_A[14]/P1[14]	R2	VDD_EMC	I/O	EMC address bit 14
			I/O	Port 1 GPIO bit 14

Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
EMC_A[15]/P1[15]	L1	VDD_EMC	I/O	EMC address bit 15
			I/O	Port 1 GPIO bit 15
EMC_A[16]/P1[16]	K3	VDD_EMC	I/O	EMC address bit 16
			I/O	Port 1 GPIO bit 16
EMC_A[17]/P1[17]	K4	VDD_EMC	I/O	EMC address bit 17
			I/O	Port 1 GPIO bit 17
EMC_A[18]/P1[18]	K2	VDD_EMC	I/O	EMC address bit 18
			I/O	Port 1 GPIO bit 18
EMC_A[19]/P1[19]	K1	VDD_EMC	I/O	EMC address bit 19
			I/O	Port 1 GPIO bit 19
EMC_A[20]/P1[20]	J1	VDD_EMC	I/O	EMC address bit 20
			I/O	Port 1 GPIO bit 20
EMC_A[21]/P1[21]	J2	VDD_EMC	I/O	EMC address bit 21
			I/O	Port 1 GPIO bit 21
EMC_A[22]/P1[22]	J3	VDD_EMC	I/O	EMC address bit 22
			I/O	Port 1 GPIO bit 22
EMC_A[23]/P1[23]	J4	VDD_EMC	I/O	EMC address bit 23
			I/O	Port 1 GPIO bit 23
EMC_BLS[0]	U14	VDD_EMC	O	Static memory byte lane 0 select
EMC_BLS[1]	T13	VDD_EMC	O	Static memory byte lane 1 select
EMC_BLS[2]	R12	VDD_EMC	O	Static memory byte lane 2 select
EMC_BLS[3]	P12	VDD_EMC	O	Static memory byte lane 3 select
$\overline{\text{EMC\_CAS}}$	R5	VDD_EMC	O	SDRAM column address strobe out, active LOW
EMC_CKE0	U3	VDD_EMC	O	Clock enable out for SDRAM bank 0
EMC_CKE1	L2	VDD_EMC	O	Clock enable out for SDRAM bank 1
EMC_CLK	T3	VDD_EMC	O	SDRAM clock out
EMC_CLKIN	T4	VDD_EMC	I	SDRAM clock feedback
$\overline{\text{EMC\_CS0}}$	U13	VDD_EMC	O	EMC static memory chip select 0
$\overline{\text{EMC\_CS1}}$	R11	VDD_EMC	O	EMC static memory chip select 1
$\overline{\text{EMC\_CS2}}$	T12	VDD_EMC	O	EMC static memory chip select 2
$\overline{\text{EMC\_CS3}}$	V15	VDD_EMC	O	EMC static memory chip select 3
EMC_D[0]	U4	VDD_EMC	I/O: BK	EMC data bit 0
EMC_D[1]	R7	VDD_EMC	I/O: BK	EMC data bit 1
EMC_D[2]	T5	VDD_EMC	I/O: BK	EMC data bit 2
EMC_D[3]	U5	VDD_EMC	I/O: BK	EMC data bit 3
EMC_D[4]	V3	VDD_EMC	I/O: BK	EMC data bit 4
EMC_D[5]	V4	VDD_EMC	I/O: BK	EMC data bit 5
EMC_D[6]	T6	VDD_EMC	I/O: BK	EMC data bit 6
EMC_D[7]	R8	VDD_EMC	I/O: BK	EMC data bit 7
EMC_D[8]	V5	VDD_EMC	I/O: BK	EMC data bit 8

Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
EMC_D[9]	U6	VDD_EMC	I/O: BK	EMC data bit 9
EMC_D[10]	V6	VDD_EMC	I/O: BK	EMC data bit 10
EMC_D[11]	T7	VDD_EMC	I/O: BK	EMC data bit 11
EMC_D[12]	U7	VDD_EMC	I/O: BK	EMC data bit 12
EMC_D[13]	V7	VDD_EMC	I/O: BK	EMC data bit 13
EMC_D[14]	T8	VDD_EMC	I/O: BK	EMC data bit 14
EMC_D[15]	U8	VDD_EMC	I/O: BK	EMC data bit 15
EMC_D[16]/ EMC_DQS0	V8	VDD_EMC	I/O: BK	EMC data bit 16
			I/O: BK	DDR data strobe 0
EMC_D[17]/ EMC_DQS1	R9	VDD_EMC	I/O: BK	EMC data bit 17
			I/O: BK	DDR data strobe 1
EMC_D[18]/ EMC_CLK	V9	VDD_EMC	I/O: P	EMC data bit 18
			I/O: P	DDR inverted clock output
EMC_D[19]/P2[0]	U9	VDD_EMC	I/O: P	EMC data bit 19
			I/O: P	Port 2 GPIO bit 0
EMC_D[20]/P2[1]	T9	VDD_EMC	I/O: P	EMC data bit 20
			I/O: P	Port 2 GPIO bit 1
EMC_D[21]/P2[2]	V10	VDD_EMC	I/O: P	EMC data bit 21
			I/O: P	Port 2 GPIO bit 2
EMC_D[22]/P2[3]	U10	VDD_EMC	I/O: P	EMC data bit 22
			I/O: P	Port 2 GPIO bit 3
EMC_D[23]/P2[4]	T10	VDD_EMC	I/O: P	EMC data bit 23
			I/O: P	Port 2 GPIO bit 4
EMC_D[24]/P2[5]	R10	VDD_EMC	I/O: P	EMC data bit 24
			I/O: P	Port 2 GPIO bit 5
EMC_D[25]/P2[6]	V11	VDD_EMC	I/O: P	EMC data bit 25
			I/O: P	Port 2 GPIO bit 6
EMC_D[26]/P2[7]	U11	VDD_EMC	I/O: P	EMC data bit 26
			I/O: P	Port 2 GPIO bit 7
EMC_D[27]/P2[8]	T11	VDD_EMC	I/O: P	EMC data bit 27
			I/O: P	Port 2 GPIO bit 8
EMC_D[28]/P2[9]	V12	VDD_EMC	I/O: P	EMC data bit 28
			I/O: P	Port 2 GPIO bit 9
EMC_D[29]/P2[10]	V13	VDD_EMC	I/O: P	EMC data bit 29
			I/O: P	Port 2 GPIO bit 10
EMC_D[30]/P2[11]	U12	VDD_EMC	I/O: P	EMC data bit 30
			I/O: P	Port 2 GPIO bit 11
EMC_D[31]/P2[12]	V14	VDD_EMC	I/O: P	EMC data bit 31
			I/O: P	Port 2 GPIO bit 12
EMC_DQM[0]	R3	VDD_EMC	O	SDRAM data mask 0 out

Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
EMC_DQM[1]	P4	VDD_EMC	O	SDRAM data mask 1 out
EMC_DQM[2]	T1	VDD_EMC	O	SDRAM data mask 2 out
EMC_DQM[3]	P5	VDD_EMC	O	SDRAM data mask 3 out
EMC_DYCS0	R6	VDD_EMC	O	SDRAM active LOW chip select 0
EMC_DYCS1	G1	VDD_EMC	O	SDRAM active LOW chip select 1
EMC_OE	H1	VDD_EMC	O	EMC static memory output enable
EMC_RAS	T2	VDD_EMC	O	SDRAM row address strobe, active LOW
EMC_WR	R4	VDD_EMC	O	EMC write strobe, active LOW
FLASH_ALE	D2	VDD_IOC	O	Flash address latch enable
FLASH_CE	E3	VDD_IOC	O	Flash chip enable
FLASH_CLE	F3	VDD_IOC	O	Flash command latch enable
FLASH_IO[0]	H2	VDD_IOC	I/O: BK	Flash data bus, bit 0
FLASH_IO[1]	H3	VDD_IOC	I/O: BK	Flash data bus, bit 1
FLASH_IO[2]	F1	VDD_IOC	I/O: BK	Flash data bus, bit 2
FLASH_IO[3]	E1	VDD_IOC	I/O: BK	Flash data bus, bit 3
FLASH_IO[4]	H4	VDD_IOC	I/O: BK	Flash data bus, bit 4
FLASH_IO[5]	G2	VDD_IOC	I/O: BK	Flash data bus, bit 5
FLASH_IO[6]	G3	VDD_IOC	I/O: BK	Flash data bus, bit 6
FLASH_IO[7]	E2	VDD_IOC	I/O: BK	Flash data bus, bit 7
FLASH_RD	C1	VDD_IOC	O	Flash read enable
FLASH_RDY	D1	VDD_IOC	I	Flash ready (from flash device)
FLASH_WR	F2	VDD_IOC	O	Flash write enable
GPI_0/I2S1RX_SDA	C16	VDD_IOD	I	General purpose input 0
			I	I <sup>2</sup> S1 Receive data
GPI_1/SERVICE	C15	VDD_IOD	I	General purpose input 1
			I	Boot select input
GPI_2/CAP2[0]/ENET_RXD3	C14	VDD_IOD	I	General purpose input 2
			I	Timer 2 capture input 0
			I	Ethernet receive data 3 (LPC3240 and LPC3250 only)
GPI_3	F4	VDD_IOC	I	General purpose input 3
GPI_4/SPI1_BUSY	E13	VDD_IOD	I	General purpose input 4
			I	SPI1 busy input
GPI_5/U3_DCD	N16	VDD_IOA	I	General purpose input 5
			I	UART 3 data carrier detect input
GPI_6/HSTIM_CAP/ENET_RXD2	C7	VDD_IOB	I: BK	General purpose input 6
			I: BK	High-speed timer capture input
			I: BK	Ethernet receive data 2 (LPC3240 and LPC3250 only)

Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
GPI_7/CAP4[0]/ MCABORT	D13	VDD_IOD	I	General purpose input 7
			I	Timer 4 capture input 0
			I	Motor control PWM LOW-active fast abort input
GPI_8/KEY_COL6/ SPI2_BUSY/ ENET_RX_DV	B16	VDD_IOD	I	General purpose input 8
			I	Keyscan column 6 input
			I	SPI2 busy input
			I	Ethernet receive data valid input (LPC3240 and LPC3250 only)
GPI_9/KEY_COL7/ ENET_COL	E12	VDD_IOD	I	General purpose input 9
			I	Keyscan column 7 input
			I	Ethernet collision input (LPC3240 and LPC3250 only)
GPI_19/U4_RX	B15	VDD_IOD	I	General purpose input 19
			I	UART 4 receive
GPI_28/U3_RI	N17	VDD_IOA	I	General purpose input 28
			I	UART 3 ring indicator input
GPIO_0	A12	VDD_IOD	I/O	General purpose input/output 0
GPIO_1	A11	VDD_IOD	I/O	General purpose input/output 1
GPIO_2/ KEY_ROW6/ ENET_MDC	D9	VDD_IOD	I/O	General purpose input/output 2
			O	Keyscan row 6 output
			O	Ethernet PHY interface clock (LPC3240 and LPC3250 only)
GPIO_3/ KEY_ROW7/ ENET_MDIO	C11	VDD_IOD	I/O	General purpose input/output 3
			I/O	Keyscan row 7 output
			I/O	Ethernet PHY interface data (LPC3240 and LPC3250 only)
GPIO_4/ SSEL1/ LCDVD[22]	B11	VDD_IOD	I/O	General purpose input/output 4
			I/O	SSP1 Slave Select
			I/O	LCD data bit 22 (LPC3230 and LPC3250 only)
GPIO_5/ SSEL0/ MCIO	E9	VDD_IOD	I/O	General purpose input/output 5
			I/O	SSP0 Slave Select
			I/O	Motor control channel 0 input
GPO_0/ TST_CLK1	C3	VDD_IOC	O	General purpose output 0
			O	Test clock 1 out
GPO_1	D4	VDD_IOC	O	General purpose output 1
GPO_2/ MAT1[0]/ LCDVD[0]	B14	VDD_IOD	O	General purpose output 2
			O	Timer 1 match output 0
			O	LCD data bit 0 (LPC3230 and LPC3250 only)
GPO_3/ LCDVD[1]	D12	VDD_IOD	O	General purpose output 3
			O	LCD data bit 1 (LPC3230 and LPC3250 only)
GPO_4	D8	VDD_IOB	O	General purpose output 4

Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
GPO_5	B3	VDD_IOC	O	General purpose output 5
GPO_6/ LCDVD[18]	A16	VDD_IOD	O	General purpose output 6
			O	LCD data bit 18 (LPC3230 and LPC3250 only)
GPO_7/ LCDVD[2]	A15	VDD_IOD	O	General purpose output 7
			O	LCD data bit 2 (LPC3230 and LPC3250 only)
GPO_8/ LCDVD[8]	C13	VDD_IOD	O	General purpose output 8
			O	LCD data bit 8 (LPC3230 and LPC3250 only)
GPO_9/ LCDVD[9]	C12	VDD_IOD	O	General purpose output 9
			O	LCD data bit 9 (LPC3230 and LPC3250 only)
GPO_10/ MCOB2/ LCDPWR	E11	VDD_IOD	O	General purpose output 10
			O	Motor control PWM channel 2, output B
			O	LCD panel power enable (LPC3230 and LPC3250 only)
GPO_11	E8	VDD_IOB	O	General purpose output 11
GPO_12/ MCOA2/ LCDLE	B12	VDD_IOD	O	General purpose output 12
			O	Motor control PWM channel 2, output A
			O	LCD line end signal (LPC3230 and LPC3250 only)
GPO_13/ MCOB1/ LCDDCLK	B13	VDD_IOD	O	General purpose output 13
			O	Motor control PWM channel 1, output B
			O	LCD clock output (LPC3230 and LPC3250 only)
GPO_14	D3	VDD_IOC	O	General purpose output 14
GPO_15/ MCOA1/ LCDFP	A14	VDD_IOD	O	General purpose output 15
			O	Motor control PWM channel 1, output A
			O	LCD frame/sync pulse (LPC3230 and LPC3250 only)
GPO_16/ MCOB0/ LCDENAB/LCDM	D10	VDD_IOD	O	General purpose output 16
			O	Motor control PWM channel 0, output B
			O	LCD STN AC bias/TFT data enable (LPC3230 and LPC3250 only)
GPO_17	N18	VDD_IOA	O	General purpose output 17
GPO_18/ MCOA0/ LCDLP	D11	VDD_IOD	O	General purpose output 18
			O	Motor control PWM channel 0, output A
			O	LCD line sync/horizontal sync (LPC3230 and LPC3250 only)
GPO_19	C2	VDD_IOC	O	General purpose output 19
GPO_20	B2	VDD_IOC	O	General purpose output 20
GPO_21/ U4_TX/ LCDVD[3]	A13	VDD_IOD	O	General purpose output 21
			O	UART 4 transmit
			O	LCD data bit 3 (LPC3230 and LPC3250 only)



Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
GPO_22/ U7_HRTS/ LCDVD[14]	E10	VDD_IOD	O	General purpose output 22
			O	HS UART 7 RTS out
			O	LCD data bit 14 (LPC3230 and LPC3250 only)
GPO_23/ U2_HRTS/ U3_RTS	M16	VDD_IOA	O	General purpose output 23
			O	HS UART 2 RTS out
			O	UART 3 RTS out
HIGHCORE/ LCDVD[17]	H16	VDD_IOD	O	Core voltage control out
			O	LCD data bit 17 (LPC3230 and LPC3250 only)
I2C1_SCL	A5	VDD_IOB	I/O T	I <sup>2</sup> C1 serial clock input/output
I2C1_SDA	B6	VDD_IOB	I/O T	I <sup>2</sup> C1 serial data input/output
I2C2_SCL	A3	VDD_IOC	I/O T	I <sup>2</sup> C2 serial clock input/output
I2C2_SDA	E4	VDD_IOC	I/O T	I <sup>2</sup> C2 serial data input/output
I2S1TX_CLK/ MAT3[0]	A4	VDD_IOB	I/O	I <sup>2</sup> S1 transmit clock
			O	Timer 3 match output 0
I2S1TX_SDA/ MAT3[1]	E7	VDD_IOB	I/O	I <sup>2</sup> S1 transmit data
			O	Timer 3 match output 1
I2S1TX_WS/ CAP3[0]	B4	VDD_IOB	I/O	I <sup>2</sup> S1 transmit word select
			I/O	Timer 3 capture input 0
JTAG_NTRST	H17	VDD_IOD	I: PU	JTAG1 reset input. Must be LOW during power-on reset. See <a href="#">Section 12.1 “Connecting the JTAG_NTRST pin”</a> .
JTAG_RTCK	H18	VDD_IOD	O	JTAG1 return clock out
JTAG_TCK	H14	VDD_IOD	I	JTAG1 clock input
JTAG_TDI	J16	VDD_IOD	I: PU	JTAG1 data input
JTAG_TDO	J15	VDD_IOD	O	JTAG1 data out
JTAG_TMS	G18	VDD_IOD	I: PU	JTAG1 test mode select input
KEY_COL0/ ENET_TX_CLK	F15	VDD_IOD	I	Keyscan column 0 input
			I	Ethernet transmit clock (LPC3240 and LPC3250 only)
KEY_COL1/ ENET_RX_CLK/ ENET_REF_CLK	E16	VDD_IOD	I	Keyscan column 1 input
			I	Ethernet receive clock (MII mode, LPC3240 and LPC3250 only)
			I	Ethernet reference clock (RMII mode, LPC3240 and LPC3250 only)
KEY_COL2/ ENET_RX_ER	D17	VDD_IOD	I	Keyscan column 2 input
			I	Ethernet receive error input (LPC3240 and LPC3250 only)
KEY_COL3/ ENET_CRIS	D18	VDD_IOD	I	Keyscan column 3 input
			I	Ethernet carrier sense input (LPC3240 and LPC3250 only)

Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
KEY_COL4/ ENET_RXD0	G15	VDD_IOD	I	Keyscan column 4 input
			I	Ethernet receive data 0 (LPC3240 and LPC3250 only)
KEY_COL5/ ENET_RXD1	F16	VDD_IOD	I	Keyscan column 5 input
			I	Ethernet receive data 1 (LPC3240 and LPC3250 only)
KEY_ROW0/ ENET_TX_ER	E15	VDD_IOD	I/O T	Keyscan row 0 out
			I/O T	Ethernet transmit error (LPC3240 and LPC3250 only)
KEY_ROW1/ ENET_TXD2	E14	VDD_IOD	I/O T	Keyscan row 1 out
			I/O T	Ethernet transmit data 2 (LPC3240 and LPC3250 only)
KEY_ROW2/ ENET_TXD3	F14	VDD_IOD	I/O T	Keyscan row 2 out
			I/O T	Ethernet transmit data 3 (LPC3240 and LPC3250 only)
KEY_ROW3/ ENET_TX_EN	D16	VDD_IOD	I/O T	Keyscan row 3 out
			I/O T	Ethernet transmit enable (LPC3240 and LPC3250 only)
KEY_ROW4/ ENET_TXD0	C17	VDD_IOD	I/O T	Keyscan row 4 out
			I/O T	Ethernet transmit data 0 (LPC3240 and LPC3250 only)
KEY_ROW5/ ENET_TXD1	C18	VDD_IOD	I/O T	Keyscan row 5 out
			I/O T	Ethernet transmit data 1 (LPC3240 and LPC3250 only)
MS_BS/MAT2[1]	A6	VDD_IOD	I/O: P	MS/SD card command out
			O	Timer 2 match output 1
MS_DIO0/MAT0[0]	A8	VDD_IOD	I/O: P	MS/SD card data 0
			O	Timer 0 match output 0
MS_DIO1/ MAT0[1]	A7	VDD_IOD	I/O: P	MS/SD card data 1
			O	Timer 0 match output 1
MS_DIO2/ MAT0[2]	B8	VDD_IOD	I/O: P	MS/SD card data 2
			O	Timer 0 match output 2
MS_DIO3/ MAT0[3]	C8	VDD_IOD	I/O: P	MS/SD card data 3
			O	Timer 0 match output 3
MS_SCLK/ MAT2[0]	B7	VDD_IOD	I/O	MS/SD card clock output
			O	Timer 2 match output 0
n.c.	B17, U17, U2	-	-	not connected
ONSW	M15	VDD_RTC	O	RTC match output for external power control
P0[0]/ I2S1RX_CLK	B5	VDD_IOB	I/O	Port 0 GPIO bit 0
			I/O	I2S1 receive clock

Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
P0[1]/ I2S1RX_WS	D7	VDD_IOB	I/O	Port 0 GPIO bit 1
			I/O	I <sup>2</sup> S1 receive word select
P0[2]/ I2S0RX_SDA/ LCDVD[4]	M17	VDD_IOA	I/O	Port 0 GPIO bit 2
			I/O	I <sup>2</sup> S0 receive data
			I/O	LCD data bit 4 (LPC3230 and LPC3250 only)
P0[3]/ I2S0RX_CLK/ LCDVD[5]	M18	VDD_IOA	I/O	Port 0 GPIO bit 3
			I/O	I <sup>2</sup> S0 receive clock
			I/O	LCD data bit 5 (LPC3230 and LPC3250 only)
P0[4]/ I2S0RX_WS/ LCDVD[6]	L15	VDD_IOA	I/O	Port 0 GPIO bit 4
			I/O	I <sup>2</sup> S0 receive word select
			I/O	LCD data bit 6 (LPC3230 and LPC3250 only)
P0[5]/ I2S0TX_SDA/ LCDVD[7]	L16	VDD_IOA	I/O	Port 0 GPIO bit 5
			I/O	I <sup>2</sup> S0 transmit data
			I/O	LCD data bit 7 (LPC3230 and LPC3250 only)
P0[6]/ I2S0TX_CLK/ LCDVD[12]	L17	VDD_IOA	I/O	Port 0 GPIO bit 6
			I/O	I <sup>2</sup> S0 transmit clock
			I/O	LCD data bit 12 (LPC3230 and LPC3250 only)
P0[7]/ I2S0TX_WS/ LCDVD[13]	L18	VDD_IOA	I/O	Port 0 GPIO bit 7
			I/O	I <sup>2</sup> S0 transmit word select
			I/O	LCD data bit 13 (LPC3230 and LPC3250 only)
PLL397_LOOP	R14	VDD_PLL397	analog filter	PLL397 loop filter (for external components)
PWM_OUT1/ LCDVD[16]	D14	VDD_IOD	O	PWM1 out
			O	LCD data bit 16 (LPC3230 and LPC3250 only)
PWM_OUT2/INTSTAT/ LCDVD[19]	D15	VDD_IOD	O	PWM2 output/internal interrupt status <sup>[1]</sup>
			O	LCD data bit 19 (LPC3230 and LPC3250 only)
RESET	M14	VDD_RTC	I	Reset input, active LOW
RESOUT	G4	VDD_IOC	O	Reset out. Reflects external and WDT reset
RTCX_IN	P16	VDD_RTC	analog in	RTC oscillator input
RTCX_OUT	P17	VDD_RTC	analog out	RTC oscillator output
SPI1_CLK/ SCK0	C9	VDD_IOD	O	SPI1 clock out
			O	SSP0 clock out
SPI1_DATIN/ MISO0/ GPI_25/ MCI1	C10	VDD_IOD	I/O	SPI1 data in
			I/O	SSP0 MISO
			I/O	General purpose input bit 25
			I	Motor control channel 1 input
SPI1_DATIO/ MOSI0/ MCI2	B9	VDD_IOD	I/O	SPI1 data out (and optional input)
			I/O	SSP0 MOSI
			I	Motor control channel 2 input

Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
SPI2_CLK/ SCK1/ LCDVD[23]	B10	VDD_IOD	I/O	SPI2 clock out
			I/O	SSP1 clock out
			I/O	LCD data bit 23 (LPC3230 and LPC3250 only)
SPI2_DATIO/ MOSI1/ LCDVD[20]	A9	VDD_IOD	I/O	SPI2 data out (and optional input)
			I/O	SSP1 MOSI
			I/O	LCD data bit 20 (LPC3230 and LPC3250 only)
SPI2_DATIN/ MISO1/ LCDVD[21]/ GPI_27	A10	VDD_IOD	I/O	SPI2 data in
			I/O	SSP1 MISO
			I/O	LCD data bit 21 (LPC3230 and LPC3250 only)
			I/O	General purpose input bit 27
SYSCLKEN/ LCDVD[15]	G17	VDD_IOD	I/O T	Clock request out for external clock source
			I/O T	LCD data bit 15 (LPC3230 and LPC3250 only)
SYSX_IN	T17	VDD_OSC	analog in	System clock oscillator input
SYSX_OUT	R15	VDD_OSC	analog out	System clock oscillator output
TS_XP	R13	VDD_AD	I/O	Touchscreen X output
TS_YP	U16	VDD_AD	I/O	Touchscreen Y output
TST_CLK2	C6	VDD_IOB	O	Test clock 2 out
U1_RX/CAP1[0]/ GPI_15	K15	VDD_IOA	I/O	HS UART 1 receive
			I/O	Timer 1 capture input 0
			I/O	General purpose input bit 15
U1_TX	K16	VDD_IOA	O	HS UART 1 transmit
U2_HCTS/ U3_CTS/GPI_16	J18	VDD_IOA	I/O	HS UART 2 Clear to Send input
			I	UART 3 Clear to Send
			I/O	General purpose input bit 16
U2_RX/ U3_DSR/GPI_17	K18	VDD_IOA	I/O	HS UART 2 receive
			I/O	UART 3 data set ready
			I/O	General purpose input bit 17
U2_TX/U3_DTR	K17	VDD_IOA	O	HS UART 2 transmit
			O	UART 3 data terminal ready out
U3_RX/ GPI_18	J14	VDD_IOD	I/O	UART 3 receive
			I/O	General purpose input bit 18
U3_TX	J17	VDD_IOD	O	UART 3 transmit
U5_RX/ GPI_20	F18	VDD_IOD	I/O	UART 5 receive
			I	General purpose input bit 20
U5_TX	H15	VDD_IOD	O	UART 5 transmit
U6_IRRX/ GPI_21	F17	VDD_IOD	I/O	UART 6 receive (with IrDA)
			I	General purpose input bit 21
U6_IRTX	G16	VDD_IOD	O	UART 6 transmit (with IrDA)

Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
U7_HCTS/ CAP0[1]/ LCDCLKIN/ GPI_22	G13	VDD_IOD	I	HS UART 7 CTS in
			I	Timer 0 capture input 1
			I	LCD panel clock in (LPC3230 and LPC3250 only)
			I	General purpose input bit 22
U7_RX/ CAP0[0]/ LCDVD[10]/ GPI_23	E17	VDD_IOD	I/O	HS UART 7 receive
			I/O	Timer 0 capture input 0
			I/O	LCD data bit 10 (LPC3230 and LPC3250 only)
			I/O	General purpose input bit 23
U7_TX/ MAT1[1]/ LCDVD[11]	E18	VDD_IOD	O	HS UART 7 transmit
			O	Timer 1 match output 1
			O	LCD data bit 11 (LPC3230 and LPC3250 only)
USB_ATX_INT	C4	VDD_IOC	I	Interrupt from USB ATX
USB_DAT_VP/ U5_RX	D5	VDD_IOC	I/O: P	USB transmit data, D+ receive
			I/O: P	UART 5 receive
USB_I2C_SCL	E5	VDD_IOC	I/O T	I <sup>2</sup> C clock for USB ATX interface
USB_I2C_SDA	E6	VDD_IOC	I/O T	I <sup>2</sup> C data for USB ATX interface
USB_OE_TP	D6	VDD_IOC	I/O	USB transmit enable for DAT/SE0
USB_SE0_VM/ U5_TX	C5	VDD_IOC	I/O: P	USB single ended zero transmit, D- Receive
			I/O: P	UART 5 transmit
VDD_AD	N12, N13	VDD_AD	power	3.3 V supply for ADC/touch screen
VDD_CORE	G7, G9, G11, J7, J12, M7, M11	VDD_CORE	power	1.2 V or 0.9 V supply for core
VDD_COREFXD	L12, M13	VDD_COREFXD	power	Fixed 1.2 V supply for digital portion of the analog block
VDD EMC	J6, K6, K7, L6, M6, M8, N7, N8, N9, N10, N11	VDD EMC	power	1.8 V or 2.5 V or 3.3 V supply for External Memory Controller (EMC)
VDD_IOA	H13, J13	VDD_IOA	power	1.8 V or 3.3 V supply for IOA domain
VDD_IOB	F8	VDD_IOB	power	1.8 V or 3.3 V supply for IOB domain

Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
VDD_IOC	F7, G6, H6, J5	VDD_IOC	power	1.8 V or 3.3 V supply for IOC domain
VDD_IOD	F13, F9	VDD_IOD	power	1.8 V to 3.3 V supply for IOD domain
VDD_OSC	T18	VDD_OSC	power	1.2 V supply for main oscillator
VDD_PLL397	T16	VDD_PLL397	power	1.2 V supply for 397x PLL
VDD_PLLHCLK	R17	VDD_PLLHCLK	power	1.2 V supply for HCLK PLL
VDD_PLLUSB	P15	VDD_PLLUSB	power	1.2 V supply for USB PLL
VDD_FUSE	N14	VDD_FUSE	power	1.2 V supply
VDD_RTC	K14	VDD_RTC	power	1.2 V supply for RTC I/O
VDD_RTCCORE	L13	VDD_RTCCORE	power	1.2 V supply for RTC
VDD_RTCOSC	N15	VDD_RTCOSC	power	1.2 V supply for RTC oscillator
VSS_AD	P13	-	power	Ground for ADC/touch screen
VSS_CORE	G8, G10, G12, H7, K12, L7, M9, M10, M12	-	power	Ground for core
VSS_EMC	K5, L5, M5, N5, N6, P6, P7, P8, P9, P10, P11	-	power	Ground for EMC
VSS_IOA	K13	-	power	Ground VDD_IOA domain
VSS_IOB	F6	-	power	Ground VDD_IOB domain
VSS_IOC	F5, G5, H5	-	power	Ground VDD_IOC domain
VSS_IOD	F10, F11, F12, H12	-	power	Ground VDD_IOD domain
VSS_OSC	P14	-	power	Ground for main oscillator
VSS_PLL397	T15	-	power	Ground for 397x PLL
VSS_PLLHCLK	R18	-	power	Ground for HCLK PLL

Table 4. Pin description ...continued

Symbol	Pin	Power supply domain	Type	Description
VSS_PLLUSB	R16	-	power	Ground for USB PLL
VSS_RTCCORE	L14	-	power	Ground for RTC
VSS_RTCOSC	P18	-	power	Ground for RTC oscillator

[1] The PWM2\_CTRL register controls this pin function (see LPC32x0 User manual).

Table 5. Digital I/O pad types<sup>[1]</sup>

Parameter	Abbreviation
I/O type	I = input. O = output. I/O = bidirectional. I/O T = bidirectional or high impedance.
Pin detail	BK: pin has a bus keeper function that weakly retains the last logic level driven on an I/O pin. Bus keeper current for different I/O pin voltages: 0 V = 1 µA (max) VDD_x = 1 µA (max) 2/3 × VDD_x = 55 µA (max) 1/3 × VDD_x = 60 µA (max) PU: pin has a nominal 50 µA internal pull-up connected. PD: pin has a nominal 50 µA internal pull-down connected. P: pin has programmable input characteristics.

[1] See LPC32x0 User manual for details.

Table 6. Supply domains

Supply domain	Voltage range	Related supply pins	Description
VDD_CORE	0.9 V to 1.39 V	VDD_CORE	Core power domain.
VDD_COREFXD	1.2 V	VDD_COREFXD	Fixed 1.2 V supply for digital portion of the analog block.
other core domains	1.2 V	VDD_PLL397, VDD_PLLHCLK, VDD_PLLUSB, VDD_FUSE, VDD_OSC	1.2 V supplies, tied to VDD_COREFXD.
VDD_RTC	0.9 V to 1.39 V	VDD_RTC, VDD_RTCCORE, VDD_RTCOSC	RTC supply domain. Can be connected to a battery backed-up power source.
VDD_AD	2.7 V to 3.6 V	VDD_AD	3.3 V supply for ADC and touch screen.
VDD EMC	1.7 V to 1.95 V 2.3 V to 2.7 V 2.7 V to 3.6 V	VDD EMC	External memory interface IO pins in 1.8 V range, 2.5 V range, or 3.3 V range.

Table 6. Supply domains

Supply domain	Voltage range	Related supply pins	Description
VDD_IOA <sup>[1]</sup>	1.7 V to 1.95 V or 2.7 V to 3.6 V	VDD_IOA	Peripheral supply.
VDD_IOB <sup>[1]</sup>	1.7 V to 1.95 V or 2.7 V to 3.6 V	VDD_IOB	Peripheral supply.
VDD_IOC <sup>[1]</sup>	1.7 V to 1.95 V or 2.3 V to 3.6 V	VDD_IOC	Peripheral supply.
VDD_IOD <sup>[1]</sup>	1.7 V to 1.95 V or 2.7 V to 3.6 V	VDD_IOD	Peripheral supply.

[1] The VDD\_IOA, VDD\_IOB, VDD\_IOC, and VDD\_IOD supply domains can be operated at a voltage independent of the other domains as long as all pins connected to the same peripheral are at the same voltage level. There are two special cases for determining supply domain voltages (for details see *application note AN10777*):

- a) Ethernet configured in MII mode: VDD\_IOD must be the same as VDD\_IOB.
- b) UART 3 when used with hardware flow control or when sharing an RS-232 transceiver with another UART: VDD\_IOA must be the same as VDD\_IOD.



## 7. Functional description

### 7.1 CPU and subsystems

#### 7.1.1 CPU

NXP created the LPC3220/30/40/50 using an ARM926EJ-S CPU core that includes a Harvard architecture and a 5-stage pipeline. To this ARM core, NXP implemented a 32 kB instruction cache, a 32 kB data cache and a Vector Floating Point coprocessor. The ARM926EJ-S core also has an integral Memory Management Unit (MMU) to provide the virtual memory capabilities required to support the multi-programming demands of modern operating systems. The basic ARM926EJ-S core V5TE instruction set includes DSP instruction extensions for native Jazelle Java Byte-code execution in hardware. The LPC3220/30/40/50 operates at CPU frequencies up to 266 MHz.

#### 7.1.2 Vector Floating Point (VFP) coprocessor

The LPC3220/30/40/50 includes a VFP co-processor providing full support for single-precision and double-precision add, subtract, multiply, divide, and multiply-accumulate operations at CPU clock speeds. It is compliant with the IEEE 754 standard for binary Floating-Point Arithmetic. This hardware floating point capability makes the microcontroller suitable for advanced motor control and DSP applications. The VFP has 3 separate pipelines for floating-point MAC operations, divide or square root operations, and Load/Store operations. These pipelines operate in parallel and can complete execution out of order. All single-precision instructions execute in one cycle, except the divide and square root instructions. All double-precision multiply and multiply-accumulate instructions take two cycles. The VFP also provides format conversions between floating-point and integer word formats.

#### 7.1.3 Emulation and debugging

The LPC3220/30/40/50 supports emulation and debugging via a dedicated JTAG serial port. An Embedded Trace Buffer allows tracing program execution. The dedicated JTAG port allows debugging of all chip features without impact to any pins that may be used in the application.

##### 7.1.3.1 Embedded ICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an Embedded ICE protocol converter. The Embedded ICE protocol converter converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel (DCC) function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or entering the debug state.

### 7.1.3.2 Embedded trace buffer

The Embedded Trace Module (ETM) is connected directly to the ARM core. It compresses the trace information and exports it through a narrow trace port. An internal Embedded Trace Buffer (ETB) of  $2048 \times 24$  bits captures the trace information under software debugger control. Data from the ETB is recovered by the debug software through the JTAG port.

The trace contains information about when the ARM core switches between states. Instruction shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. For data accesses either data or address or both can be traced.

## 7.2 AHB matrix

The LPC3220/30/40/50 has a multi-layer AHB matrix for inter-block communication. AHB is an ARM defined high-speed bus, which is part of the ARM bus architecture. AHB is a high-bandwidth low-latency bus that supports multi-master arbitration and a bus grant/request mechanism. For systems that have only one (CPU), or two (CPU and DMA) bus masters a simple AHB works well. However, if a system requires multiple bus masters and the CPU needs access to external memory, a single AHB bus can cause a bottleneck.

To increase performance, the LPC3220/30/40/50 uses an expanded AHB architecture known as Multi-layer AHB. A Multi-layer AHB replaces the request/grant and arbitration mechanism used in a simple AHB with an interconnect matrix that moves arbitration out toward the slave devices. Thus, if a CPU and a DMA controller want access to the same memory, the interconnect matrix arbitrates between the two when granting access to the memory. This advanced architecture allows simultaneous access by bus masters to different resources with an increase in arbitration complexity. In this architectural implementation, removing guaranteed central arbitration and allowing more than one bus master to be active at the same time provides better overall microcontroller performance.

In the LPC3220/30/40/50, the multi-Layer AHB system has a separate bus for each of seven AHB Masters:

- CPU data bus
- CPU instruction bus
- General purpose DMA Master 0
- General purpose DMA Master 1
- Ethernet controller
- USB controller
- LCD controller

There are no arbitration delays unless two masters attempt to access the same slave at the same time.