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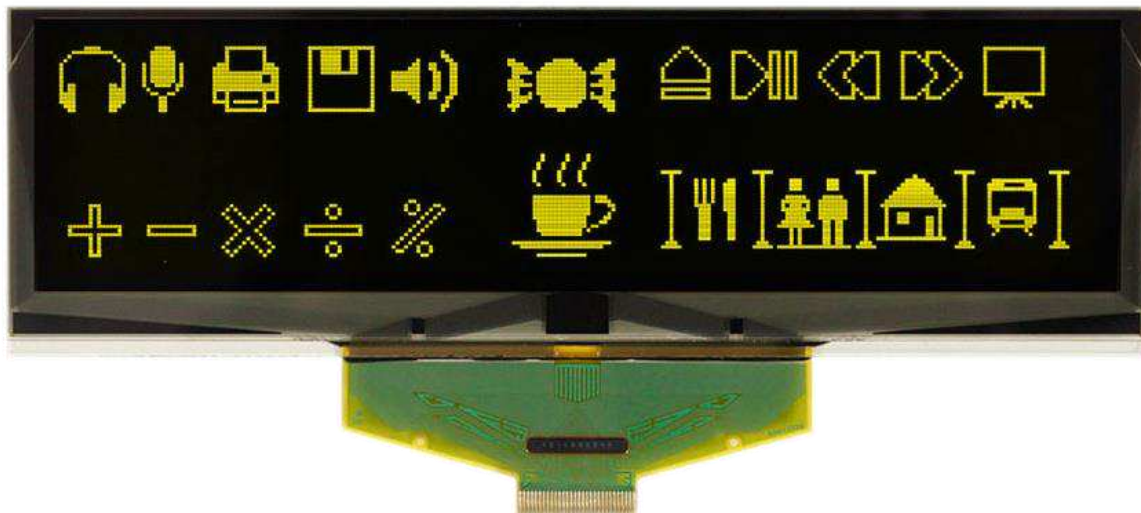
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



03.2018

OLED 5.5" - 256x64 dots

Incl. controller SSD1322



Features

- 5.5" Low-Power OLED
- -40..+80°C (Top.)
- 256x64 dots
- Yellow display
- Incl. controller SSD1322
- SPI, 8-Bit Interface
- Fast response time (10µs) even at -40°C
- ZIFF connection
- 146x45mm outline dimensions

Ordering code

OLED 5.5" - 256x64 dots, yellow

EA W256064-XGLG

Accessory

ZIFF connector 30 pins, 0.5mm pitch, top contact

EA WF050-30T

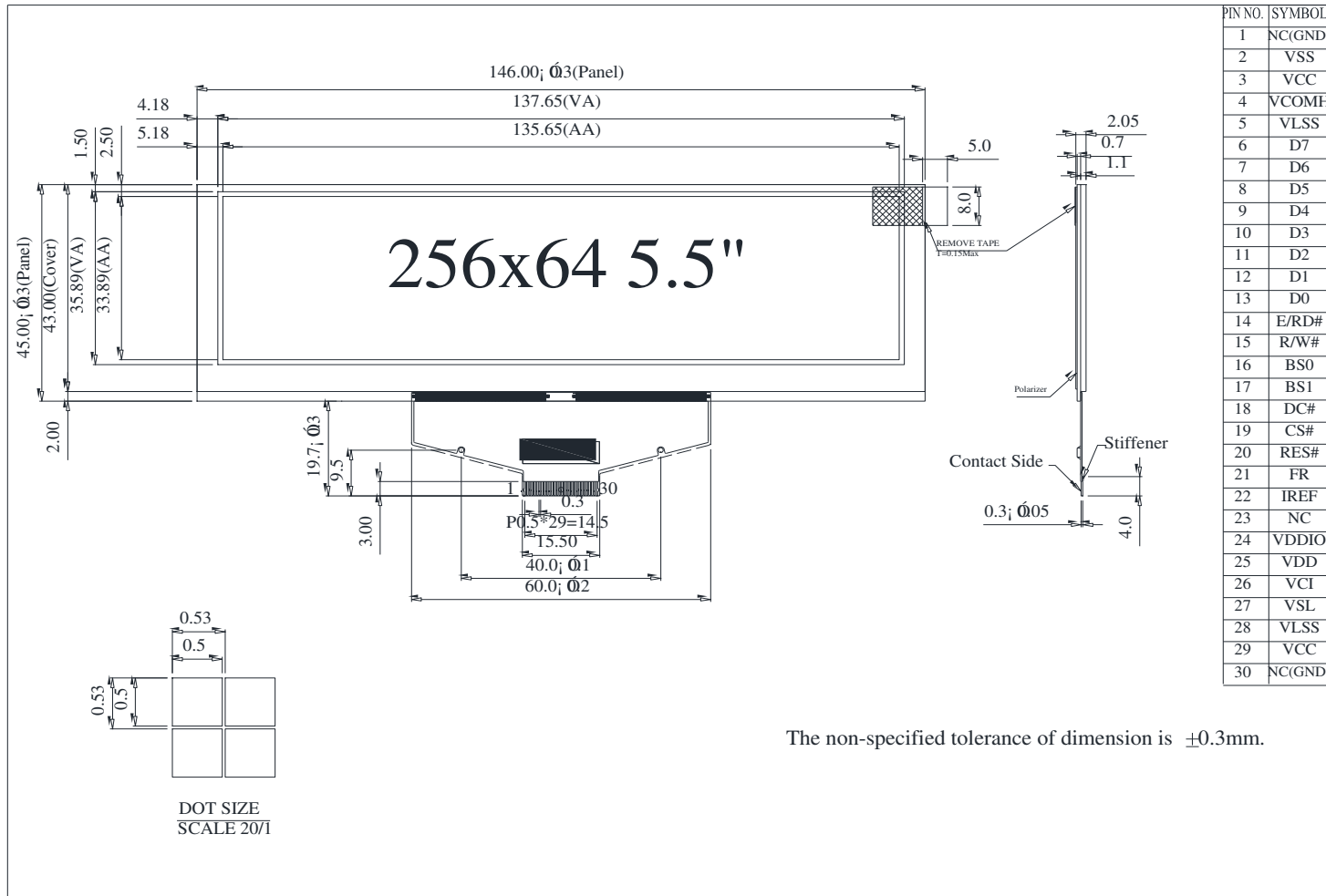
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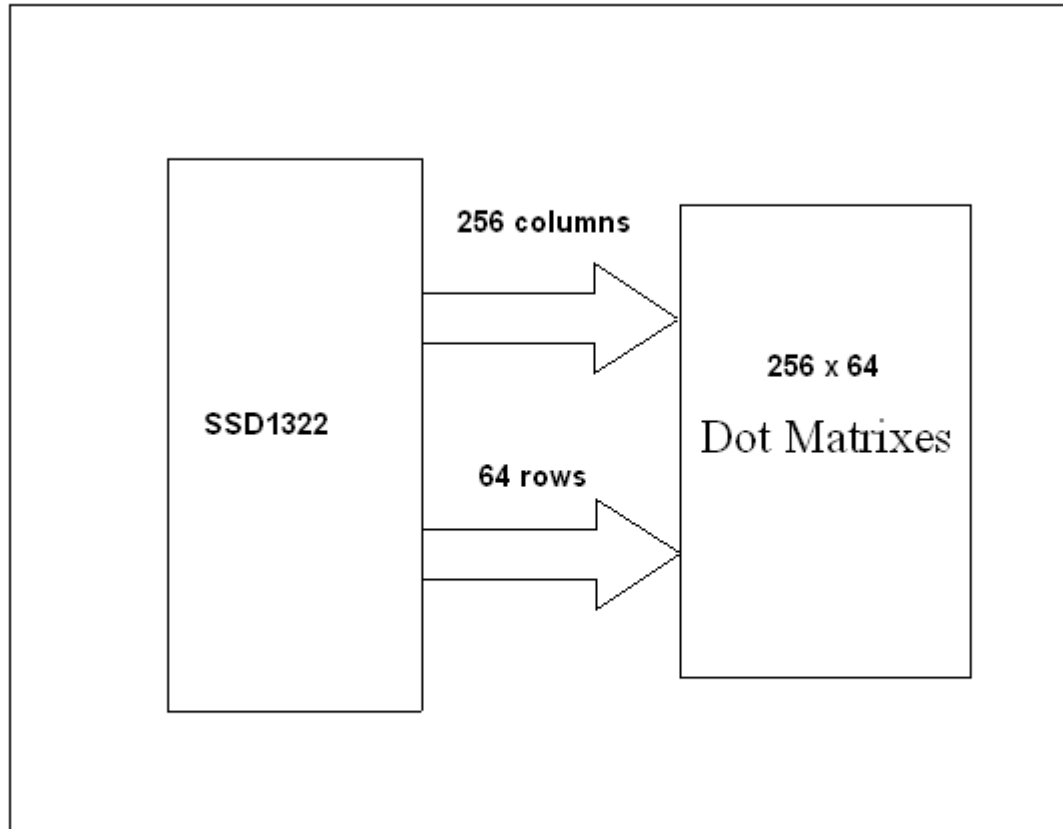
1. General Specification

Item	Dimension	Unit
Dot Matrix	256 x 64 Dots	—
Module dimension	146.0 x 45.0 x 2.05	mm
Active Area	135.65 x 33.89	mm
Pixel Size	0.5 x 0.5	mm
Pixel Pitch	0.53 x 0.53	mm
Display Mode	Passive Matrix	
Display Color	Green	
Drive Duty	1/64 Duty	
IC	SSD1322	

2. Contour Drawing & Block Diagram



FUNCTION BLOCK DIAGRAM



3. Interface Pin Function

Pin	Symbol	I/O	Function
Power Supply			
26	VCI	P	Power Supply for Operation This is a voltage supply pin. It must be connected to external source & always be equal to or higher than VDD & VDDIO.
25	VDD	P	Power Supply for Core Logic Circuit This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.
24	VDDIO	P	Power Supply for I/O Pin This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals...) pull high, they should be connected to VDDIO.
2	VSS	P	Ground of Logic Circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.
3,29	VCC	P	Power Supply for OLED Panel These are the most positive voltage supply pin of the chip. They must be connected to external source.
5,28	VLSS	P	Ground of Analog Circuit These are the analog ground pins. They should be connected to VSS externally.
Driver			
22	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 10uA.
4	VCOMH	P	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
27	VSL	P	Voltage Output Low Level for SEG Signal This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.

Testing Pads																		
21	FR	O	This pin is No Connection pins. Nothing should be connected to this pin. This pin should be left open individually.															
16	BS0	I	<p>Communicating Protocol Select These pins are MCU interface selection input. See the following table:</p> <table border="1"> <thead> <tr> <th></th> <th>BS0</th> <th>BS1</th> </tr> </thead> <tbody> <tr> <td>3-wire SPI</td> <td>1</td> <td>0</td> </tr> <tr> <td>4-wire SPI</td> <td>0</td> <td>0</td> </tr> <tr> <td>8-bit 68XX Parallel</td> <td>1</td> <td>1</td> </tr> <tr> <td>8-bit 80XX Parallel</td> <td>0</td> <td>1</td> </tr> </tbody> </table>		BS0	BS1	3-wire SPI	1	0	4-wire SPI	0	0	8-bit 68XX Parallel	1	1	8-bit 80XX Parallel	0	1
	BS0			BS1														
3-wire SPI	1	0																
4-wire SPI	0	0																
8-bit 68XX Parallel	1	1																
8-bit 80XX Parallel	0	1																
17	BS1																	
20	RES#	I	<p>Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed.</p>															
19	CS#	I	<p>Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</p>															
18	D/C#	I	<p>Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</p>															
14	E/RD#	I	<p>Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.</p>															
15	R/W#	I	<p>Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.</p>															

			When serial mode is selected, this pin must be connected to VSS.
6~13	D7~D0	I/O	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.
Reserve			
23	N.C.	-	Reserved Pin The N.C. pin between function pins are reserved for compatible and flexible design.
1,30	N.C. (GND)	-	Reserved Pin (Supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	VCI	-0.3	4	V	1, 2
Supply Voltage for Logic	VDD	-0.5	2.75	V	1, 2
Supply Voltage for I/O Pins	VDDIO	-0.5	VCI	V	1, 2
Supply Voltage for Display	VCC	-0.5	20	V	1, 2
Operating Temperature	TOP	-40	80	°C	-
Storage Temperature	TSTG	-40	80	°C	-

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 6 "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate

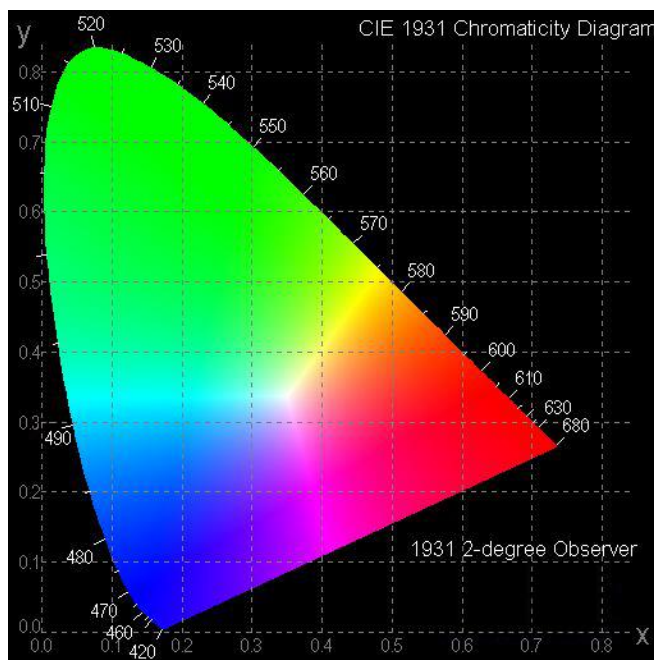
5. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Operation	VCI	Note	2.8	3.0	3.3	V
Supply Voltage for Display	VCC	—	14	14.5	16	V
High Level Input	VIH	—	$0.8 \times V_{DDIO}$	—	V_{DDIO}	V
Low Level Input	VIL	—	0	—	$0.2 \times V_{DDIO}$	V
High Level Output	VOH	—	$0.9 \times V_{DDIO}$	—	V_{DDIO}	V
Low Level Output	VOL	—	0	—	$0.1 \times V_{DDIO}$	V
50% Check Board operating Current		VCC =14.5V	34	36	45	mA

Note: Supply Voltage for Logic = VDD core power supply can be regulated from VCI.

6. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) θ		160			deg
	(H) ϕ		160			deg
Contrast Ratio	CR	Dark	2000:1		—	—
Response Time	T rise	—		10		μ s
	T fall	—		10		μ s
Display with 50% check Board Brightness			60	80		cd/m ²
CIEx(Green)		(CIE1931)	0.24	0.28	0.32	
CIEy(Green)		(CIE1931)	0.59	0.63	0.67	



7. OLED Lifetime

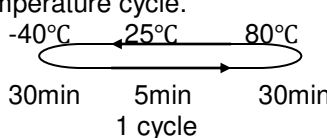
ITEM	Conditions	Min	Typ	Remark
Operating Life Time	Ta=25°C / Initial 50% check board brightness Typical Value	40,000 Hrs	—	Note

Notes:

1. Life time is defined the amount of time when the luminance has decayed to <50% of the initial value.
2. This analysis method uses life data obtained under accelerated conditions to extrapolate an estimated probability density function (*pdf*) for the product under normal use conditions.
3. Screen saving mode will extend OLED lifetime.

8. Reliability

Content of Reliability Test

Environmental Test			
Test Item	Content of Test	Test Condition	Applicable Standard
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 240hrs	—
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-40°C 240hrs	—
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	80°C 240hrs	—
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-40°C 240hrs	—
High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60°C,90%RH 240hrs	—
Temperature Cycle	Endurance test applying the low and high temperature cycle. 	-40°C/80°C 100 cycles	—
Mechanical Test			
Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hr	—
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sin wave 11 ms 3 times of each direction	—
Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	—
Others			
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact), ±800v(air), RS=330Ω CS=150pF 10 times	—

*** Supply voltage for OLED system =Operating voltage at 25°C

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability. After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at $23\pm 5^{\circ}\text{C}$; $55\pm 15\%$ RH.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for High Temperature storage, High Temperature/ Humidity Storage, Temperature Cycle

Evaluation criteria

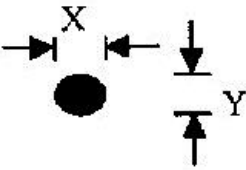
1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within $\pm 50\%$ of initial value.

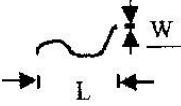
APPENDIX:

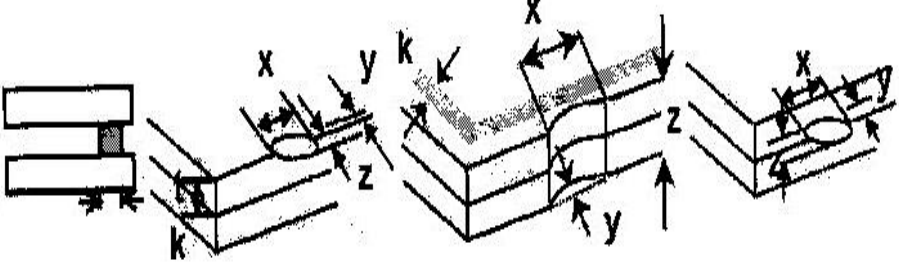
RESIDUE IMAGE

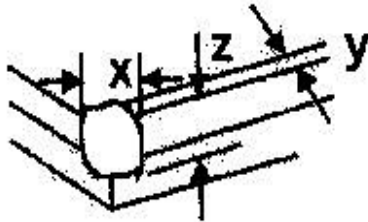
Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.

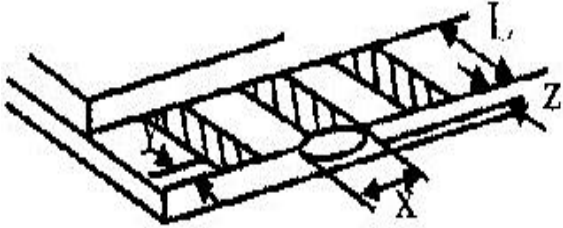
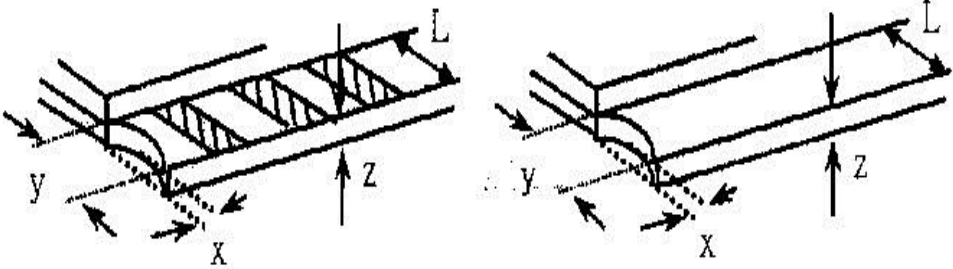
9. Inspection specification

NO	Item	Criterion	AQL											
01	Electrical Testing	1.1 Missing vertical, horizontal segment, segment contrast defect. 1.2 Missing character , dot or icon. 1.3 Display malfunction. 1.4 No function or no display. 1.5 Current consumption exceeds product specifications. 1.6 OLED viewing angle defect. 1.7 Mixed product types. 1.8 Contrast defect.	0.65											
02	Black or white spots on OLED (display only)	2.1 White and black spots on display $\leq 0.25\text{mm}$, no more than three white or black spots present. 2.2 Densely spaced: No more than two spots or lines within 3mm.	2.5											
03	OLED black spots, white spots, contamination (non-display)	3.1 Round type : As following drawing $\Phi = (x + y) / 2$  <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SIZE</th> <th>Acceptable Q TY</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.10$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.10 < \Phi \leq 0.20$</td> <td>2</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.25$</td> <td>1</td> </tr> <tr> <td>$0.25 < \Phi$</td> <td>0</td> </tr> </tbody> </table>	SIZE	Acceptable Q TY	$\Phi \leq 0.10$	Accept no dense	$0.10 < \Phi \leq 0.20$	2	$0.20 < \Phi \leq 0.25$	1	$0.25 < \Phi$	0	2.5	
SIZE	Acceptable Q TY													
$\Phi \leq 0.10$	Accept no dense													
$0.10 < \Phi \leq 0.20$	2													
$0.20 < \Phi \leq 0.25$	1													
$0.25 < \Phi$	0													
		3.2 Line type : (As following drawing) <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Length</th> <th>Width</th> <th>Acceptable Q TY</th> </tr> </thead> <tbody> <tr> <td>---</td> <td>$W \leq 0.02$</td> <td>Accept no dense</td> </tr> <tr> <td>$L \leq 3.0$</td> <td>$0.02 < W \leq 0.03$</td> <td rowspan="2">2</td> </tr> <tr> <td>$L \leq 2.5$</td> <td>$0.03 < W \leq 0.05$</td> </tr> </tbody> </table>	Length	Width	Acceptable Q TY	---	$W \leq 0.02$	Accept no dense	$L \leq 3.0$	$0.02 < W \leq 0.03$	2	$L \leq 2.5$	$0.03 < W \leq 0.05$	2.5
Length	Width	Acceptable Q TY												
---	$W \leq 0.02$	Accept no dense												
$L \leq 3.0$	$0.02 < W \leq 0.03$	2												
$L \leq 2.5$	$0.03 < W \leq 0.05$													

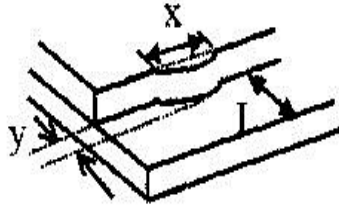
			---	$0.05 < W$	As round type													
04	Polarizer bubbles	<p>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.</p> <table border="1"> <thead> <tr> <th>Size Φ</th> <th>Acceptable Q TY</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.20$</td> <td>Accept no dense</td> </tr> <tr> <td>$0.20 < \Phi \leq 0.50$</td> <td>3</td> </tr> <tr> <td>$0.50 < \Phi \leq 1.00$</td> <td>2</td> </tr> <tr> <td>$1.00 < \Phi$</td> <td>0</td> </tr> <tr> <td>Total Q TY</td> <td>3</td> </tr> </tbody> </table>	Size Φ	Acceptable Q TY	$\Phi \leq 0.20$	Accept no dense	$0.20 < \Phi \leq 0.50$	3	$0.50 < \Phi \leq 1.00$	2	$1.00 < \Phi$	0	Total Q TY	3				2.5
Size Φ	Acceptable Q TY																	
$\Phi \leq 0.20$	Accept no dense																	
$0.20 < \Phi \leq 0.50$	3																	
$0.50 < \Phi \leq 1.00$	2																	
$1.00 < \Phi$	0																	
Total Q TY	3																	

NO	Item	Criterion	AQL						
05	Scratches	Follow NO.3 OLED black spots, white spots, contamination							
06	Chipped glass	<p>Symbols Define: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: OLED side length L: Electrode pad length:</p> <p>6.1 General glass chip : 6.1.1 Chip on panel surface and crack between panels:</p>  <table border="1"> <tr> <td>z: Chip thickness</td> <td>y: Chip width</td> <td>x: Chip length</td> </tr> <tr> <td>$Z \leq 1/2t$</td> <td>Not over viewing</td> <td>$x \leq 1/8a$</td> </tr> </table>	z: Chip thickness	y: Chip width	x: Chip length	$Z \leq 1/2t$	Not over viewing	$x \leq 1/8a$	2.5
z: Chip thickness	y: Chip width	x: Chip length							
$Z \leq 1/2t$	Not over viewing	$x \leq 1/8a$							

			area	
		$1/2t < z \leq 2t$	Not exceed $1/3k$	$x \leq 1/8a$
		<p>⊙ If there are 2 or more chips, x is total length of each chip.</p> <p>6.1.2 Corner crack:</p> 		
		z: Chip thickness	y: Chip width	x: Chip length
		$Z \leq 1/2t$	Not over viewing area	$x \leq 1/8a$
		$1/2t < z \leq 2t$	Not exceed $1/3k$	$x \leq 1/8a$
		<p>⊙ If there are 2 or more chips, x is the total length of each chip.</p>		

NO	Item	Criterion	AQL												
06	Glass crack	<p>Symbols :</p> <p>x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: OLED side length L: Electrode pad length</p> <p>6.2 Protrusion over terminal :</p> <p>6.2.1 Chip on electrode pad :</p>  <table border="1" data-bbox="337 1077 1239 1176"> <tr> <td>y: Chip width</td> <td>x: Chip length</td> <td>z: Chip thickness</td> </tr> <tr> <td>$y \leq 0.5\text{mm}$</td> <td>$x \leq 1/8a$</td> <td>$0 < z \leq t$</td> </tr> </table> <p>6.2.2 Non-conductive portion:</p>  <table border="1" data-bbox="407 1560 1239 1703"> <tr> <td>y: Chip width</td> <td>x: Chip length</td> <td>z: Chip thickness</td> </tr> <tr> <td>$y \leq L$</td> <td>$x \leq 1/8a$</td> <td>$0 < z \leq t$</td> </tr> </table> <p>⊙ If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.</p> <p>⊙ If the product will be heat sealed by the customer, the alignment mark not be damaged.</p>	y: Chip width	x: Chip length	z: Chip thickness	$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$	y: Chip width	x: Chip length	z: Chip thickness	$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$	2.5
y: Chip width	x: Chip length	z: Chip thickness													
$y \leq 0.5\text{mm}$	$x \leq 1/8a$	$0 < z \leq t$													
y: Chip width	x: Chip length	z: Chip thickness													
$y \leq L$	$x \leq 1/8a$	$0 < z \leq t$													

6.2.3 Substrate protuberance and internal crack.


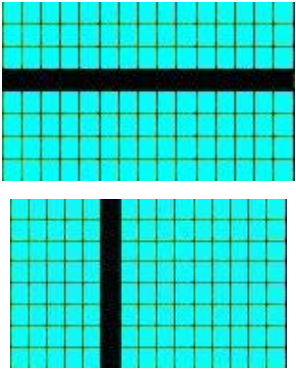
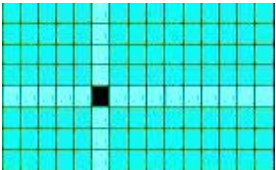
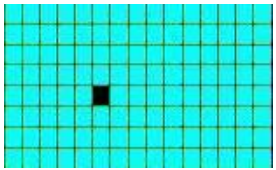
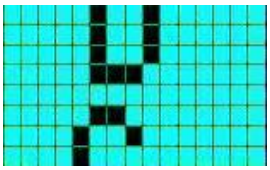
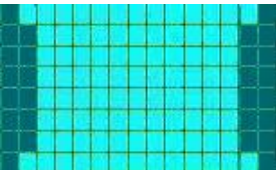


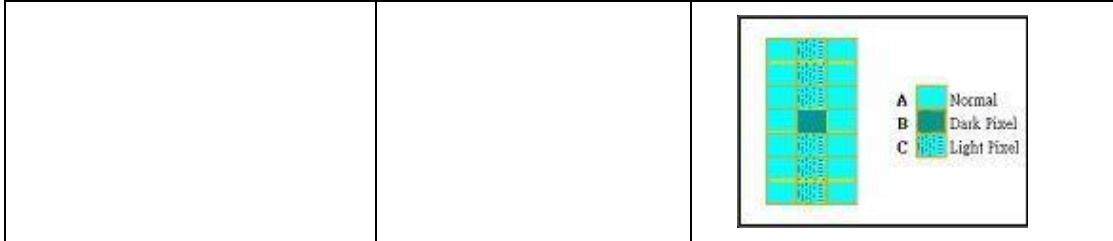
y: width	x: length
$y \leq 1/3L$	$x \leq a$

NO	Item	Criterion	AQL
07	Cracked glass	The OLED with extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using OLED spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB, COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, OLED pad, zebra pad	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5

		or screw hold pad, make sure it is smoothed down.	
11	Soldering	<p>11.1 No un-melted solder paste may be present on the PCB. 2.5</p> <p>11.2 No cold solder joints, missing solder connections, oxidation or icicle. 2.5</p> <p>11.3 No residue or solder balls on PCB. 2.5</p> <p>11.4 No short circuits in components on PCB. 0.65</p>	

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP.	2.5
		12.2 No cracks on interface pin (OLB) of TCP.	0.65
		12.3 No contamination, solder residue or solder balls on product.	2.5
		12.4 The IC on the TCP may not be damaged, circuits.	2.5
		12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever.	2.5
		12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color.	2.5
		12.7 Sealant on top of the ITO circuit has not hardened.	0.65
		12.8 Pin type must match type in specification sheet.	0.65
		12.9 OLED pin loose or missing pins.	
		12.10 Product packaging must the same as specified on packaging specification sheet.	0.65
		12.11 Product dimension and structure must conform to product specification sheet.	

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Short	Major	
Wrong Display	Major	
Un-uniform B/A x 100% < 70% A/C x 100% < 70%	Major	



10. Precautions in use of OLED Modules

Modules

- (1) Avoid applying excessive shocks to module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of OLED display module.
- (3) Don't disassemble the OLED display module.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist OLED display module.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.
- (8) It's pretty common to use "Screen Saver" to extend the lifetime and Don't use fix information for long time in real application.
- (9) Don't use fixed information in OLED panel for long time, that will extend "screen burn" effect time..
- (10) ELECTRONIC ASSEMBLY has the right to change the passive components, including R2 and R3 adjust resistors. (Resistors, capacitors and other passive components will have different appearance and color caused by the different supplier.)
- (11) ELECTRONIC ASSEMBLY have the right to change the PCB Rev. (In order to satisfy the supplying stability, management optimization and the best product performance...etc, under the premise of not affecting the electrical characteristics and external dimensions, ELECTRONIC ASSEMBLY have the right to modify the version.)

11.1. Handling Precautions

- (1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
- (2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- (3) If pressure is applied to the display surface or its neighborhood of the OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
- (4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.
- (5) When the surface of the polarizer of the OLED display module has soil, clean the surface. It