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ACT8936

Rev 4, 17-Sep-13

Advanced PMU for Samsung S3C6410

FEATURES

- Optimized for Samsung S3C6410 Processor
- Three Step-Down DC/DC Converters
- Four Low-Dropout Linear Regulators
- Integrated *ActivePath*™ Charger
- I²C™ Serial Interface
- Advanced Enable/Disable Sequencing Controller
- Minimal External Components
- Tiny 5×5mm TQFN55-40 Package
  - 0.75mm Package Height
  - Pb-Free and RoHS Compliant

GENERAL DESCRIPTION

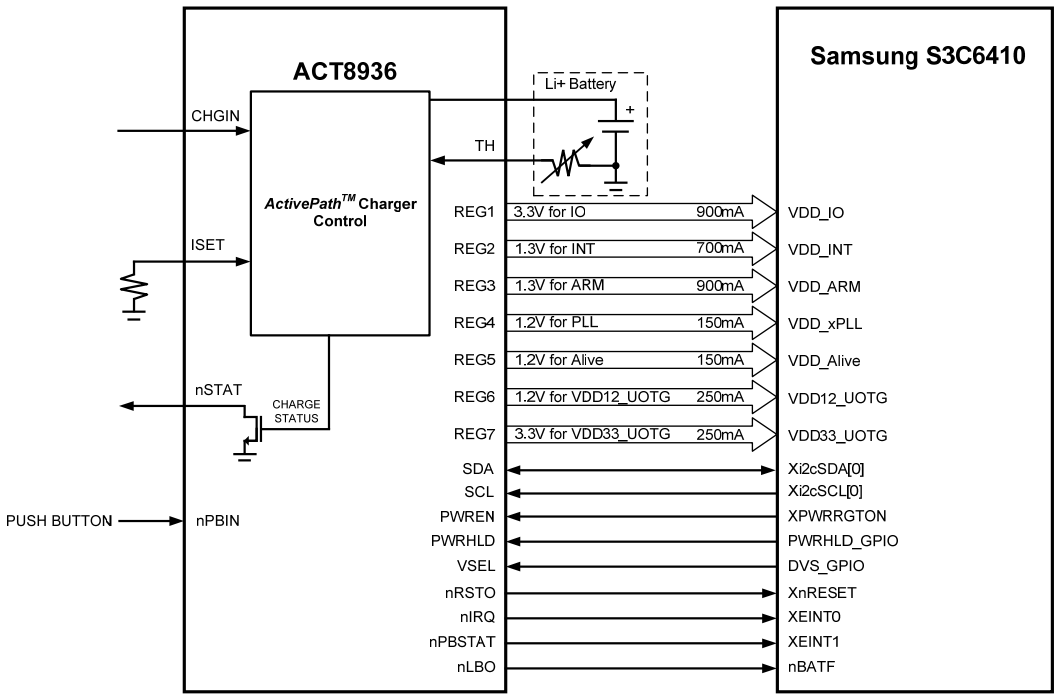
The ACT8936 is a complete, cost effective, highly-efficient *ActivePMU*™ power management solution, optimized for the unique power, voltage-sequencing, and control requirements of the Samsung S3C6410 processor.

This device features three step-down DC/DC converters and four low-noise, low-dropout linear regulators, along with a complete battery charging solution featuring the advanced *ActivePath*™ system-power selection function.

The three DC/DC converters utilize a high-efficiency, fixed-frequency (2MHz), current-mode PWM control architecture that requires a minimum number of external components. Two DC/DCs are capable of supplying up to 900mA of output current, while the third supports up to 700mA. All four low-dropout linear regulators are high-performance, low-noise regulators that supply up to 150mA, 150mA, 250mA, and 250mA, respectively.

The ACT8936 is available in a compact, Pb-Free and RoHS-compliant TQFN55-40 package.

TYPICAL APPLICATION DIAGRAM



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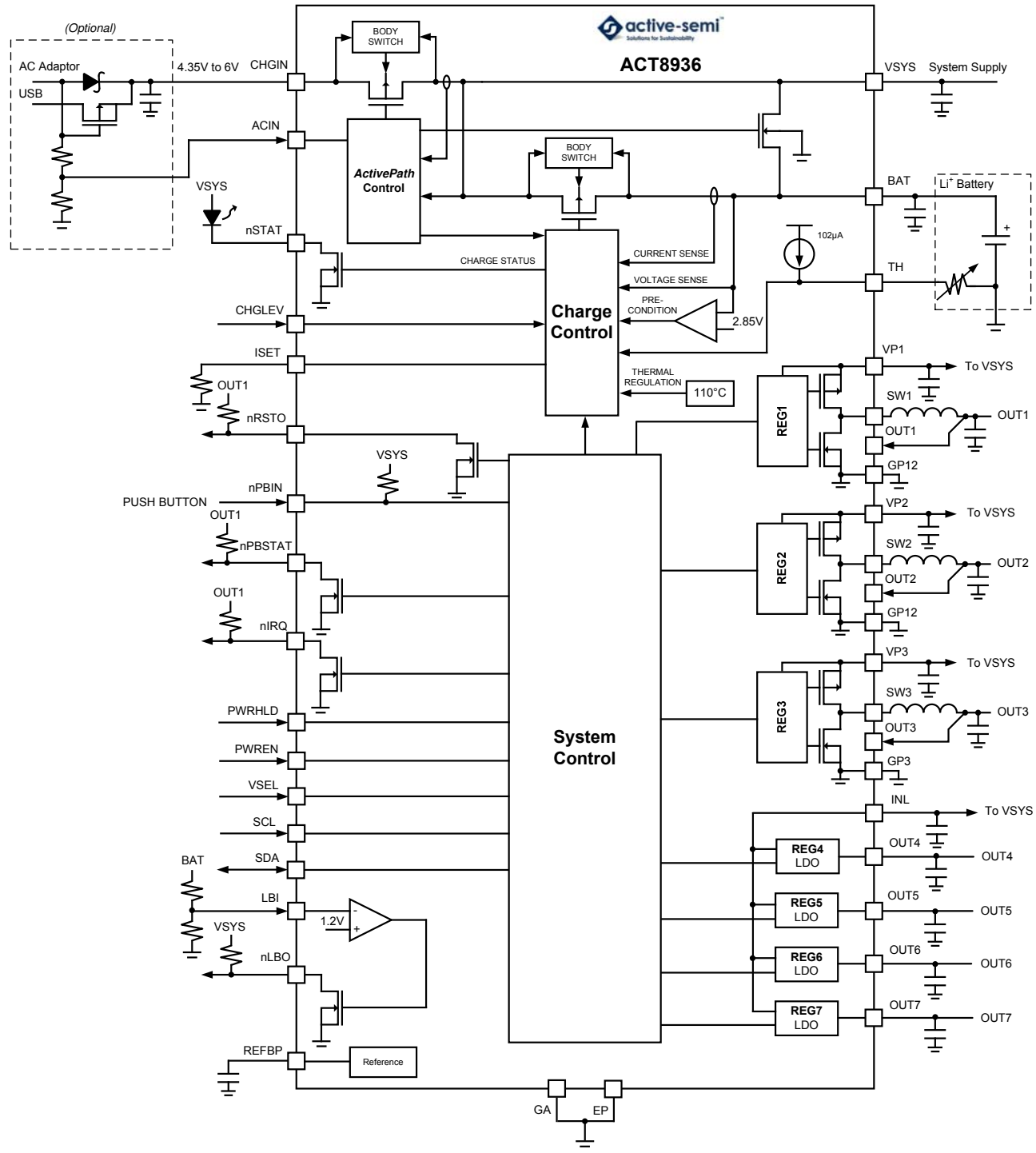
FUNCTIONAL BLOCK DIAGRAM



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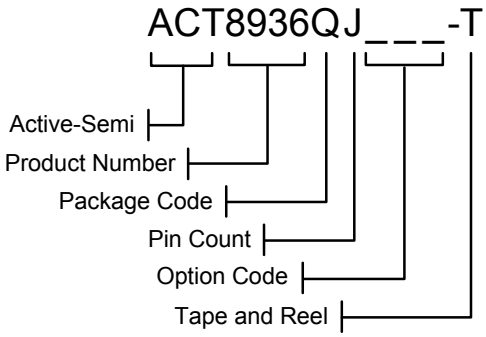
ORDERING INFORMATION①②

PART NUMBER	V_{OUT1}/V_{STBY1}③	V_{OUT2}/V_{STBY2}	V_{OUT3}/V_{STBY3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	V_{OUT7}	PACKAGE	PINS	TEMPERATURE RANGE
ACT8936QJ133-T	3.3V/3.3V	1.3V/1.3V	1.3V/1.3V	1.2V	1.2V	1.2V	3.3V	TQFN55-40	40	-40°C to +85°C
ACT8936QJ233-T	3.3V/3.3V	1.3V/1.3V	1.3V/1.3V	1.2V	1.2V	1.2V	3.3V	TQFN55-40	40	-40°C to +85°C

①: All Active-Semi components are RoHS Compliant and with Pb-free plating otherwise specified.

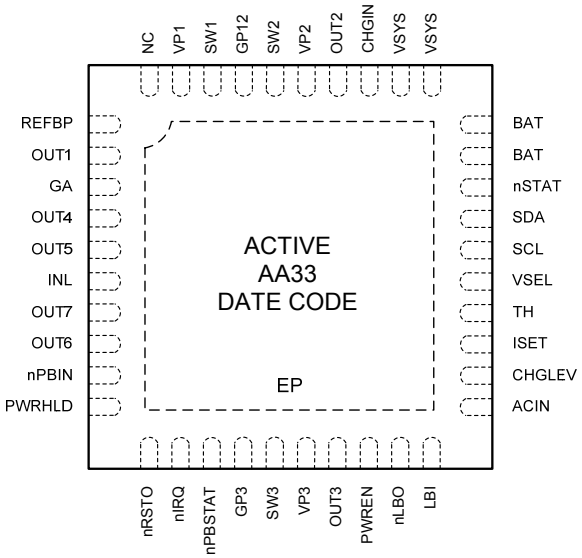
②: Standard product options are listed in this table. Contact factory for custom options. Minimum order quantity is 12,000 units.

③: To select V_{STBYx} as the output regulation voltage for REGx, drive VSEL to logic high. V_{STBYx} can be set by software via I^2C interface. Refer to appropriate sections of this datasheet for V_{STBYx} setting.



PIN CONFIGURATION

TOP VIEW



Thin - QFN (TQFN55-40)

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PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	REFBP	Reference Bypass. Connect a 0.047µF ceramic capacitor from REFBP to GA. This pin is discharged to GA in shutdown.
2	OUT1	Output Feedback Sense for REG1.
3	GA	Analog Ground. Connect GA directly to a quiet ground node. Connect GA, GP12 and GP3 together at a single point as close to the IC as possible.
4	OUT4	REG4 output. Capable of delivering up to 150mA of output current. Connect a 1.5µF ceramic capacitor from OUT4 to GA. The output is discharged to GA with 1.5kΩ resistor when disabled.
5	OUT5	REG5 output. Capable of delivering up to 150mA of output current. Connect a 1.5µF ceramic capacitor from OUT5 to GA. The output is discharged to GA with 1.5kΩ resistor when disabled.
6	INL	Power Input for REG4, REG5, REG6, and REG7. Bypass to GA with a high quality ceramic capacitor placed as close to the IC as possible.
7	OUT7	REG7 output. Capable of delivering up to 250mA of output current. Connect a 2.2µF ceramic capacitor from OUT7 to GA. The output is discharged to GA with 1.5kΩ resistor when disabled.
8	OUT6	REG6 output. Capable of delivering up to 250mA of output current. Connect a 2.2µF ceramic capacitor from OUT6 to GA. The output is discharged to GA with 1.5kΩ resistor when disabled.
9	nPBIN	Master Enable Input. Drive nPBIN to GA through a 50kΩ resistor to enable the IC, drive nPBIN directly to GA to assert a manual reset condition. Refer to the *nPBIN Multi-Function Input* section for more information. nPBIN is internally pulled up to VSYS through a 35kΩ resistor.
10	PWRHLD	Power Hold Input. Refer to the *Control Sequences* section for more information.
11	nRSTO	Active Low Reset Output. See the *nRSTO Output* section for more information.
12	nIRQ	Open-Drain Interrupt Output. nIRQ is asserted any time an unmasked fault condition exists or a charger interrupt occurs. See the *nIRQ Output* section for more information.
13	nPBSTAT	Active-Low Open-Drain Push-Button Status Output. nPBSTAT is asserted low whenever the nPBIN is pushed, and is high-Z otherwise. See the *nPBSTAT Output* section for more information.
14	GP3	Power Ground for REG3. Connect GA, GP12, and GP3 together at a single point as close to the IC as possible.
15	SW3	Switching Node Output for REG3.
16	VP3	Power Input for REG3. Bypass to GP3 with a high quality ceramic capacitor placed as close to the IC as possible.
17	OUT3	Output Feedback Sense for REG3.
18	PWREN	Power Enable Input. Refer to the *Control Sequences* section for more information.
19	nLBO	Low Battery Indicator Output. nLBO is asserted low whenever the voltage at LBI is lower than 1.2V, and is high-Z otherwise. See the *Precision Voltage Detector* section for more information.
20	LBI	Low Battery Input. The input voltage is compared to 1.2V and the output of this comparison drives nLBO. See the *Precision Voltage Detector* section for more information.
21	ACIN	AC Input Supply Detection. See the *Charge Current Programming* section for more information.
22	CHGLEV	Charge Current Selection Input. See the *Charge Current Programming* section for more information.

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PIN DESCRIPTIONS CONT'D

PIN	NAME	DESCRIPTION
23	ISET	Charge Current Set. Program the charge current by connecting a resistor (R_{ISET}) between ISET and GA. See the *Charge Current Programming* section for more information.
24	TH	Temperature Sensing Input. Connect to battery thermistor. TH is pulled up with a 102µA (typ) current internally. See the *Battery Temperature Monitoring* section for more information.
25	VSEL	Step-Down DC/DCs Output Voltage Selection. Drive to logic low to select default output voltage. Drive to logic high to select secondary output voltage. See the *Output Voltage Programming* section for more information.
26	SCL	Clock Input for I^2C Serial Interface.
27	SDA	Data Input for I^2C Serial Interface. Data is read on the rising edge of SCL.
28	nSTAT	Active-Low Open-Drain Charger Status Output. nSTAT has a 8mA (typ) current limit, allowing it to directly drive an indicator LED without additional external components. See the *Charge Status Indicator* section for more information.
29, 30	BAT	Battery Charger Output. Connect this pin directly to the battery anode (+ terminal)
31, 32	VSYS	System Output Pin. Bypass to GA with a 10µF or larger ceramic capacitor.
33	CHGIN	Power Input for the Battery Charger. Bypass CHGIN to GA with a capacitor placed as close to the IC as possible.
34	OUT2	Output Feedback Sense for REG2.
35	VP2	Power Input for REG2. Bypass to GP12 with a high quality ceramic capacitor placed as close to the IC as possible.
36	SW2	Switching Node Output for REG2.
37	GP12	Power Ground for REG1 and REG2. Connect GA, GP12 and GP3 together at a single point as close to the IC as possible.
38	SW1	Switching Node Output for REG1.
39	VP1	Power Input for REG1. Bypass to GP12 with a high quality ceramic capacitor placed as close to the IC as possible.
40	NC	No Connect. Not internally connected.
EP	EP	Exposed Pad. Must be soldered to ground on PCB.

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ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
VP1, VP2 to GP12 VP3 to GP3	-0.3 to + 6	V
BAT, VSYS, INL to GA	-0.3 to + 6	V
CHGIN to GA	-0.3 to + 14	V
SW1, OUT1 to GP12	-0.3 to (V_{VP1} + 0.3)	V
SW2, OUT2 to GP12	-0.3 to (V_{VP2} + 0.3)	V
SW3, OUT3 to GP3	-0.3 to (V_{VP3} + 0.3)	V
nIRQ, nLBO, nPBSTAT, nRSTO, nSTAT to GA	-0.3 to + 6	V
nPBIN, ACIN, CHGLEV, ISET, LBI, PWRHLD, PWREN, REFBP, SCL, SDA, TH, VSEL to GA	-0.3 to (VSYS + 0.3)	V
OUT4, OUT5, OUT6, OUT7 to GA	-0.3 to (V_{INL} + 0.3)	V
GP12, GP3 to GA	-0.3 to + 0.3	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Junction Temperature	125	°C
Maximum Power Dissipation TQFN55-40 (Thermal Resistance θ_{JA} = 30°C/W)	2.7	W
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

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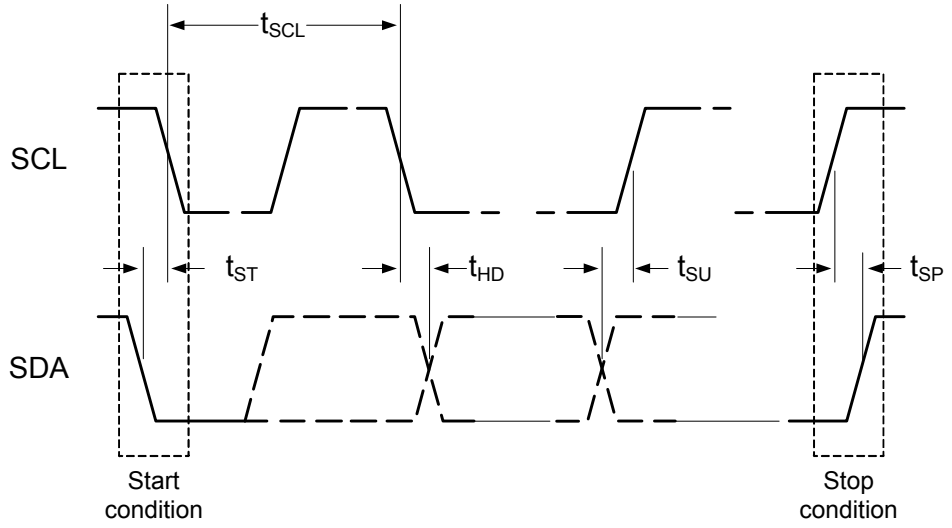
I²C INTERFACE ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{VSYS} = 3.1V to 5.5V, T_A = -40ºC to 85ºC			0.35	V
SCL, SDA Input High	V_{VSYS} = 3.1V to 5.5V, T_A = -40ºC to 85ºC	1.55			V
SDA Leakage Current				1	µA
SCL Leakage Current			8	18	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Period, t_{SCL}		1.5			µs
SDA Data Setup Time, t_{SU}		100			ns
SDA Data Hold Time, t_{HD}		300			ns
Start Setup Time, t_{ST}	For Start Condition	100			ns
Stop Setup Time, t_{SP}	For Stop Condition	100			ns

Figure 1:
I²C Compatible Serial Bus Timing



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GLOBAL REGISTER MAP

OUTPUT	ADDRESS		BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
SYS	0x00	NAME	TRST	nSYSMODE	nSYSLEVMSK	nSYSSTAT	SYSLEV[3]	SYSLEV[2]	SYSLEV[1]	SYSLEV[0]
		DEFAULT①	0	1	0	R	0	1	1	1
SYS	0x01	NAME	*Reserved*	*Reserved*	*Reserved*	*Reserved*	SCRATCH	SCRATCH	SCRATCH	SCRATCH
		DEFAULT①	0	0	0	0	0	0	0	0
REG1	0x20	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG1	0x21	NAME	*Reserved*	*Reserved*	VSET2[5]	VSET2[4]	VSET2[3]	VSET2[2]	VSET2[1]	VSET2[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG1	0x22	NAME	ON	PHASE	MODE	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	0	0	R
REG2	0x30	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	0	1	1	0	1	0
REG2	0x31	NAME	*Reserved*	*Reserved*	VSET2[5]	VSET2[4]	VSET2[3]	VSET2[2]	VSET2[1]	VSET2[0]
		DEFAULT①	0	0	0	1	1	0	1	0
REG2	0x32	NAME	ON	PHASE	MODE	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	0	0	R
REG3	0x40	NAME	*Reserved*	*Reserved*	VSET1[5]	VSET1[4]	VSET1[3]	VSET1[2]	VSET1[1]	VSET1[0]
		DEFAULT①	0	0	0	1	1	0	1	0
REG3	0x41	NAME	*Reserved*	*Reserved*	VSET2[5]	VSET2[4]	VSET2[3]	VSET2[2]	VSET2[1]	VSET2[0]
		DEFAULT①	0	0	0	1	1	0	1	0
REG3	0x42	NAME	ON	*Reserved*	MODE	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	0	0	0	0	0	0	R
REG4	0x50	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG4	0x51	NAME	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	1	0	0	0	0	0	R
REG5	0x54	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG5	0x55	NAME	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	1	0	0	0	0	0	R
REG6	0x60	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	0	1	1	0	0	0
REG6	0x61	NAME	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	1	0	0	0	0	0	R
REG7	0x64	NAME	*Reserved*	*Reserved*	VSET[5]	VSET[4]	VSET[3]	VSET[2]	VSET[1]	VSET[0]
		DEFAULT①	0	0	1	1	1	0	0	1
REG7	0x65	NAME	ON	DIS	LOWIQ	DELAY[2]	DELAY[1]	DELAY[0]	nFLTMSK	OK
		DEFAULT①	0	1	0	0	0	0	0	R
APCH	0x70	NAME	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*	*Reserved*
		DEFAULT①	0	1	0	1	0	0	0	0
APCH	0x71	NAME	SUSCHG	*Reserved*	TOTTIMO[1]	TOTTIMO[0]	PRETIMO[1]	PRETIMO[0]	OVPSET[1]	OVPSET[0]
		DEFAULT①	0	0	1	0	1	0	0	0
APCH	0x78	NAME	TIMRSTAT	TEMPSTAT	INSTAT	CHGSTAT	TIMRDAT	TEMPDAT	INDAT	CHGDAT
		DEFAULT①	0	0	0	0	R	R	R	R
APCH	0x79	NAME	TIMRTOT	TEMPIN	INCON	CHGEOCIN	TIMRPRE	TEMPOUT	INDIS	CHGEOCOUT
		DEFAULT①	0	0	0	0	0	0	0	0
APCH	0x7A	NAME	*Reserved*	*Reserved*	CSTATE[0]	CSTATE[1]	*Reserved*	*Reserved*	ACINSTAT	*Reserved*
		DEFAULT①	0	0	R	R	R	R	R	R

①: Default values of ACT8936QJ133-T.

②: All bits are automatically cleared to default values when the input power is removed or falls below the system UVLO.

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REGISTER AND BIT DESCRIPTIONS

Table 1:

Global Register Map

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
SYS	0x00	[7]	TRST	R/W	Reset Timer Setting. Defines the reset time-out threshold. Reset time-out is 65ms when value is 1, reset time-out is 260ms when value is 0. See *nRSTO Output* section for more information.
SYS	0x00	[6]	nSYSMODE	R/W	SYSLEV Mode Select. Defines the response to the SYSLEV voltage detector, 1: Generate an interrupt when V_{VSYS} falls below the programmed SYSLEV threshold, 0: automatic shutdown when V_{VSYS} falls below the programmed SYSLEV threshold.
SYS	0x00	[5]	nSYSLEVMSK	R/W	System Voltage Level Interrupt Mask. SYSLEV interrupt is masked by default, set to 1 to unmask this interrupt. See the *Programmable System Voltage Monitor* section for more information
SYS	0x00	[4]	nSYSSTAT	R	System Voltage Status. Value is 1 when V_{VSYS} is lower than the SYSLEV voltage threshold, value is 0 when V_{VSYS} is higher than the system voltage detection threshold.
SYS	0x00	[3:0]	SYSLEV	R/W	System Voltage Detect Threshold. Defines the SYSLEV voltage threshold. See the *Programmable System Voltage Monitor* section for more information.
SYS	0x01	[7:4]	-	R/W	Reserved.
SYS	0x01	[3:0]	SCRATCH	R/W	Scratchpad Bits. Non-functional bits, maybe be used by user to store system status information. Volatile bits, which are cleared when system voltage falls below UVLO threshold.
REG1	0x20	[7:6]	-	R	Reserved.
REG1	0x20	[5:0]	VSET1	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information.
REG1	0x21	[7:6]	-	R	Reserved.
REG1	0x21	[5:0]	VSET2	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG1	0x22	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG1	0x22	[6]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG1	0x22	[5]	MODE	R/W	Regulator Mode Select. Set bit to 1 for fixed-frequency PWM under all load conditions, clear bit to 0 to transit to power-savings mode under light-load conditions.
REG1	0x22	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG1, REG2, REG3 Turn-on Delay* section for more information.
REG1	0x22	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG1	0x22	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG2	0x30	[7:6]	-	R	Reserved.
REG2	0x30	[5:0]	VSET1	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information.
REG2	0x31	[7:6]	-	R	Reserved.

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REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG2	0x31	[5:0]	VSET2	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG2	0x32	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG2	0x32	[6]	PHASE	R/W	Regulator Phase Control. Set bit to 1 for the regulator to operate 180° out of phase with the oscillator, clear bit to 0 for the regulator to operate in phase with the oscillator.
REG2	0x32	[5]	MODE	R/W	Regulator Mode Select. Set bit to 1 for fixed-frequency PWM under all load conditions, clear bit to 0 to transit to power-savings mode under light-load conditions.
REG2	0x32	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG1, REG2, REG3 Turn-on Delay* section for more information.
REG2	0x32	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG2	0x32	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG3	0x40	[7:6]	-	R	Reserved.
REG3	0x40	[5:0]	VSET1	R/W	Primary Output Voltage Selection. Valid when VSEL is driven low. See the *Output Voltage Programming* section for more information.
REG3	0x41	[7:6]	-	R	Reserved.
REG3	0x41	[5:0]	VSET2	R/W	Secondary Output Voltage Selection. Valid when VSEL is driven high. See the *Output Voltage Programming* section for more information.
REG3	0x42	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG3	0x42	[6]	-	R/W	Reserved.
REG3	0x42	[5]	MODE	R/W	Regulator Mode Select. Set bit to 1 for fixed-frequency PWM under all load conditions, clear bit to 0 to transit to power-savings mode under light-load conditions.
REG3	0x42	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG1, REG2, REG3 Turn-on Delay* section for more information.
REG3	0x42	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG3	0x42	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG4	0x50	[7:6]	-	R	Reserved.
REG4	0x50	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG4	0x51	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG4	0x51	[6]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG4	0x51	[5]	LOWIQ	R/W	LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.
REG4	0x51	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG4, REG5, REG6, REG7 Turn-on Delay* section for more information.
REG4	0x51	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.

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REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
REG4	0x51	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG5	0x54	[7:6]	-	R	Reserved.
REG5	0x54	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG5	0x55	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG5	0x55	[6]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG5	0x55	[5]	LOWIQ	R/W	LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.
REG5	0x55	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG4, REG5, REG6, REG7 Turn-on Delay* section for more information.
REG5	0x55	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG5	0x55	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG6	0x60	[7:6]	-	R	Reserved.
REG6	0x60	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG6	0x61	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG6	0x61	[6]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG6	0x61	[5]	LOWIQ	R/W	LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.
REG6	0x61	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG4, REG5, REG6, REG7 Turn-on Delay* section for more information.
REG6	0x61	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG6	0x61	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.
REG7	0x64	[7:6]	-	R	Reserved.
REG7	0x64	[5:0]	VSET	R/W	Output Voltage Selection. See the *Output Voltage Programming* section for more information.
REG7	0x65	[7]	ON	R/W	Regulator Enable Bit. Set bit to 1 to enable the regulator, clear bit to 0 to disable the regulator.
REG7	0x65	[6]	DIS	R/W	Output Discharge Control. When activated, LDO output is discharged to GA through 1.5kΩ resistor when in shutdown. Set bit to 1 to enable output voltage discharge in shutdown, clear bit to 0 to disable this function.
REG7	0x65	[5]	LOWIQ	R/W	LDO Low-IQ Mode Control. Set bit to 1 for low-power operating mode, clear bit to 0 for normal mode.
REG7	0x65	[4:2]	DELAY	R/W	Regulator Turn-On Delay Control. See the *REG4, REG5, REG6, REG7 Turn-on Delay* section for more information.
REG7	0x65	[1]	nFLTMSK	R/W	Regulator Fault Mask Control. Set bit to 1 enable fault-interrupts, clear bit to 0 to disable fault-interrupts.
REG7	0x65	[0]	OK	R	Regulator Power-OK Status. Value is 1 when output voltage exceeds the power-OK threshold, value is 0 otherwise.

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REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
APCH	0x70	[7:0]	-	R	Reserved.
APCH	0x71	[7]	SUSCHG	R/W	Charge Suspend Control Input. Set bit to 1 to suspend charging, clear bit to 0 to allow charging to resume.
APCH	0x71	[6]	-	R/W	Reserved.
APCH	0x71	[5:4]	TOTTIMO	R/W	Total Charge Time-out Selection. See the *Charge Safety Timers* section for more information.
APCH	0x71	[3:2]	PRETIMO	R/W	Precondition Charge Time-out Selection. See the *Charge Safety Timers* section for more information.
APCH	0x71	[1:0]	OVPSET	R/W	Input Over-Voltage Protection Threshold Selection. See the *Input Over-Voltage Protection* section for more information.
APCH	0x78	[7]	TIMRSTAT①	R/W	Charge Time-out Interrupt Status. Set this bit with TIMRPRE[ ] and/or TIMRTOT[ ] to 1 to generate an interrupt when charge safety timers expire, read this bit to get charge time-out interrupt status. See the *Charge Safety Timers* section for more information.
APCH	0x78	[6]	TEMPSTAT①	R/W	Battery Temperature Interrupt Status. Set this bit with TEMPIN[ ] and/or TEMPOUT[ ] to 1 to generate an interrupt when a battery temperature event occurs, read this bit to get the battery temperature interrupt status. See the *Battery Temperature Monitoring* section for more information.
APCH	0x78	[5]	INSTAT	R/W	Input Voltage Interrupt Status. Set this bit with INCON[ ] and/or INDIS[ ] to generate an interrupt when UVLO or OVP condition occurs, read this bit to get the input voltage interrupt status. See the *Charge Current Programming* section for more information.
APCH	0x78	[4]	CHGSTAT①	R/W	Charge State Interrupt Status. Set this bit with CHGEOCIN[ ] and/or CHGEOCOUT[ ] to 1 to generate an interrupt when the state machine gets in or out of EOC state, read this bit to get the charger state interrupt status. See the *State Machine Interrupts* section for more information.
APCH	0x78	[3]	TIMRDAT①	R	Charge Timer Status. Value is 1 when precondition time-out or total charge time-out occurs. Value is 0 in other case.
APCH	0x78	[2]	TEMPDAT①	R	Temperature Status. Value is 0 when battery temperature is outside of valid range. Value is 1 when battery temperature is inside of valid range.
APCH	0x78	[1]	INDAT	R	Input Voltage Status. Value is 1 when a valid input at CHGIN is present. Value is 0 when a valid input at CHGIN is not present.
APCH	0x78	[0]	CHGDAT①	R	Charge State Machine Status. Value is 1 indicates the charger state machine is in EOC state, value is 0 indicates the charger state machine is in other states.
APCH	0x79	[7]	TIMRTOT	R/W	Total Charge Time-out Interrupt control. Set both this bit and TIMRSTAT[ ] to 1 to generate an interrupt when a total charge time-out occurs. See the *Charge Safety Timers* section for more information.
APCH	0x79	[6]	TEMPIN	R/W	Battery Temperature Interrupt Control. Set both this bit and TEMPSTAT[ ] to 1 to generate an interrupt when the battery temperature goes into the valid range. See the *Battery Temperature Monitoring* section for more information.

①: Valid only when CHGIN UVLO Threshold<V_{CHGIN}<CHGIN OVP Threshold.

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REGISTER AND BIT DESCRIPTIONS CONT'D

OUTPUT	ADDRESS	BIT	NAME	ACCESS	DESCRIPTION
APCH	0x79	[5]	INCON	R/W	Input Voltage Interrupt Control. Set both this bit and INSTAT[ ] to 1 to generate an interrupt when CHGIN input voltage goes into the valid range. See the *Charge Current Programming* section for more information.
APCH	0x79	[4]	CHGEOCIN	R/W	Charge State Interrupt Control. Set both this bit and CHGSTAT[ ] to 1 to generate an interrupt when the state machine goes into the EOC state. See the *State Machine Interrupts* section for more information.
APCH	0x79	[3]	TIMRPRE	R/W	PRECHARGE Time-out Interrupt control. Set both this bit and TIMRSTAT[ ] to 1 to generate an interrupt when a PRECHARGE time-out occurs. See the *Charge Safety Timers* section for more information.
APCH	0x79	[2]	TEMPOUT	R/W	Battery Temperature Interrupt Control. Set both this bit and TEMPSTAT[ ] to 1 to generate an interrupt when the battery temperature goes out of the valid range. See the *Battery Temperature Monitoring* section for more information.
APCH	0x79	[1]	INDIS	R/W	Input Voltage Interrupt Control. Set both this bit and INSTAT[ ] to 1 to generate an interrupt when CHGIN input voltage goes out of the valid range. See the *Charge Current Programming* section for more information.
APCH	0x79	[0]	CHGEOCOUT	R/W	Charge State Interrupt Control. Set both this bit and CHGSTAT[ ] to 1 to generate an interrupt when the state machines jumps out of the EOC state. See the *State Machine Interrupts* section for more information.
APCH	0x7A	[7:6]	-	R	Reserved.
APCH	0x7A	[5:4]	CSTATE	R	Charge State. Values indicate the current charging state. See the *State Machine Interrupts* section for more information.
APCH	0x7A	[3:2]	-	R	Reserved.
APCH	0x7A	[1]	ACINSTAT	R	ACIN Status. Indicates the state of the ACIN input, typically in order to identify the type of input supply connected. Value is 1 when ACIN is above the 1.2V precision threshold, value is 0 when ACIN is below this threshold.
APCH	0x7A	[0]	-	R	Reserved.

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SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		2.7		5.5	V
UVLO Threshold Voltage	V_{VSYS} Rising	2.2	2.45	2.65	V
UVLO Hysteresis	V_{VSYS} Falling		200		mV
Supply Current	REG1 and REG5 Enabled. REG2, REG3, REG4, REG6 and REG7 Disabled		185		μA
	REG1, REG2, REG3, REG4 and REG5 Enabled. REG6 and REG7 Disabled		350		
	REG1, REG2, REG3, REG4, REG5, REG6 and REG7 Enabled		420		
Shutdown Supply Current	All Regulators Disabled		8	18	μA
Oscillator Frequency		1.8	2	2.2	MHz
Logic High Input Voltage①		1.4			V
Logic Low Input Voltage				0.4	V
Leakage Current	V_{nIRQ} = V_{nRSTO} = 4.2V			1	μA
LBI Threshold Voltage	V_{BAT} Falling	1.03	1.2	1.31	V
LBI Hysteresis Threshold	V_{BAT} Rising		200		mV
Low Level Output Voltage②	I_{SINK} = 5mA			0.35	V
nRSTO Delay			260③		ms
Thermal Shutdown Temperature	Temperature rising		160		°C
Thermal Shutdown Hysteresis			20		°C

①: PWRHLD, PWREN, VSEL are logic inputs.

②: nLBO, nPBSTAT, nIRQ, nRSTO are open drain outputs.

③: Typical value shown. Actual value may vary from 227.9ms to 291.2ms.

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STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

(V_{VP1} = V_{VP2} = V_{VP3} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
UVLO Threshold	Input Voltage Rising	2.5	2.6	2.7	V
UVLO Hysteresis	Input Voltage Falling		100		mV
Quiescent Supply Current	Regulator Enabled		65	90	µA
Shutdown Current	V_{VP} = 5.5V, Regulator Disabled		0	1	µA
Output Voltage Accuracy	V_{OUT} ≥ 1.2V, I_{OUT} = 10mA	-1%	V_{NOM}①	1%	V
	V_{OUT} < 1.2V, I_{OUT} = 10mA	-2%	V_{NOM}①	2%	
Line Regulation	V_{VP} = Max (V_{NOM}① +1, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT} = 10mA to IMAX②		0.0017		%/mA
Power Good Threshold	V_{OUT} Rising		93		%V_{NOM}
Power Good Hysteresis	V_{OUT} Falling		2		%V_{NOM}
Oscillator Frequency	V_{OUT} ≥ 20% of V_{NOM}	1.8	2	2.2	MHz
	V_{OUT} = 0V		500		kHz
Soft-Start Period			400		µs
Minimum On-Time			75		ns
REG1					
Maximum Output Current		0.9			A
Current Limit		1.2	1.4	1.7	A
PMOS On-Resistance	I_{SW1} = -100mA		0.18		Ω
NMOS On-Resistance	I_{SW1} = 100mA		0.16		Ω
SW1 Leakage Current	V_{VP1} = 5.5V, V_{SW1} = 0 or 5.5V		0	1	µA
REG2					
Maximum Output Current		0.7			A
Current Limit		0.9	1.1	1.3	A
PMOS On-Resistance	I_{SW2} = -100mA		0.21		Ω
NMOS On-Resistance	I_{SW2} = 100mA		0.16		Ω
SW2 Leakage Current	V_{VP2} = 5.5V, V_{SW2} = 0 or 5.5V		0	1	µA
REG3					
Maximum Output Current		0.9			A
Current Limit		1.2	1.4	1.7	A
PMOS On-Resistance	I_{SW3} = -100mA		0.18		Ω
NMOS On-Resistance	I_{SW3} = 100mA		0.16		Ω
SW3 Leakage Current	V_{VP3} = 5.5V, V_{SW3} = 0 or 5.5V		0	1	µA

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

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LOW-NOISE LDO ELECTRICAL CHARACTERISTICS

(V_{INL} = 3.6V, C_{OUT4} = C_{OUT5} = 1.5μF, C_{OUT6} = C_{OUT7} = 2.2μF, LOWIQ[ ] = [0], T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.5		5.5	V
Output Voltage Accuracy	V_{OUT} ≥ 1.2V, T_A = 25°C, I_{OUT} = 10mA	-1%	V_{NOM}①	2%	V
	V_{OUT} < 1.2V, T_A = 25°C, I_{OUT} = 10mA	-2%	V_{NOM}①	4%	
Line Regulation	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V LOWIQ[ ] = [0]		0.05		mV/V
	V_{INL} = Max (V_{OUT} + 0.5V, 3.6V) to 5.5V LOWIQ[ ] = [1]		0.5		
Load Regulation	I_{OUT} = 1mA to IMAX②		0.08		V/A
Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 20mA, V_{OUT} =1.2V		75		dB
	f = 10kHz, I_{OUT} = 20mA, V_{OUT} =1.2V		65		
Supply Current per Output	Regulator Enabled, LOWIQ[ ] = [0]		37	60	μA
	Regulator Enabled, LOWIQ[ ] = [1]		31	52	
	Regulator Disabled		0	1	
Soft-Start Period	V_{OUT} = 2.9V		140		μs
Power Good Threshold	V_{OUT} Rising		89		%
Power Good Hysteresis	V_{OUT} Falling		3		%
Output Noise	I_{OUT} = 20mA, f = 10Hz to 100kHz, V_{OUT} = 1.2V		50		$μV_{RMS}$
Discharge Resistance	LDO Disabled, DIS[ ] = 1		1.5		kΩ
REG4					
Dropout Voltage③	I_{OUT} = 80mA, V_{OUT} > 3.1V		90	180	mV
Maximum Output Current		150			mA
Current Limit④	V_{OUT} = 95% of regulation voltage	200			mA
Stable C_{OUT4} Range		1.5		20	μF
REG5					
Dropout Voltage	I_{OUT} = 80mA, V_{OUT} > 3.1V		140	280	mV
Maximum Output Current		150			mA
Current Limit	V_{OUT} = 95% of regulation voltage	200			mA
Stable C_{OUT5} Range		1.5		20	μF
REG6					
Dropout Voltage	I_{OUT} = 120mA, V_{OUT} > 3.1V		90	180	mV
Maximum Output Current		250			mA
Current Limit	V_{OUT} = 95% of regulation voltage	300			mA
Stable C_{OUT6} Range		2.2		20	μF
REG7					
Dropout Voltage	I_{OUT} = 120mA, V_{OUT} > 3.1V		140	280	mV
Maximum Output Current		250			mA
Current Limit	V_{OUT} = 95% of regulation voltage	300			mA
Stable C_{OUT7} Range		2.2		20	μF

①: V_{NOM} refers to the nominal output voltage level for V_{OUT} as defined by the *Ordering Information* section.

②: IMAX Maximum Output Current.

③: Dropout Voltage is defined as the differential voltage between input and output when the output voltage drops 100mV below the regulation voltage (for 3.1V output voltage or higher)

④: LDO current limit is defined as the output current at which the output voltage drops to 95% of the respective regulation voltage.

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ActivePath™ CHARGER ELECTRICAL CHARACTERISTICS

(V_{CHGIN} = 5.0V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ActivePath					
CHGIN Operating Voltage Range		4.35		6.0	V
CHGIN UVLO Threshold	CHGIN Voltage Rising	3.1	3.5	3.9	V
CHGIN UVLO Hysteresis	CHGIN Voltage Falling		0.5		V
CHGIN OVP Threshold	CHGIN Voltage Rising	6.0	6.6	7.2	V
CHGIN OVP Hysteresis	CHGIN Voltage Falling		0.4		V
CHGIN Supply Current	V_{CHGIN} < V_{UVLO}		35	70	µA
	V_{CHGIN} < V_{BAT} + 50mV, V_{CHGIN} > V_{UVLO}		100	200	µA
	V_{CHGIN} > V_{BAT} + 150mV, V_{CHGIN} > V_{UVLO} Charger disabled, I_{VSYS} = 0mA		1.3	2.0	mA
CHGIN to VSYS On-Resistance	I_{VSYS} = 100mA		0.3		Ω
CHGIN to VSYS Current Limit	ACIN = VSYS	1.5	2		A
	ACIN = GA, CHGLEV = GA	80	90	100	mA
	ACIN = GA, CHGLEV = VSYS	400	450	500	
VSYS REGULATION					
VSYS Regulated Voltage	I_{VSYS} = 10mA	4.45	4.6	4.8	V
nSTAT OUTPUT					
nSTAT Sink current	V_{nSTAT} = 2V	4	8	12	mA
nSTAT Leakage Current	V_{nSTAT} = 4.2V			1	µA
ACIN AND CHGLEV INPUTS					
CHGLEV Logic High Input Voltage		1.4			V
CHGLEV Logic Low Input Voltage				0.4	V
CHGLEV Leakage Current	V_{CHGLEV} = 4.2V			1	µA
ACIN Voltage Thresholds	ACIN voltage rising	1.03	1.2	1.31	V
ACIN Hysteresis Voltage	ACIN voltage falling		200		mV
ACIN Leakage Current	V_{ACIN} = 4.2V			1	µA
TH INPUT					
TH Pull-Up Current	V_{CHGIN} > V_{BAT} + 100mV, Hysteresis = 50mV	91	102	110	µA
V_{TH} Upper Temperature Voltage Threshold (V_{THH})	Hot Detect NTC Thermistor	2.44	2.51	2.58	V
V_{TH} Lower Temperature Voltage Threshold (V_{THL})	Cold Detect NTC Thermistor	0.47	0.50	0.53	V
V_{TH} Hysteresis	Upper and Lower Thresholds		30		mV

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ActivePath™ CHARGER ELECTRICAL CHARACTERISTICS CONT'D

(V_{CHGIN} = 5.0V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CHARGER						
BAT Reverse Leakage Current	V_{CHGIN} = 0V, V_{BAT} = 4.2V, I_{VSYS} = 0mA			8		μA
BAT to VSYS On-Resistance				70		mΩ
ISET Pin Voltage	Fast Charge			1.2		V
	Precondition			0.13		
Charge Termination Voltage V_{TERM}	T_A = -20°C to 70°C		4.179	4.2	4.221	V
	T_A = -40°C to 85°C		4.170	4.2	4.230	
Charge Current	V_{BAT} = 3.8V R_{ISET} = 6.8K	ACIN = VSYS, CHGLEV = VSYS	-10%	I_{CHG} ①	+10%	mA
		ACIN = VSYS, CHGLEV = GA	-10%	I_{CHG}/5	+10%	
		ACIN = GA, CHGLEV = VSYS	400	450	500	
		ACIN = GA, CHGLEV = GA	80	90	100	
Precondition Charge Current	V_{BAT} = 2.7V R_{ISET} = 6.8K	ACIN = VSYS, CHGLEV = VSYS		10% I_{CHG}		mA
		ACIN = VSYS, CHGLEV = GA		10% I_{CHG}		
		ACIN = GA, CHGLEV = VSYS		45		
		ACIN = GA, CHGLEV = GA		45		
Precondition Threshold Voltage	V_{BAT} Voltage Rising		2.75	2.85	3.0	V
Precondition Threshold Hysteresis	V_{BAT} Voltage Falling			150		mV
END-OF-CHARGE Current Threshold	V_{BAT} = 4.15V,	ACIN = VSYS, CHGLEV = VSYS		10% I_{CHG}		mA
		ACIN = VSYS, CHGLEV = GA		10% I_{CHG}		
		ACIN = GA, CHGLEV = VSYS		45		
		ACIN = GA, CHGLEV = GA		45		
Charge Restart Threshold	V_{TERM} - V_{BAT}, V_{BAT} Falling		190	205	220	mV
Precondition Safety Timer	PRETIMO[ ] = 10			80		min
Total Safety Timer	TOTTIMO[ ] = 10			5		hr
Thermal Regulation Threshold				100		°C

①: R_{ISET} (kΩ) = 2336 × (1V/I_{CHG} (mA)) - 0.205

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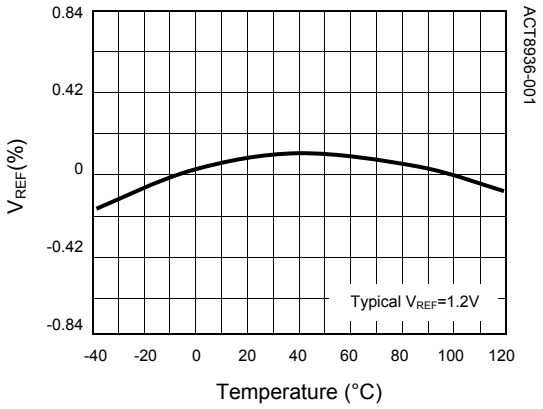
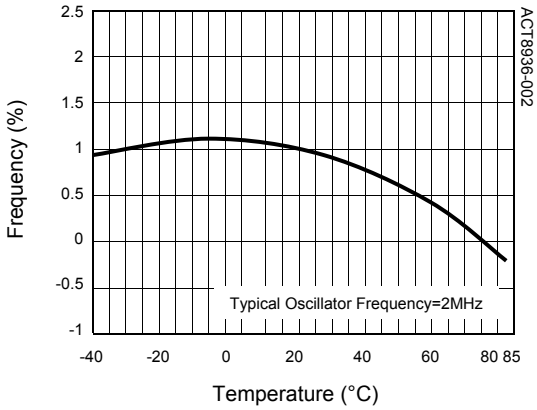
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{VSYS} = 3.6V, T_A = 25°C, unless otherwise specified.)

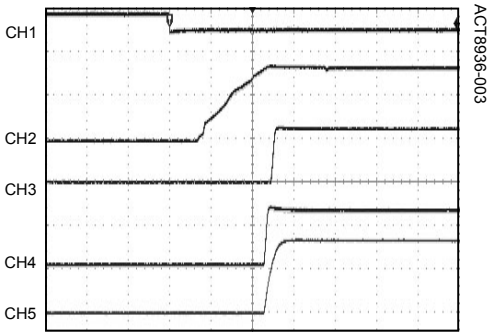
V_{REF} vs. Temperature



Frequency vs. Temperature

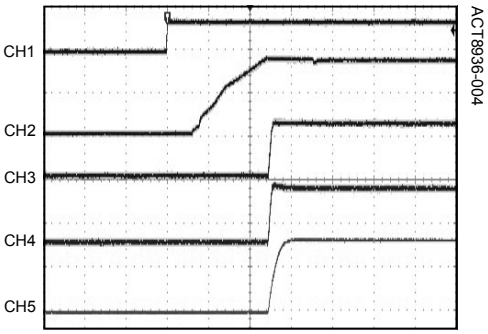


nPBIN Startup Sequence



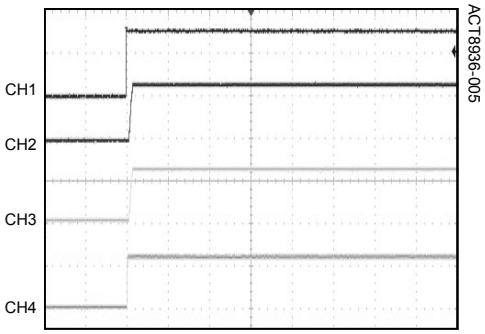
CH1: V_{nPBIN}, 5V/div
CH2: V_{OUT1}, 2V/div
CH3: V_{OUT5}, 1V/div
CH4: V_{OUT6}, 1V/div
CH5: V_{OUT7}, 2V/div
TIME: 400µs/div

PWRHLD Startup Sequence



CH1: V_{PWRHLD}, 5V/div
CH2: V_{OUT1}, 2V/div
CH3: V_{OUT5}, 1V/div
CH4: V_{OUT6}, 1V/div
CH5: V_{OUT7}, 2V/div
TIME: 400µs/div

PWREN Sequence



CH1: V_{PWREN}, 2V/div
CH2: V_{OUT2}, 1V/div
CH3: V_{OUT3}, 1V/div
CH4: V_{OUT4}, 1V/div
TIME: 2ms/div

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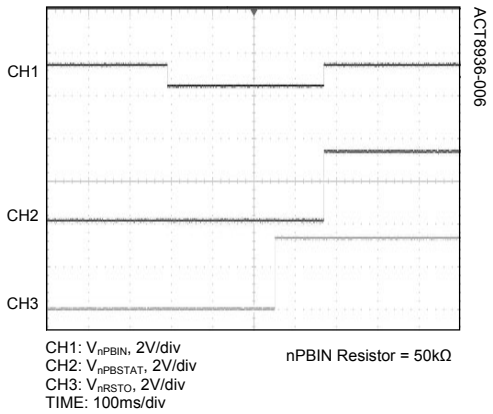
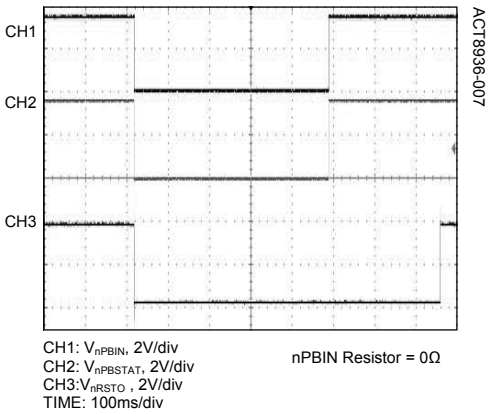
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

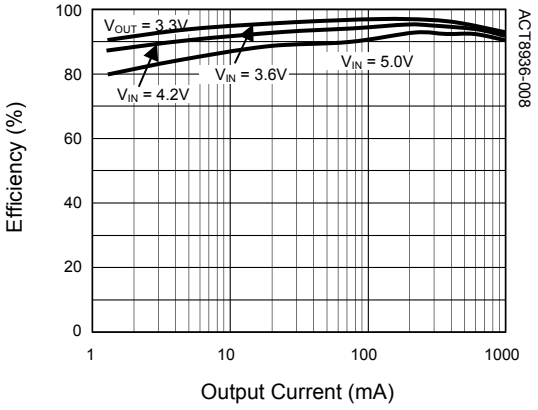
Push-Button Response (First Power-Up)



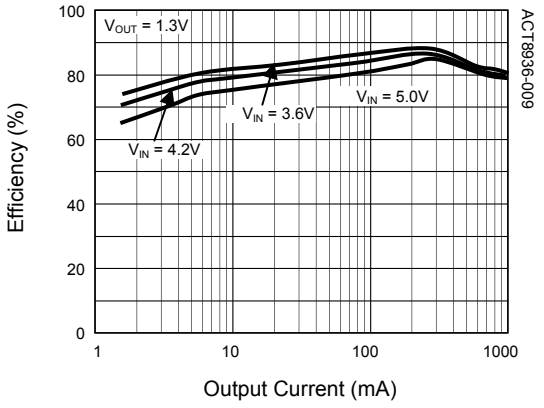
Manual Reset Response



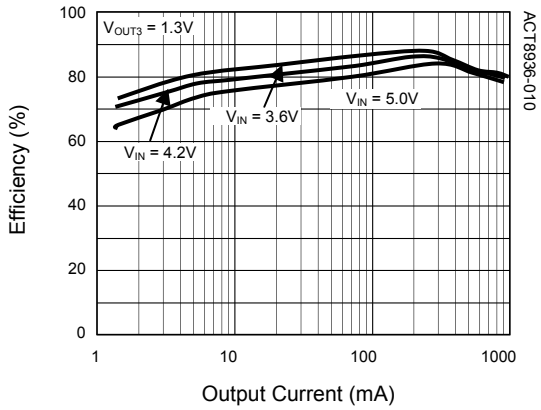
REG1 Efficiency vs. Output Current



REG2 Efficiency vs. Output Current



REG3 Efficiency vs. Output Current



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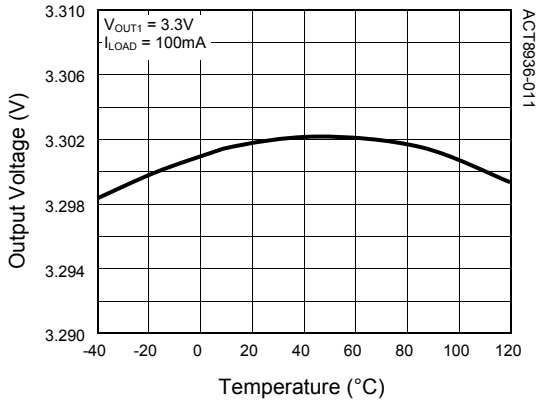
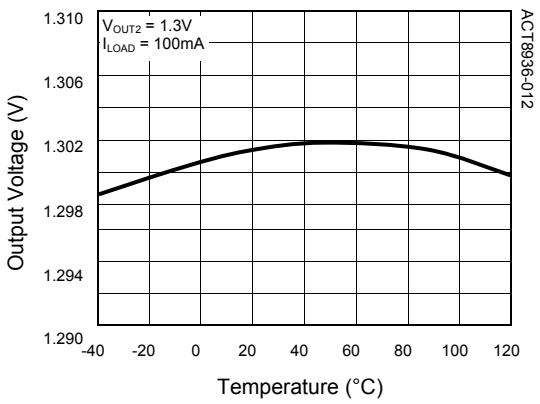
TYPICAL PERFORMANCE CHARACTERISTICS CONT'D

(T_A = 25°C, unless otherwise specified.)

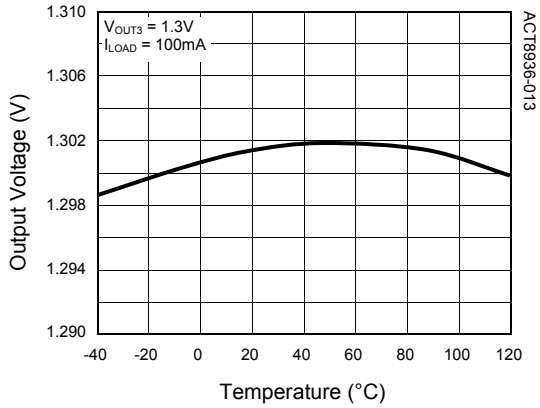
REG1 Output Voltage vs. Temperature



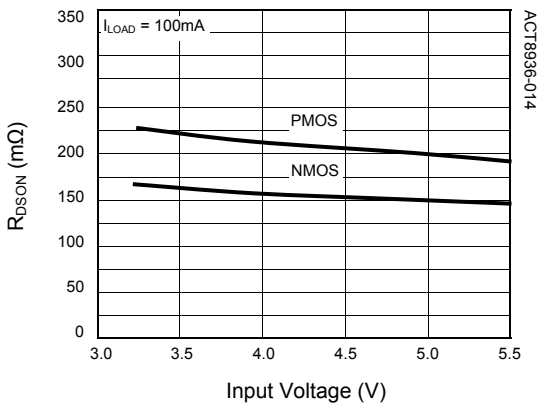
REG2 Output Voltage vs. Temperature



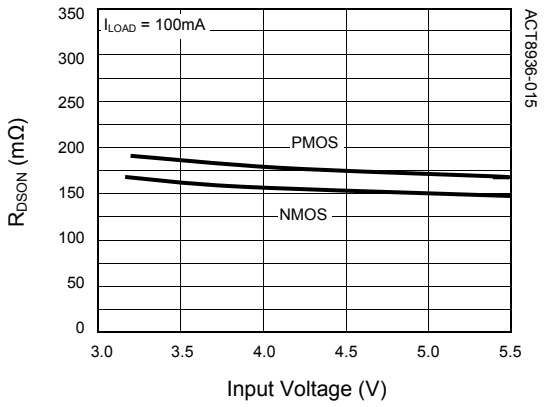
REG3 Output Voltage vs. Temperature



REG2 MOSFET Resistance



REG1, 3 MOSFET Resistance



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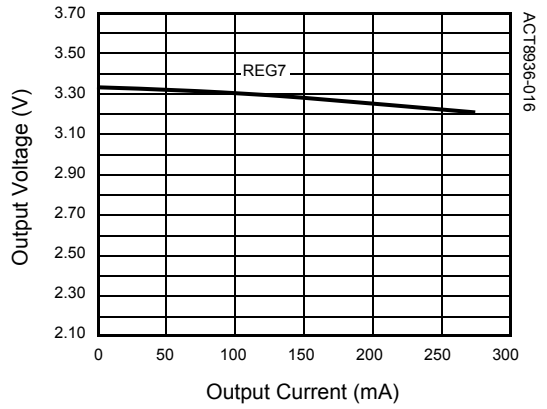
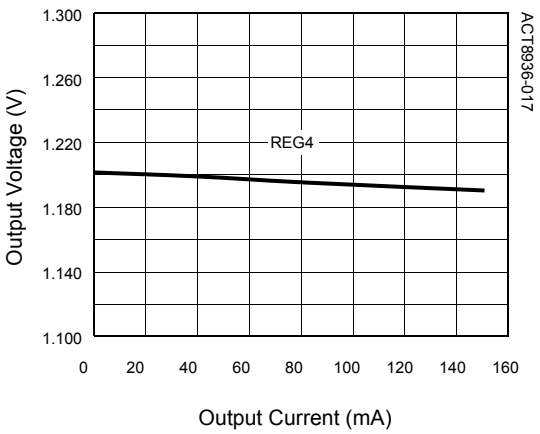
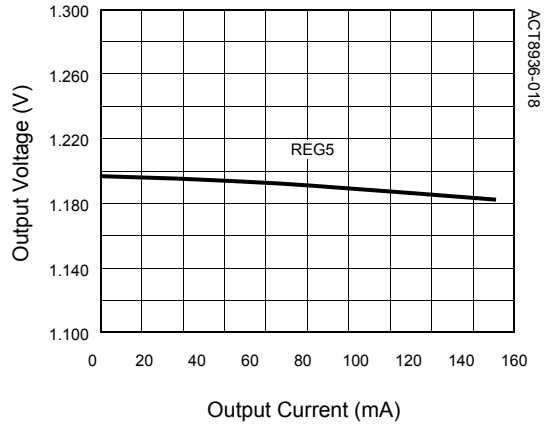
Output Voltage vs. Output Current



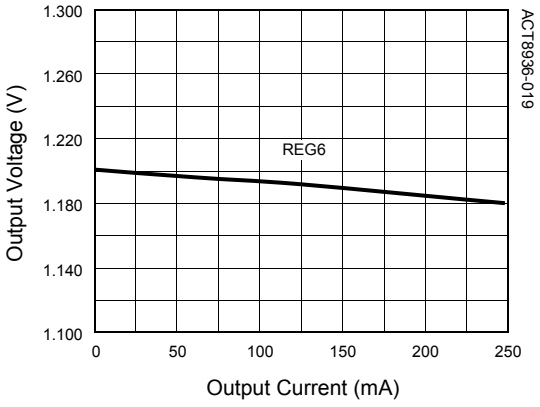
Output Voltage vs. Output Current



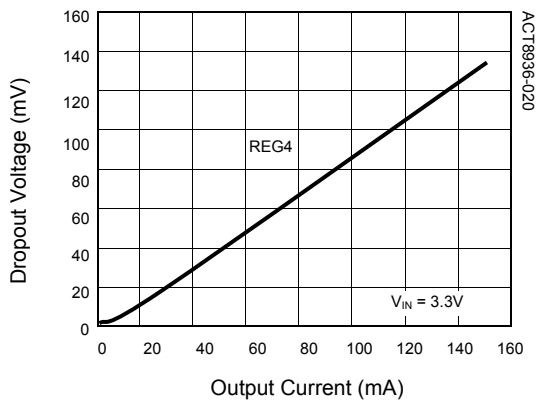
Output Voltage vs. Output Current



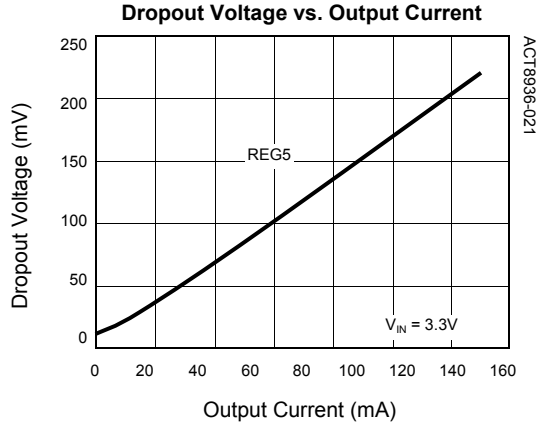
Output Voltage vs. Output Current



Dropout Voltage vs. Output Current



Dropout Voltage vs. Output Current



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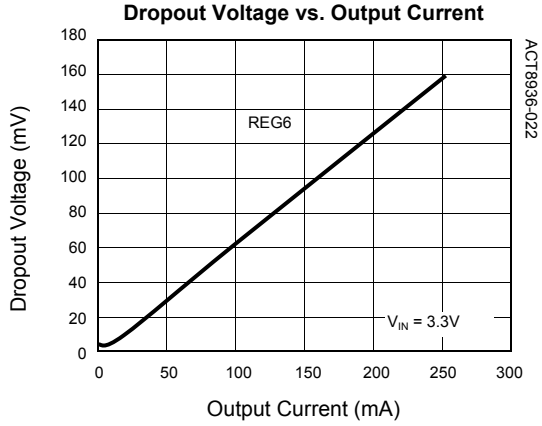
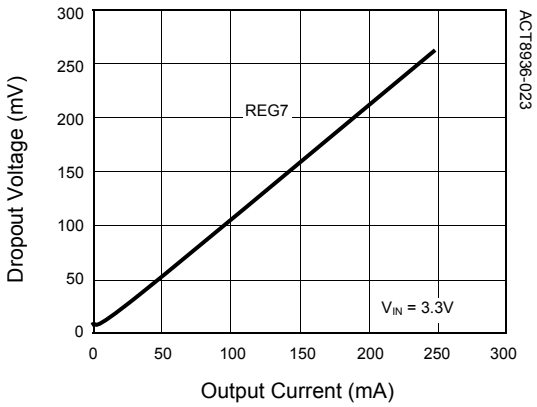
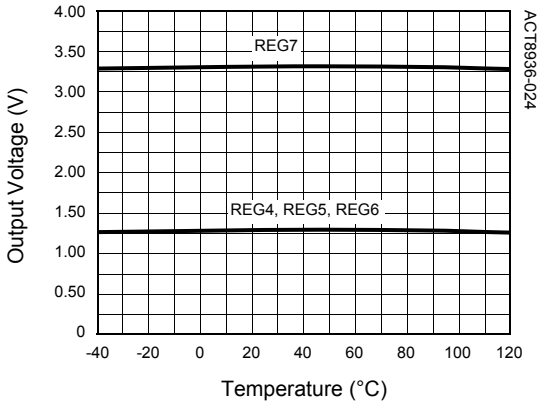
Dropout Voltage vs. Output Current



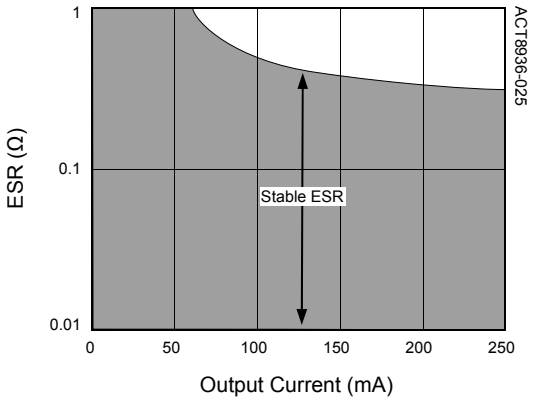
Dropout Voltage vs. Output Current



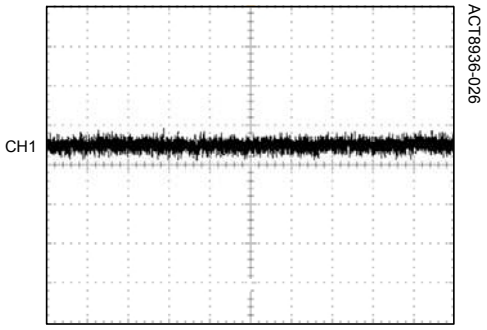
Output Voltage vs. Temperature



Region of Stable C_{OUT} ESR vs. Output Current



LDO Output Voltage Noise



CH1: V_{OUTx}, 200μV/div (AC COUPLED)
TIME: 200ms/div

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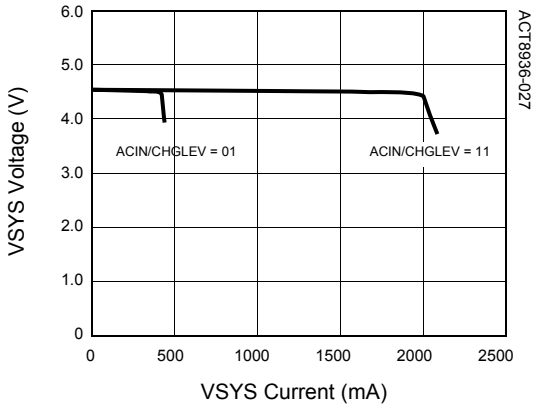
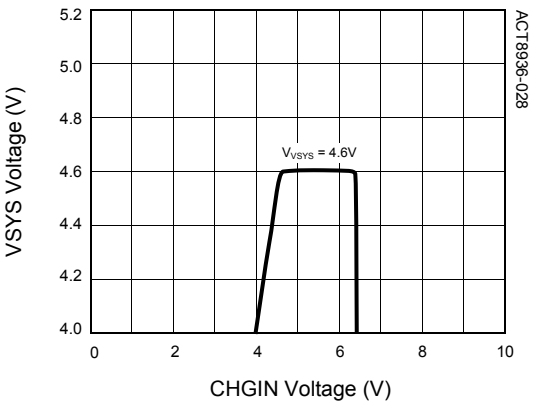
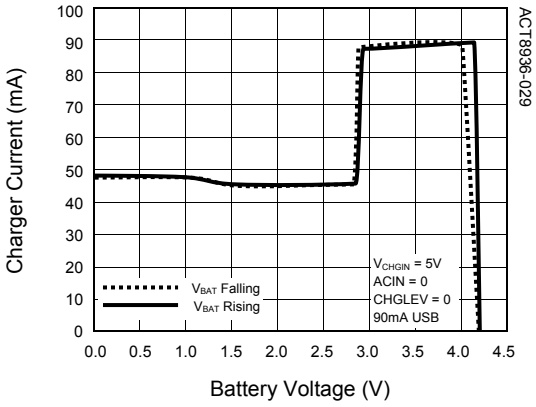
VSYS Voltage vs. VSYS Current



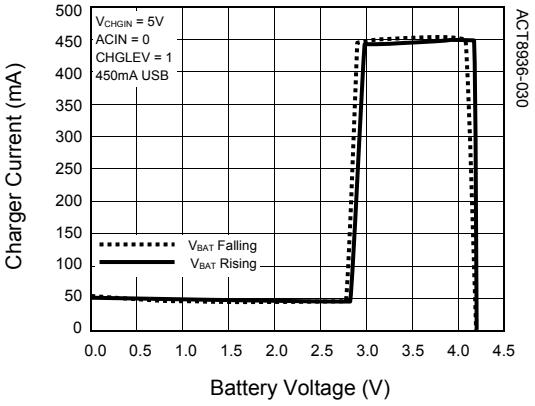
VSYS Voltage vs. CHGIN Voltage



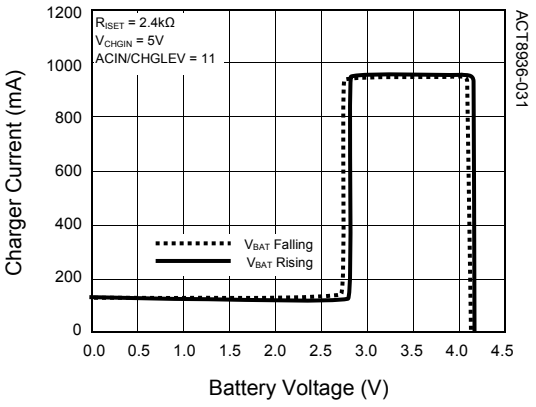
Charger Current vs. Battery Voltage



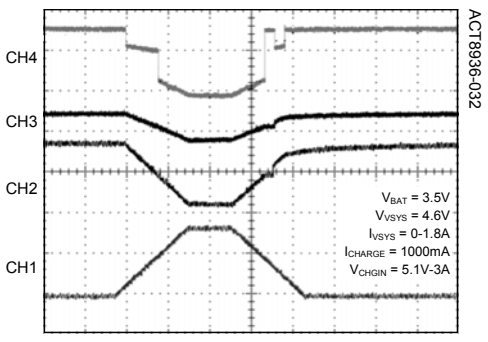
Charger Current vs. Battery Voltage



Charger Current vs. Battery Voltage



DCCC and Battery Supplement Modes



CH1: I_{VSYS}, 1.00A/div
CH2: I_{BAT}, 1.00A/div
CH3: V_{BAT}, 1.00V/div
CH4: V_{VSYS}, 1V/div
TIME: 200ms/div

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