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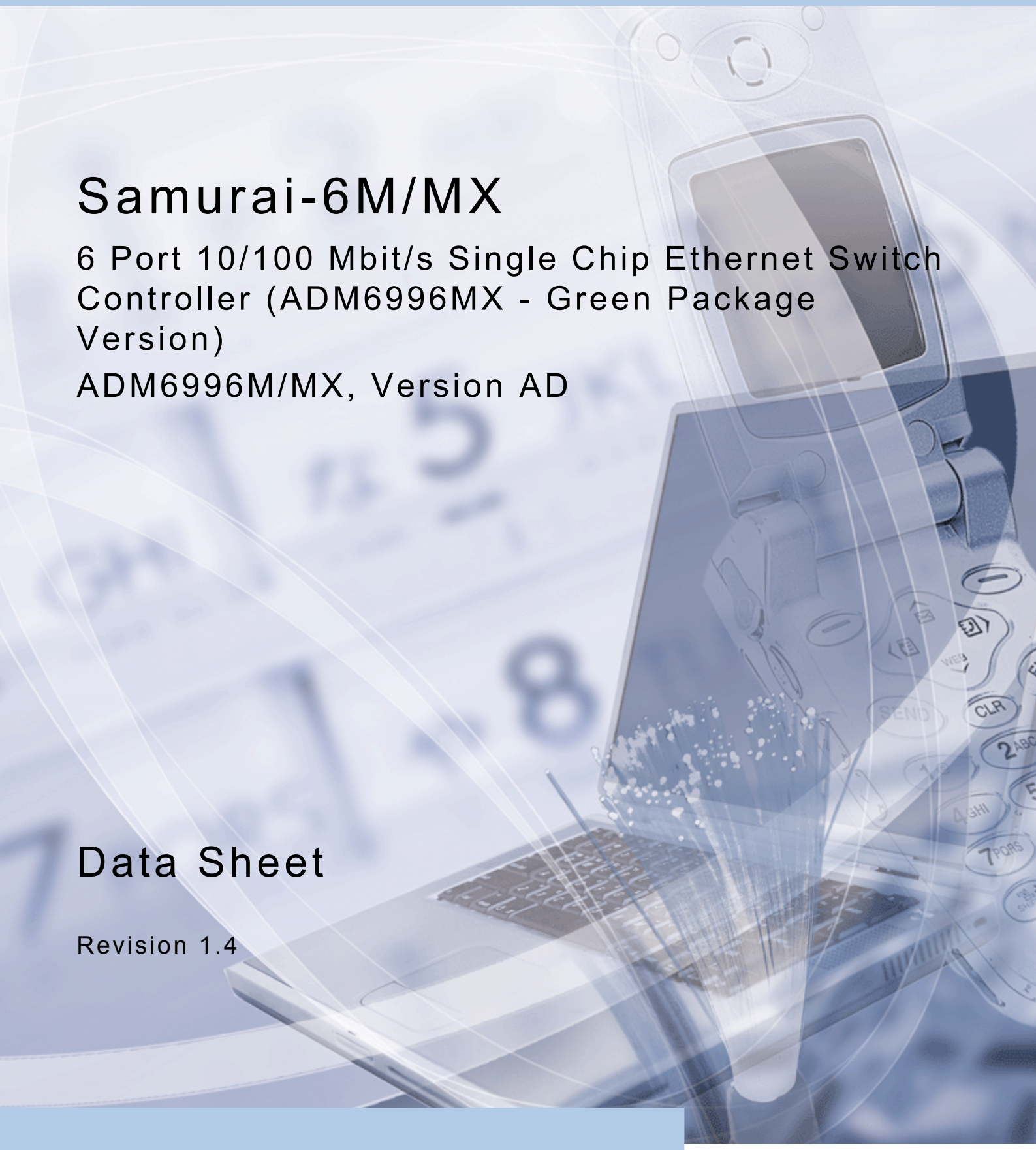
March 2006

Samurai-6M/MX

6 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller (ADM6996MX - Green Package Version)

ADM6996M/MX, Version AD



Data Sheet

Revision 1.4

Communication Solutions

Never stop thinking

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Revision History: 2006-03-24, Revision 1.4

Previous Version: Rev. 1.23	
Page/Date	**Subjects (major changes since last revision)**
Page 15	**Rev. 1.2: Modify analog pins number (RXP4-0, RXN4-0, TXP4-0 and TXN4-0)**
Page 81-82	Rev. 1.21: Rearrange $0E_H$ and $0F_H$ registers map
Page 22	Rev. 1.22: Modify LNKFP5 pin description/1_B, Link Failed
2005-07-04	Changed to the new Infineon format
2005-07-04	Rev. 1.22 changed to Rev. 1.23
2005-08-23	Rev 1.3: Update in content
2005-11-01	Revision 1.3 changed to Revision 1.31 Minor change. Included Green package information
2006-03-04	Revision 1.31 changed to Revision 1.4 Modify 3.1.10 Bandwidth Control and add Table 4 Bandwidth Control Timer Select Modify 3.1.15.3 and Figure 5 Configure Samurai QoS Function Correct Figure 10 Full duplex MAC to MAC MII Connection Add 29_H[10:9] register for BCTS and 29_H[8] register for BPM Add thermal resistance information

Trademarks

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1 Product Overview

1.1 Samurai-6M/6MX (ADM6996M/MX) Overview

The Samurai-6M/6MX (ADM6996M/MX) is a high performance, low cost, highly integrated (Controller, PHY and Memory) four 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and two MII port with one MII supporting GPSI/RMII. The Samurai-6M/6MX (ADM6996M/MX) is intended for applications such as stand alone bridges for the low cost SOHO markets such as 5-port switches and router applications. The Samurai-6MX (ADM6996MX) is the environmentally friendly “green” package version.

The Samurai-6M/6MX (ADM6996M/MX) provides functions such as: 802.1p(Q.O.S.), 802.1Q(VLAN), Port MAC address locking, management, port status, TP auto-MDIX, 25M crystal & extra MII port functions to meet customer requests on switch demand.

The Samurai-6M/6MX (ADM6996M/MX) also supports back pressure in Half-Duplex mode and the 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet loss when buffers are full. When Back Pressure is enabled, and there is no receive buffer available for the incoming packet, the Samurai-6M/6MX (ADM6996M/MX) will issue a JAM pattern on the receiving port in Half Duplex mode and issue the 802.3x Pause packet back to the receiving end in Full Duplex mode.

The built-in SRAM used for the packet buffer is divided into 256 bytes per block to achieve the optimized memory utilization through complicated link lists on packets with various lengths.

The Samurai-6M/6MX (ADM6996M/MX) also supports priority features using Port-Based, VLAN and IP TOS field checking. Users can easily set different priority modes in individual ports, through a small low-cost micro controller when initializing or configuring on-the-fly. Each output port supports four queues in the way of fixed N: 1 fairness queuing to fit the bandwidth demand on various types of packets such as Voice, Video and Data. 802.1Q, Tag/Untag, and up to 16 groups of VLAN are also supported.

An intelligent address recognition algorithm allows Samurai-6M/6MX (ADM6996M/MX) to recognize up to 2K different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by Samurai-6M/6MX (ADM6996M/MX) to use on building Internet access to prevent multiple users sharing one port.

1.2 Features

- Supports four 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and two MII port with one MII supporting GPSI/RMII
- Supports four 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces, one MII port (for CPU LAN MII) and one isolated PHY(for CPU WAN MII).Five 10M/100M auto-detect Half/Full duplex switch ports with **TX/FX** interfaces
- 2K MAC address tables with 4-ways associative hash algorithm
- 6KX64 bits packet buffers are divided into 192 blocks of 256 bytes each
- Four queues for QoS
- Priority features by Port-Based, 802.1p, IP TOS, Diffserv, TCP/UDP Port Application-Based of packets
- Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed
- Single/Dual color LED mode with Power On auto diagnostic. Collision/Duplex LED can be separated using register setting
- 802.3x Flow Control pause packet for Full Duplex
- Back Pressure function for Half Duplex operation
- Supports packet lengths up to 1518/1522 (Default)/1536/1784 bytes in maximum
- Scalable Per Port Bandwidth Control (Both Ingress and Egress).
- Broadcast/Multicast Storm Suppression

- 802.1Q VLAN. Up to 16 VLAN groups are implemented by full 12 bits VID matching
- MAC clone function to enable multiple WAN application
- TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Interrupt pin, Interrupt Register and Interrupt Mask Register. Programmable interrupt polarity (Default active low)
- Easy Management 32-bit smart counter for per port RX/TX byte/packet count, 16-bit smart counter for per port ERROR count and Collision count
- Supports 32 hardware IGMP Table (Multicast Table)
- MAC Address Table is accessible
- Supports 802.1x security function
- Supports Spanning Tree Protocol
- Supports internal counter/PHY status output for management system
- 25M Crystal
- 128 QFP package with 0.18 μm technology. 1.8 V/3.3 V power supply.
- 1.0 W low power consumption.

1.3 Applications

Samurai-6M/6MX (ADM6996M/MX):

- SOHO 5-port switch
- 5-port switch + Router with 2 MII CPU interface

1.4 Block Diagram

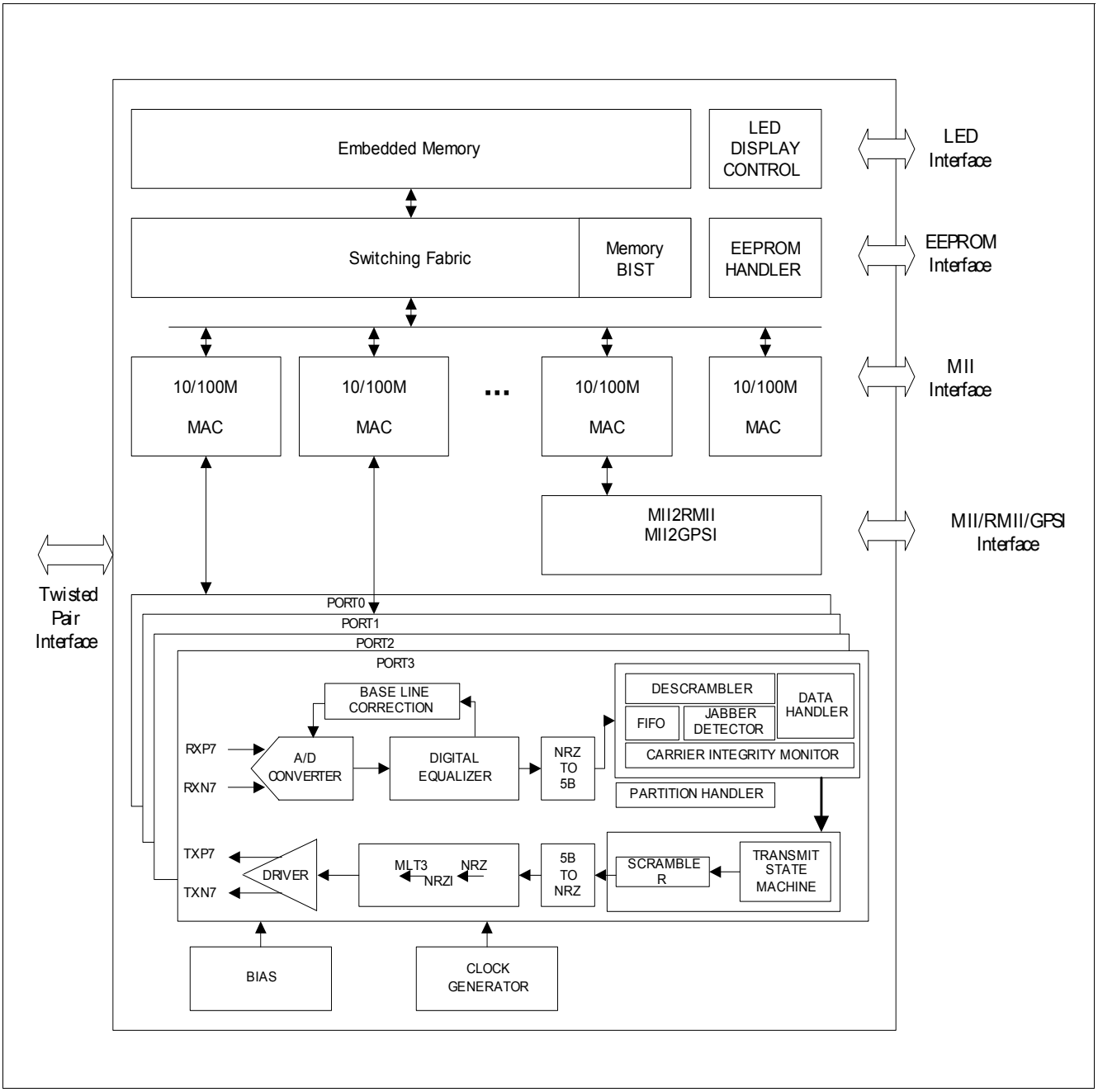

Figure 1 Samurai-6M/6MX (ADM6996M/MX) Block Diagram

1.5 Data Lengths

qword: 64 bits

dword: 32 bits

word: 16 bits

byte: 8 bits

nibble: 4 bits

2 Interface Description

This chapter describes the interface descriptions for the Samurai-6M/6MX (ADM6996M/MX)

- Pin Diagram
- Abbreviations
- Pin Description by Function

2.1 Pin Diagram

Figure 2 shows the pin diagram for the Samurai-6M/6MX (ADM6996M/MX).

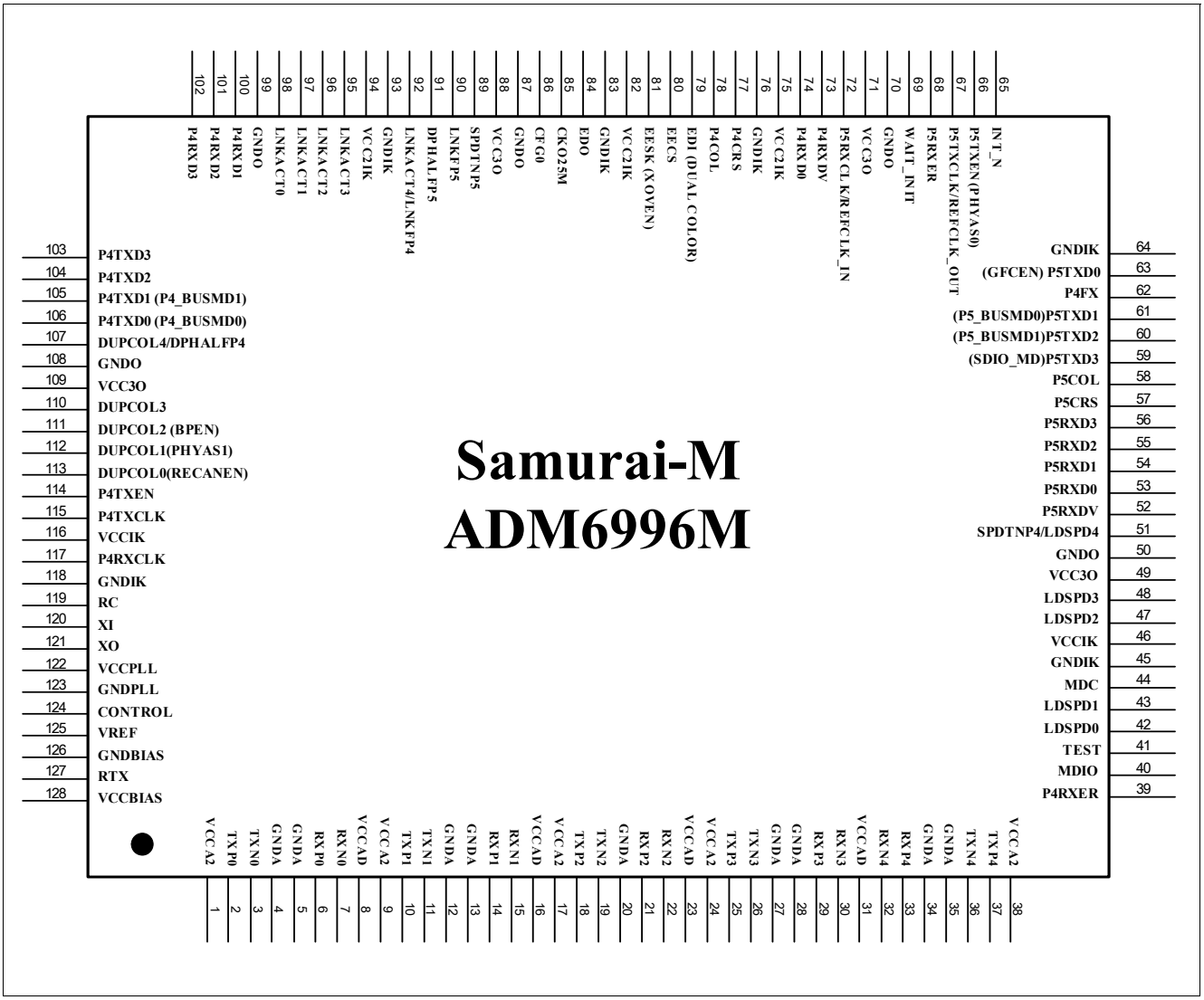

Figure 2 4 TP/FX PORT + 2 MII PORT 128 Pin Diagram

2.2 Abbreviations

Standard abbreviations for I/O tables:

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU	Pull up, 10 kΩ
PD	Pull down, 10 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.3 Pin Description by Function

Samurai-6M/6MX (ADM6996M/MX) pins are categorized into one of the following groups:

- Network Media Connection
- Port 4 MII Interface
- Port 5 MII Interface
- LED Interface
- EEPROM Interface
- Power/Ground, 48 pins
- Miscellaneous

*Note: **Table 1** can be used for reference.*

Table 3 IO Signals

Ball No.	Name	Pin Type	Buffer Type	Function
Network Media Connection				
33	RXP_4	AI/O	ANA	**Receive Pair** Differential data is received on this pin.
29	RXP_3			
21	RXP_2			
14	RXP_1			
6	RXP_0			
32	RXN_4	AI/O	ANA	
30	RXN_3			
22	RXN_2			
15	RXN_1			
7	RXN_0			
37	TXP_4	AI/O	ANA	**Transmit Pair** Differential data is transmitted on this pin.
25	TXP_3			
18	TXP_2			
10	TXP_1			
2	TXP_0			
36	TXN_4	AI/O	ANA	
26	TXN_3			
19	TXN_2			
11	TXN_1			
3	TXN_0			
Port 4 MII Interface				
74	MMII_P4RXD0	I	PD, LVTTL	**Port 4 Receive Data Bit 0 in MAC MII Mode** In MAC MII mode, the bit is the LSB of MII receive data, synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD0	O	8 mA, PD, LVTTL	**Port 4 Receive Data Bit 0 in PCS MII Mode** When port 4 is operating in PCS MII mode, the bit is the LSB of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.
102	MMII_P4RXD3	I	PD, LVTTL	**Port 4 Receive Data Bit 3 in MAC MII Mode** In MAC MII mode, this bit is bit[3] of MII receive data, and synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD3	O	8 mA, PD, LVTTL	**Port 4 Receive Data Bit 3 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[3] of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
101	MMII_P4RXD2	I	PD, LVTTL	**Port 4 Receive Data Bit 2 in MAC MII Mode** In MAC MII mode, this pin is bit[2] of MII receive data, and synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD2	O	8 mA, PD, LVTTL	**Port 4 Receive Data Bit 2 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[2] of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.
100	MMII_P4RXD1	I	PD, LVTTL	**Port 4 Receive Data Bit 1 in MAC MII Mode** In MAC MII mode, this pin is bit[1] of MII receive data, and synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD1	O	8 mA, PD, LVTTL	**Port 4 Receive Data Bit 1 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[1] of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.
73	MMII_P4RXDV	I	PD, LVTTL	**Port 4 Receive Data Valid in MAC MII Mode** Active high to indicate that the data on MMII_P4RXD[3:0] is valid. Synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXDV	O	8 mA, PD, LVTTL	**Port 4 Receive Data Valid in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is an active high output signal to indicate PMII_P4RXD[3:0] is valid. Synchronous to the rising edge of PMII_P4RXCLK.
39	MII_P4RXER	I	PD, LVTTL	**Port 4 Receive Error in MAC MII Mode** Active high to indicate that there is symbol error on the MII_P4RXD[3:0]. Only valid in 100M operation.
77	MMII_P4CRS	I	PD, LVTTL	**Port 4 Carrier Sense in MAC MII Mode** In full duplex mode, MMII_P4CRS reflects the receive carrier sense situation on medium only; In Half Duplex, CRS will be high both in receive and transmit condition.
	PMII_P4CRS	O	8 mA, PD, LVTTL	**Port 4 Carrier Sense in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is used to output Carrier Sense status.
78	MMII_P4COL	I	PD, LVTTL	**Port 4 Collision input in MAC MII Mode** Active high to indicate that there is collision on the medium. Stay low in full duplex operation.
	PMII_P4COL	O	8 mA, PD, LVTTL	**Port 4 Collision output in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is used to output collision status.

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
106	P4_BUSMD0	I	PD, LVTTL	**Port 4 Bus Type Configuration 0** Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(**RC**) for Port 4 Configuration Bit 0. Combined with **CFG0** and **P4_BUSMD1**, Samurai-6M/6MX (ADM6996M/MX) provides 4 bus type for port 4. See **CFG0** pin description for more details. *Note: Power On Setting*
	MMII_P4TXD0	O	8 mA, PD, LVTTL	**Port 4 Transmit Data Bit 0 in MAC MII Mode** The LSB bit of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD0	I	PD, LVTTL	**Port 4 Transmit Data Bit 0 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is the LSB of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.
105	P4_BUSMD1	I	PD, LVTTL	**Port 4 Bus Type Configuration 1** Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(**RC**) for Port 4 Configuration Bit 1. Combined with **CFG0** and **P4_BUSMD0**, Samurai-6M/6MX (ADM6996M/MX) provides 4 bus type for port 4. See **CFG0** for more details. *Note: Power On Setting*
	MMII_P4TXD1	O	8 mA, PD, LVTTL	**Port 4 Transmit Data Bit 1 in MAC MII Mode** The bit[1] of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD1	I	PD, LVTTL	**Port 4 Transmit Data Bit 1 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[1] of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.
103	MMII_P4TXD3	O	8 mA, PD, LVTTL	**Port 4 Transmit Data Bit 3 in MAC MII Mode** The bit[3] of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD3	I	PD, LVTTL	**Port 4 Transmit Data Bit 3 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[3] of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.
104	MMII_P4TXD2	O	8 mA, PD, LVTTL	**Port 4 Transmit Data Bit 2 in MAC MII Mode** The bit[2] of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD2	I	PD, LVTTL	**Port 4 Transmit Data Bit 2 in PCS MII Mode** When port 4 is operating in PCS MII mode, this pin is bit[2] of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
114	MMII_P4TXEN	O	8 mA, PD, LVTTL	**Port 4 Transmit Enable in MAC MII Mode** Output by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of MMII_P4TXCLK when Samurai-6M/6MX (ADM6996M/MX) is programmed to MAC Type MII.
	PMII_P4TXEN	I	PD, LVTTL	**Port 4 Transmit Enable in PCS MII Mode** It is the MII Transmit Enable input to Samurai-6M/6MX (ADM6996M/MX) when programmed to PCS Type MII.
117	MMII_P4RXCLK	I	PD, LVTTL	**Port 4 Receive Clock in MAC MII Mode** 25MHz Free Running clock in 100M Mode and 2.5 MHz free running clock in 10M Mode. MMII_P4RXDV and MMII_P4RXD[3:0] should be synchronous to the rising edge of this clock
	PMII_P4RXCLK	O	8 mA, PD, LVTTL	**Port 4 Receive Clock in PCS MII Mode** 25MHz Free Running clock in 100M Mode and 2.5 MHz free running clock in 10M Mode. PMII_P4RXDV and PMII_P4RXD[3:0] should be synchronous to the rising edge of this clock
115	MMII_P4TXCLK	I	PD, LVTTL	**Port 4 Transmit Clock in MAC MII Mode** 25MHz Free Running clock in 100M Mode and 2.5 MHz free running clock in 10M Mode. MMII_P4TXEN and MMII_P4TXD[3:0] should be synchronous to the rising edge of this clock
	PMII_P4TXCLK	O	8 mA, PD, LVTTL	**Port 4 Transmit Clock in PCS MII Mode** 25MHz Free Running clock in 100M Mode and 2.5 MHz free running clock in 10M Mode. PMII_P4TXEN and PMII_P4TXD[3:0] should be synchronous to the rising edge of this clock
62	P4FX	I	PD, LVTTL	**Port 4 Fiber Selection for PCS MII/PHY mode** During power on reset, value will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(**RC**) as port 4 Fiber select. 0_B Twisted Pair Mode 1_B Fiber Mode

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
Port 5 MII Interface				
63	GFCEN	I	PU, LVTTL	**Global Flow Control Enable** Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(**RC**) as Flow control enable. *Note: Power On Setting* 0_B Flow Control Capability is depended upon the register setting in corresponding port's Basic Control Register 1_B All ports flow control capability is enabled
	MII_P5TXD0	O	4 mA, PU, LVTTL	**Port 5 Transmit Data Bit 0 in MII Mode** The LSB bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
	GPSI_P5TXD	O	4 mA, PU, LVTTL	**Port 5 Transmit Data in GPSI Mode** When port 5 is operating in GPSI mode, this pin acts as GPSI Transmit Data. Synchronous to the rising edge of GPSI_P5TXCLK.
	RMII_P5TXD0	O	4 mA, PU, LVTTL	**Port 5 Transmit Data Bit 0 in RMII Mode** When port 5 is operating in RMII mode, this pin acts as RMII Transmit Data Bit[0]. Synchronous to the rising edge of REFCLK_IN.
61	P5_BUSMD0	I	PD, LVTTL	**Port 5 Bus Mode Selection Bit 0** Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(**RC**) as port 5 bus mode selection bit 0. Combined with **P5_BUSMD1**, Samurai-6M/6MX (ADM6996M/MX) provides 3 bus types for port 5. P5_BUSMD[1:0], Interface *Note: Power On Setting* 00_B MII 01_B GPSI 10_B RMII 11_B Reserved and not allowed
	MII_P5TXD1	O	4 mA, PD, LVTTL	**Port 5 Transmit Data Bit 1 in MII Mode** The bit[1] of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
	RMII_P5TXD1	O	4 mA, PD, LVTTL	**Port 5 Transmit Data Bit 1 in RMII Mode** The bit[1] of RMII Transmit data of port 5. Synchronous to the rising edge of REFCLK_IN.

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
60	P5_BUSMD1	I	PD, LVTTL	**Port 5 Bus Mode Selection Bit 1** Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(**RC**) as port 5 bus mode selection bit 1. See **P5_BUSMD0** for more details. *Note: Power On Setting*
	MII_P5TXD2	O	4 mA, PD, LVTTL	**Port 5 Transmit Data Bit 2 in MII Mode** The bit[2] of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
59	SDIO_MD	I	PD, LVTTL	**SDC/SDIO Mode Selection** Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(**RC**) as **SDC**/**SDIO** control signal which is used to select 16 bit mode. *Note: Power On Setting* 0_B 16 bits mode, MDC/MDIO timing compatible
	MII_P5TXD3	O	4 mA, PD, LVTTL	**Port 5 Transmit Data Bit 3 in MII Mode** The MSB bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
66	PHYAS0	I	PD, LVTTL	**PHY Address MSB Bit 0** During power on reset, value will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(**RC**) as PHY start address select. PHYAS[1:0] = 00_B and PHY address starts from 01000_B. *Note: Power On Setting*
	MII_P5TXEN	O	8 mA, PD, LVTTL	**Port 5 Transmit Enable TXEN in MII Mode** Active high to indicate that the data on MII_P5TXD[3:0] is valid. Synchronous to the rising edge of MII_P5TXCLK.
	GPSI_P5TXEN	O	8 mA, PD, LVTTL	**Port 5 Transmit Enable TXEN in GPSI Mode** Active high to indicate that the data on GPSI_P5TXD is valid. Synchronous to the rising edge of GPSI_P5TXCLK.
	RMII_P5TXEN	O	8 mA, PD, LVTTL	**Port 5 Transmit Enable TXEN in RMII Mode** Active high to indicate that the data on RMII_P5TXD[1:0] is valid. Synchronous to the rising edge of REFCLK_IN.
53	MII_P5RXD0	I	PD, LVTTL	**Port 5 Receive Data Bit 0 in MII Mode** In MII mode, the bit is the LSB of MII receive data, synchronous to the rising edge of MII_P5RXCLK.
	GPSI_P5RXD	I	PD, LVTTL	**Port 5 Receive Data in GPSI Mode** In GPSI Mode, this acts as Receive Data Input, synchronous to the rising edge of GPSI_P5RXCLK.
	RMII_P5RXD0	I	PD, LVTTL	**Port 5 Receive Data Bit 0 in RMII Mode** In RMII mode, the bit is the LSB of RMII receive data, synchronous to the rising edge of REFCLK_IN.

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
54	MII_P5RXD1	I	PD, LVTTL	**Port 5 Receive Data Bit 1 in MII Mode** In MII mode, the bit is the bit[1] of MII receive data, synchronous to the rising edge of MII_P5RXCLK.
	RMII_P5RXD1	I	PD, LVTTL	**Port 5 Receive Data Bit 1 in RMII Mode** In RMII mode, the bit is the MSB of RMII receive data, synchronous to the rising edge of REFCLK_IN.
55	MII_P5RXD2	I	PD, LVTTL	**Port 5 Receive Data Bit 2 in MII Mode** In MII mode, the bit is the bit[2] of MII receive data. Synchronous to the rising edge of MII_P5RXCLK.
56	MII_P5RXD3	I	PD, LVTTL	**Port 5 Receive Data Bit 3 in MII Mode** In MII mode, the bit is the bit[3] of MII receive data. Synchronous to the rising edge of MII_P5RXCLK.
52	MII_P5RXDV	I	PD, LVTTL	**Port 5 Receive Data Valid in MII Mode** Active high to indicate that the data on MII_P5RXD[3:0] is valid. Synchronous to the rising edge of MII_P5RXCLK.
	RMII_P5 CRSDV	I	PD, LVTTL	**Port 5 Carrier Sense and Receive Data Valid in RMII Mode** Active high to indicate that the data on RMII_P5RXD[1:0] is valid. Synchronous to the rising edge of REFCLK _IN.
68	MII_P5RXER	I	PD, LVTTL	**Port 5 Receive Error in MII Mode** Active high to indicate that there is symbol error on the MII_P5RXD[3:0]. Only valid in 100M operation.
	RMII_P5RXER	I	PD, LVTTL	**Port 5 Receive Error in RMII Mode** Active high to indicate that there is symbol error on the RMII_P5 RXD[1:0]. Only valid in 100M operation.
57	MII_P5CRS	I	PD, LVTTL	**Port 5 Carrier Sense in MII Mode** In full duplex mode, MII_P5CRS reflects the receive carrier sense situation on medium only; In Half Duplex, MII_P5CRS will be high both in receive and transmit condition.
	GPSI_P5CRS	I	PD, LVTTL	**Port 5 Carrier Sense in GPSI Mode** In full duplex mode, GPSI_P5CRS reflects the receive carrier sense situation on medium only; In Half Duplex, GPSI_P5CRS will be high both in receive and transmit condition.
58	MII_P5COL	I	PD, LVTTL	**Port 5 Collision Input in MII Mode** Active high to indicate that there is collision on the medium. Stay low in full duplex operation.
	GPSI_P5COL	I	PD, LVTTL	**Port 5 Collision Input in GPSI Mode** Active high to indicate that there is collision on the medium. Stay low in full duplex operation.

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
72	MII_P5RXCLK	I	PD, LVTTL	**Port 5 Receive Clock Input in MII Mode** MII_P5RXDV and MII_P5RXD[3:0] are synchronous to the rising edge of this clock. It is free running 25 MHz clock in 100M mode and 2.5 MHz clock in 10M mode.
	GPSI_P5 RXCLK	I	PD, LVTTL	**Port 5 Receive Clock Input in GPSI Mode** GPSI_P5RXD are synchronous to the rising edge of this clock. It is non-continuous 10 MHz Clock input.
	REFCLK_IN	I	PD, LVTTL	**50MHz Reference Clock Input in RMII Mode** RMII_P5RXD[1:0], RMII_P5TXD[1:0], RMII_P5TXEN and RMII_P5CRSDV are synchronous to the rising edge of this clock.
67	MII_P5TXCLK	I	PD, LVTTL	**Port 5 Transmit Clock Input in MII Mode** MII_P5TXEN and MII_P5TXD[3:0] are output at the rising edge of this clock. It is free running 25 MHz clock in 100M mode and 2.5 MHz clock in 10M mode.
	GPSI_P5 TXCLK	I	PD, LVTTL	**Port 5 Transmit Clock Input in GPSI Mode** GPSI_P5TXEN and GPSI_P5TXD are synchronous to the rising edge of this clock. It is continuous 10 MHz Clock input.
	REFCLK _ OUT	O	8 mA, PD, LVTTL	**50MHz Reference Clock Output in RMII Mode** This pin is used as 50 MHz reference clock signal output pin when port 5 operates in RMII mode.
89	SPDTNP5	I	PD, LVTTL	**Port 5 Speed Input** This pin is used to select the speed mode of Port 5. 0_B 100M 1_B 10M
90	LNKFP5	I	PD, LVTTL	**Port 5 Link Fail Status Input** This pin is used as link control of Port 5. 0_B Link Up 1_B Link Failed
91	DPHALFP5	I	PD, LVTTL	**Port 5 Duplex Status Input** This pin is used to select the duplex mode of Port 5. 0_B Full Duplex 1_B Half Duplex
LED Interface				

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
107	DPHALFP4	I	PD, LVTTL	**Port 4 Duplex status Input** When Port 4 operates under MAC MII mode (see **CFG0** for more details), this pins is used to select the duplex mode of Port 4. 0_B Full Duplex 1_B Half Duplex
	DUPCOL4	O	8 mA, PD, LVTTL	**Port 4 Duplex /Collision LED** When Port 4 operates under PHY or PCS MII mode (see **CFG0** for more details), in Full duplex mode, this pin acts as DUPLEX LED for Port 4; in half duplex mode, it is collision LED for each port. See **Chapter 3.1.12 LED Display** for more details.
110	DUPCOL3	O	8 mA, PD, LVTTL	**Port 3 Duplex /Collision LED** In Full duplex mode, this pin acts as DUPLEX LED for Port 3; in half duplex mode, it is collision LED for each port. See **Chapter 3.1.12 LED Display** for more details.
111	BPEN	I	PU, LVTTL	**Recommend Back-Pressure in Half-Duplex** Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) during power on reset as the back-pressure enable in half-duplex mode. *Note: Power On Setting* 0_B Disable Back-Pressure 1_B Enable Back-Pressure
	DUPCOL2	O	8 mA, PU, LVTTL	**Port 2 Duplex-collision LED** In Full duplex mode, this pin acts as Port 2 DUPLEX LED; in half duplex mode, it is collision LED for Port 2. See **Chapter 3.1.12 LED Display** for more details.
112	PHYAS1	I	PD, LVTTL	**Recommend PHY Address Bit 1** Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) during power on reset as the PHY address recommends value bit 1. See **PHYAS0** description for more details. *Note: Power On Setting*
	DUPCOL1	O	8 mA, PD, LVTTL	**Port 1 Duplex-collision LED** In Full duplex mode, this pin acts as port 1 DUPLEX LED; in half duplex mode, it is collision LED for Port 1. See **Chapter 3.1.12 LED Display** for more details.

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
113	RECANEN	I	PU, LVTTL	**Recommend Auto Negotiation Enable** Only valid for Twisted pair interface. Programmed this bit to 1 has no effect to Fiber port. *Note: Power On Setting.* 0_B Disable all TP port auto negotiation capability 1_B Enable all TP port auto negotiation capability
	DUPCOL0	O	8 mA, PU, LVTTL	**Port 0 Duplex-collision LED** In Full duplex mode, this pin acts as port 0 DUPLEX LED; in half duplex mode, it is collision LED for Port 0. See **Chapter 3.1.12 LED Display** for more details.
92	LNKFP4	I	PD, LVTTL	**Port 4 Link Fail Status Input** When Port 4 operates under MAC MII mode (see **CFG0** for more details), this pin is used as link control of Port 4. 0_B Link Up 1_B Link Failed
	LNKACT_4	O	8 mA, PD, LVTTL	**LINK/Activity LED of Port 4** When Port 4 operates under PHY or PCS MII mode (see **CFG0** for more details), this pin is used to indicate the link/activity status of Port 4, see **Chapter 3.1.12 LED Display** for more details.
95	LNKACT_3	O	8 mA, PD, LVTTL	**LINK/Activity LED of Port 3 to 0** Used to indicate corresponding port' s link/activity status, see **Chapter 3.1.12 LED Display** for more details.
96	LNKACT_2			
97	LNKACT_1			
98	LNKACT_0			
51	SPDTNP4	I	PD, LVTTL	**Port 4 Speed Input** When Port 4 operates under MAC MII mode (see **CFG0** for more details), this pin is used to select the operating speed of Port 4. 0_B 100M 1_B 10M
	LDSPD_4	O	8 mA, PD, LVTTL	**Port 4 Speed LED** When Port 4 operates under PHY or PCS MII mode (see **CFG0** for more details), this pin is used to indicate the speed status of Port 4, see **Chapter 3.1.12 LED Display** for more details.
48	LDSPD_3	O	8 mA, PD, LVTTL	**Port 3 to Port 0 Speed LED** Used to indicate corresponding port' s speed status, see **Chapter 3.1.12 LED Display** for more details.
47	LDSPD_2			
43	LDSPD_1			
42	LDSPD_0			
EEPROM Interface				

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
84	EDO	I	PU, LVTTL	**EEPROM Data Output** This pin is used to input EEPROM data when reading EEPROM. During Samurai-6M/6MX (ADM6996M/MX) initialisation, Samurai-6M/6MX (ADM6996M/MX) will drive EEPROM interface signal to read settings from EEPROM. Any other devices attached to EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See **Chapter 3.4.2 EEPROM Interface** for more details.
80	IFSEL	I	PD, LVTTL	**Interface Selection** After Samurai-6M/6MX (ADM6996M/MX) initialization process is done, this pin is used to select using EEPROM interface or SDC/SDIO interface. EECS/IFSEL interface 0_B SDC/SDIO interface 1_B EEPROM interface
	EECS	O	4 mA, PD, LVTTL	**EEPROM Chip Select** During Samurai-6M/6MX (ADM6996M/MX) initialisation, this pin is used as EEPROM chip select signal. During Samurai-6M/6MX (ADM6996M/MX) initialize itself, Samurai-6M/6MX (ADM6996M/MX) will drive EEPROM interface signal to read settings from EEPROM. Any other devices attached to EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See **Chapter 3.4.2 EEPROM Interface** for more details.
81	XOVEN	I	PD, LVTTL	**Cross Over Enable** Value on this pin (active low) will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(**RC**) for Port 4~0 crossover auto detect (Only available in TP interface). *Note: Power On Setting.* 0_B Disable 1_B Enable
	EESK	I/O	4 mA, PD, LVTTL	**EEPROM Serial Clock** During Samurai-6M/6MX (ADM6996M/MX) initialisation, this pin is used to output clock to EEPROM. After Samurai-6M/6MX (ADM6996M/MX) initialization process is done, this pin is used as EEPROM interface clock input if **IFSEL** = 1.
	SDC	I	PD, LVTTL	**Serial Management interface Clock input** If **IFSEL** = 0, this pin is used as serial management interface clock input.