



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Contents

Features	1
General Description	1
1. Quick Start Sequence	3
2. Evaluation Board Schematic and PCB Layout.....	4
3. The GN2013A MSLA Feature	7
4. Configuration Examples	8
4.1 Configuration Example 1	8
4.2 Configuration Example 2	9
4.3 Configuration Example 3	10
4.4 Configuration Example 4	11
5. Revision History	12

Features

- fully assembled and tested
- recovered clock output
- on-board mode selection switch
- on-board PLL Lock and Loss of Signal LED indicators
- SMA connectors for all high-speed data and clock inputs and outputs

General Description

This document describes the application of the XBN2013A Rev1 Evaluation Board.

The XBN2013A Rev1 evaluation board is designed to simplify and speed-up the evaluation process of Gennum's GN2013A XFP Rx Signal Conditioner.

The block diagram of the XBN2013A Rev1 evaluation board is shown on [page 2](#).

An input signal is applied to the board either through the Limiting Amplifier Input (LAI) or through the Loop Back Serial Data Input (LBSDI) SMA connectors.

The on-board GN2013A chip performs conditioning of the received signal.

The retimed data signal is available on the Serial Data Output (SDO) SMA connectors.

Two sets of controls are provided on the evaluation board:

- Dip switch SW1 allows for quick selection of the GN2013A's mode of operation
- Jumpers JP2 and JP3 in combination with the potentiometers R12 and R13 provide quick and convenient method for the Manual Slice Level Adjustment (MSLA) setting.

Two LEDs indicate the status of the GN2013A device.

- The PLL Lock green LED (D1), when lit, indicates the PLL's lock condition.
- The LOS red LED (D2), when lit, indicates that the limiting amplifier input signal level is below application set threshold level.

A schematic diagram of the XBN2013A Rev1 evaluation board is shown in [Figure 2-1 on page 4](#).

The PCB layout information is shown in [Figure 2-2 on page 5](#), [Figure 2-3 on page 5](#), [Figure 2-4 on page 6](#) and [Figure 2-5 on page 6](#).

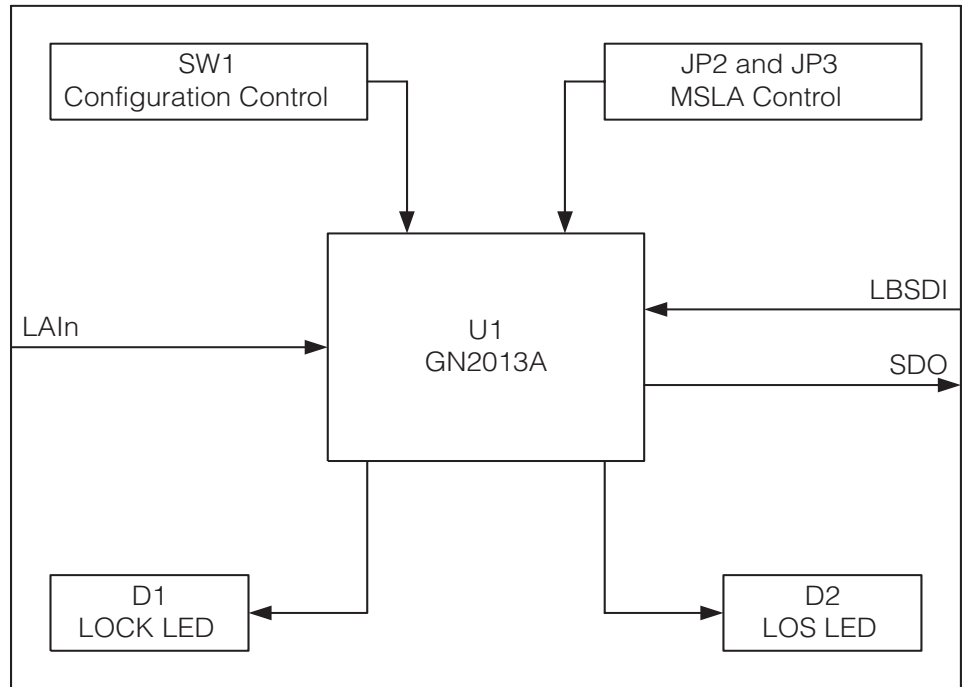
The XBN2013A Rev1 printed circuit board is a four-layer, .062" board.

Top layer uses RT Duriod 6002, low dielectric loss material.

All other layers are standard FR-4 material.

All high-speed data traces between SMA connectors and the GN2013A device are 100W differential microstrip lines on the top layer.

For more information regarding the GN2013A operational modes and alarm functions please refer to the GN2013A Data Sheet.



GN2013A Evaluation Board Block Diagram

1. Quick Start Sequence

1. Configure the evaluation board in accordance to the required mode (i.e., see [Figure 4-1 on page 8](#), [Figure 4-2 on page 9](#), [Figure 4-3 on page 10](#) and [Figure 4-4 on page 11](#)). Other configurations are possible.
2. Connect Power Supply "GND" output to the on-board "GND" connector.
3. Connect Power Supply "+3.3V" output to the on-board "VCC" connector (current limit on the Power Supply should be set to 120mA).
4. Using 50 Ω coaxial cables, apply input signal with amplitude between 10mVppd and 1200mVppd to the LAIN/LAIP SMA connectors.
5. To evaluate the Loop Back path, apply input signal with amplitude of 100mVppd to the LSBDI SMA connectors using 50 Ω coaxial cables.
6. Use the SDO SMA connectors to monitor the GN2013A data output on a high speed oscilloscope. The SDO output can also be connected to a BERT (Bit Error Rate Tester) for BER measurements.
7. Use information from the GN2013A's Preliminary Data Sheet and [Table 3-1](#) to adjust on-board controls in order to achieve desirable performance.

2. Evaluation Board Schematic and PCB Layout

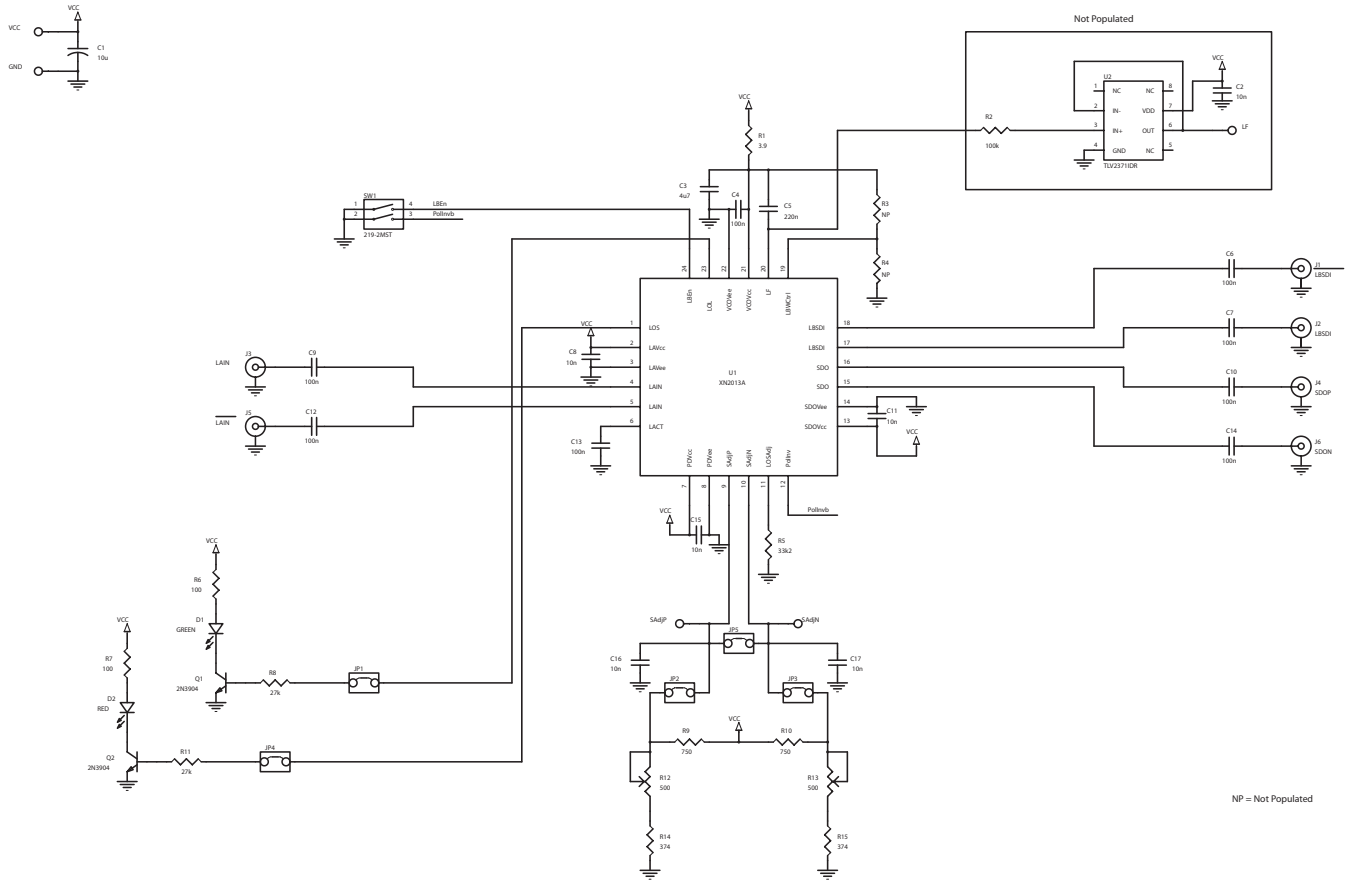


Figure 2-1: Evaluation Board Schematic

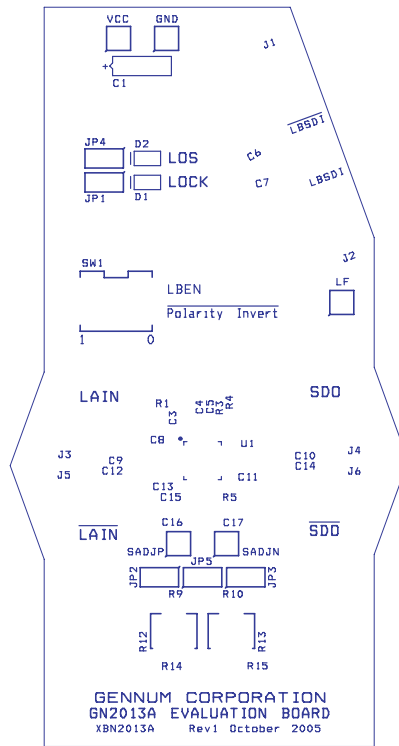


Figure 2-2: XBN2013A PCB Layout - Top Silk

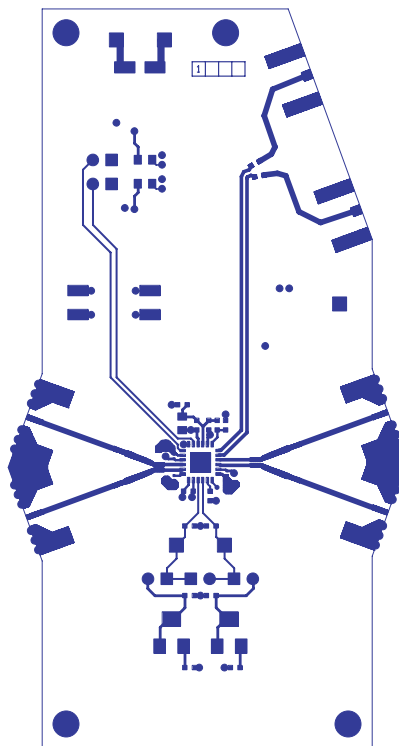


Figure 2-3: XBN2013A PCB Layout - Top Components

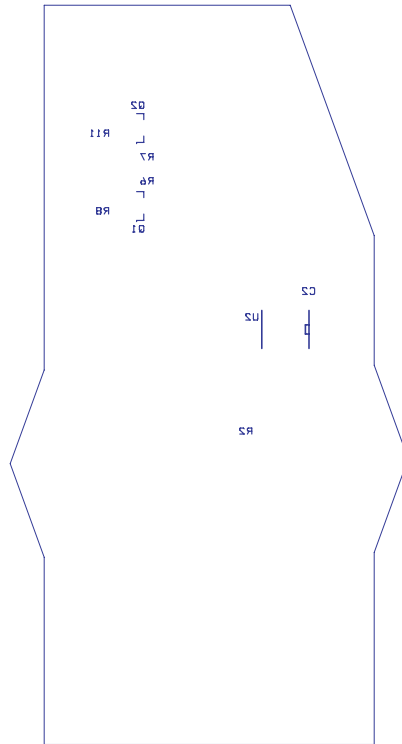


Figure 2-4: XBN2013A PCB Layout - Bottom Silk

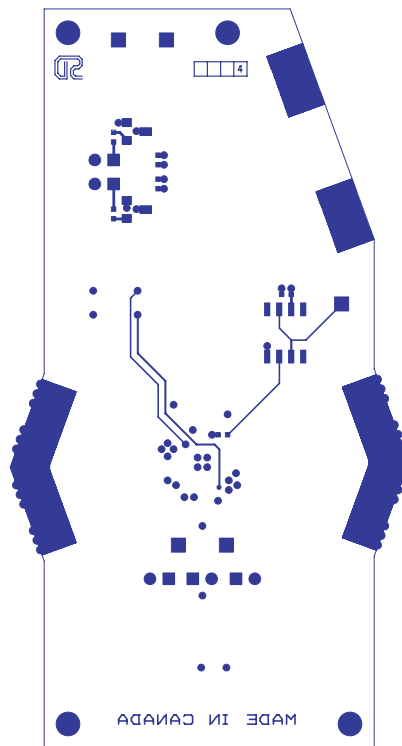


Figure 2-5: XBN2013A PCB Layout - Bottom Components

3. The GN2013A MSLA Feature

Manual Slice Level Adjust circuit, found in the GN2013A device, allows for manual optimization of the Input Slice Level. This feature is optional and can be enabled or disabled as required.

To activate the MSLA circuit the V_{SAdjP} and V_{SAdjN} voltages must be applied to the SAdjP and SAdjN control inputs. The V_{SAdjP} and V_{SAdjN} voltage values should be in the range from 1150mV to 1850mV and simultaneously satisfy two conditions:

1. $V_{com} = (V_{SAdjP} + V_{SAdjN})/2 = 1500mV \pm 50mV$
2. $V_{Adj} = V_{SAdjP} - V_{SAdjN} = 0mV \pm 600mV$

The amount and the polarity of the Input Referred Slice Level (V_{IRSL}) adjustment is controlled by the V_{Adj} voltage, applied to the SAdjP and SAdjN inputs.

When the SAdjP and SAdjN inputs are switched unconnected or tied to GND, the MSLA circuit becomes disabled. This automatically turns ON the Auto DC Offset Correction circuit which, in turn, brings the Input Slice Level to its optimum $\approx 0mV$ position.

The information provided in [Table 3-1](#) reflects results measured on a single device operating under typical conditions. This information should be considered as a guide for typical MSLA settings.

Table 3-1: Typical MSLA settings

V_{SAdjP}	V_{SAdjN}	V_{com}	V_{Adj}	V_{IRSL}
mVdc	mVdc	mVdc	mVdc	mVdc
Open	Open	–	–	≈ 0
GND	GND	–	–	≈ 0
1750	1250	1500	500	+ 26.9
1650	1350	1500	300	+ 15.8
1600	1400	1500	200	+ 10.5
1550	1450	1500	100	+ 5.2
1500	1500	1500	0	≈ 0
1450	1550	1500	-100	- 5.2
1400	1600	1500	-200	- 10.5
1350	1650	1500	-300	- 15.8
1250	1750	1500	-500	- 26.9

For more information regarding the GN2013A's MSLA feature please refer to the GN2013A Preliminary Data Sheet Doc ID 35380_2 and Application Note Doc ID 36988.

4. Configuration Examples

The GN2013A Signal Conditioner can be configured to operate with some features enabled or disabled.

This section demonstrates examples for several settings using controls on the evaluation board.

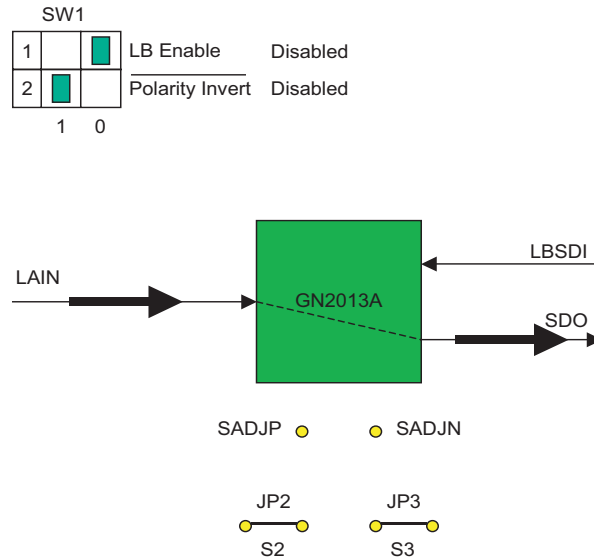
4.1 Configuration Example 1

Configuration, illustrated in Figure 4-1, corresponds to:

1. MSAL feature — Enabled
2. Loop Back Path — Disabled (LAIN input is accepted and LBSDI input is ignored)
3. Polarity Inversion — Disabled (normal polarity on the SDO output).

Data from the LAIN input is amplified and retimed. The retimed data is available on the SDO output.

Manual Slice Level Adjustment is performed using on board R12 and R13 potentiometers. The amount of the adjustment can be monitored by connecting a voltmeter to the SADJP/SADJN headers.



Place S2 and S3 shunts to Enable and the MSLA Circuit.
 Slice Level Adjustment is performed using R12 and R13 potentiometers

Figure 4-1: Configuration Example 1

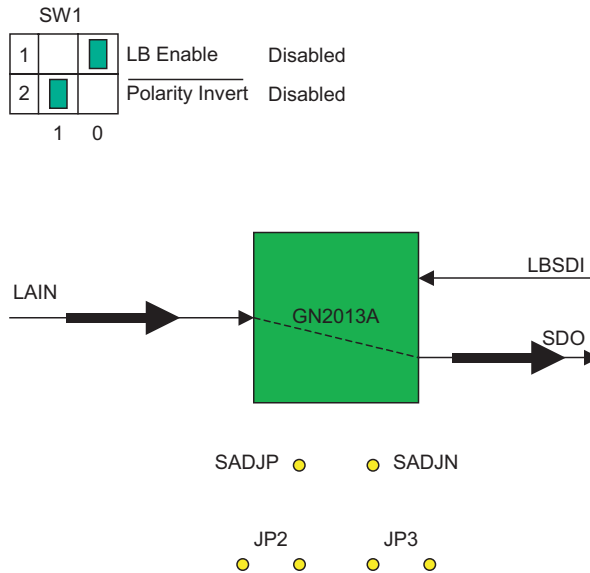
4.2 Configuration Example 2

Configuration, illustrated in Figure 4-2, corresponds to:

1. MSAL feature — Enabled
2. Loop Back Path — Disabled (LAIN input is accepted and LBSDI input is ignored)
3. Polarity Inversion — Disabled (normal polarity on the SDO output).

Data from the LAIN input is amplified and retimed. The retimed data is available on the SDO output.

Manual Slice Level Adjustment is performed by altering the External Voltage Sources' level. The amount of the adjustment can be monitored by connecting a voltmeter to the SADJP/SADJN headers.



Remove S2 and S3 shunts. Apply Control Voltage from External Source to SADJP and SADJN headers to Enable the MSLA Circuit and perform Slice Level Adjustment

Figure 4-2: Configuration Example 2

4.3 Configuration Example 3

Configuration, illustrated in Figure 4-3, corresponds to:

1. MSAL feature — Disabled
2. Loop Back Path — Disabled (LAIN input is accepted and LBSDI input is ignored)
3. Polarity Inversion — Disabled (normal polarity on the SDO output).

Data from the LAIN input is amplified and retimed. The retimed data is available on the SDO output.

Manual Slice Level Adjustment is not possible.

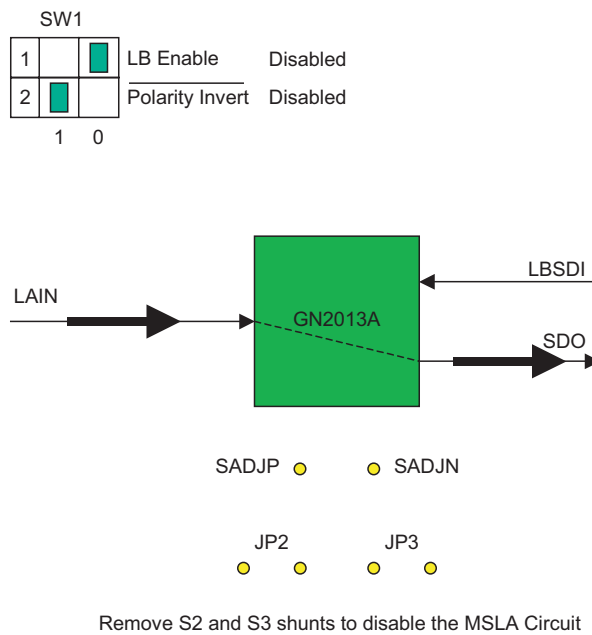


Figure 4-3: Configuration Example 3

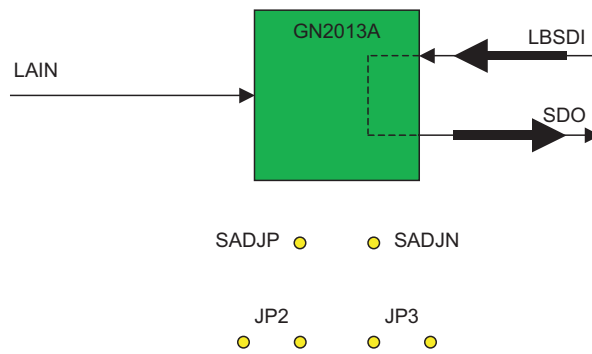
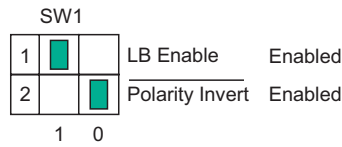
4.4 Configuration Example 4

Configuration, illustrated in Figure 4-4, corresponds to:

1. MSAL feature — Disabled
2. Loop Back Path — Enabled (LBSDI input is accepted and LAIN is ignored)
3. Polarity Inversion — Enabled (inverted polarity on the SDO output).

Data from the LBSDI input is amplified and retimed. The retimed data with inverted polarity is available on the SDO output.

Manual Slice Level Adjustment is not possible.



Remove S2 and S3 shunts to disable the MSLA Circuit

Figure 4-4: Configuration Example 4

5. Revision History

Version	ECR	Date	Changes and / or Modifications
0	138427	November 2005	New document.

CAUTION

ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION



DOCUMENT IDENTIFICATION

APPLICATION NOTE

Information relating to this product and the application or design described herein is believed to be reliable, however such information is provided as a guide only and Gennum assumes no liability for any errors in this document, or for the application or design described herein. Gennum reserves the right to make changes to the product or this document at any time without notice.

GENNUM CORPORATION

Mailing Address: P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Shipping Address: 970 Fraser Drive, Burlington, Ontario, Canada L7L 5P5
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946

GENNUM JAPAN CORPORATION

Shinjuku Green Tower Building 27F, 6-14-1, Nishi Shinjuku, Shinjuku-ku, Tokyo, 160-0023 Japan
Tel. +81 (03) 3349-5501, Fax. +81 (03) 3349-5505

GENNUM UK LIMITED

25 Long Garden Walk, Farnham, Surrey, England GU9 7HX
Tel. +44 (0)1252 747 000 Fax +44 (0)1252 726 523

Gennum Corporation assumes no liability for any errors or omissions in this document, or for the use of the circuits or devices described herein. The sale of the circuit or device described herein does not imply any patent license, and Gennum makes no representation that the circuit or device is free from patent infringement.

GENNUM and the G logo are registered trademarks of Gennum Corporation.

© Copyright 2005 Gennum Corporation. All rights reserved. Printed in Canada.

www.gennum.com