



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





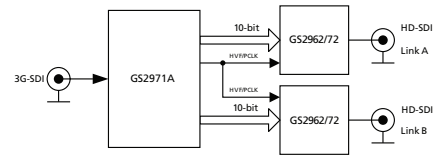
3Gb/s, HD, SD SDI Receiver, with Integrated Adaptive Cable Equalizer complete with SMPTE Audio and Video Processing

Key Features

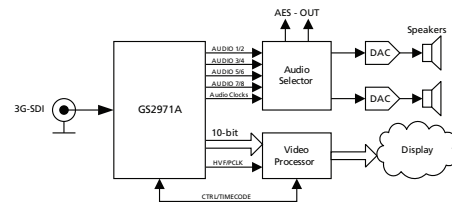
- Operation at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE ST 425 (Level A and Level B), SMPTE ST 424, SMPTE ST 292, SMPTE ST 259-C and DVB-ASI
- Integrated adaptive cable equalizer
- Typical equalized length of Belden 1694A cable:
 - ♦ 150m at 2.97Gb/s
 - ♦ 250m at 1.485Gb/s
 - ♦ 480m at 270Mb/s
- Integrated Reclocker with low phase noise, integrated VCO
- Serial digital reclocked, or non-reclocked output
- Integrated audio de-embedder for 8 channels of 48kHz audio
- Integrated audio clock generator
- Ancillary data extraction
- Optional conversion from SMPTE ST 425 Level B to Level A for 1080p 50/60 4:2:2 10-bit
- Parallel data bus selectable as either 20-bit or 10-bit
- Comprehensive error detection and correction features
- Output H, V, F or CEA 861 Timing Signals
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- GSPI Host Interface
- -20°C to +85°C operating temperature range
- Low power operation (typically 545mW)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and RoHS compliant

Applications

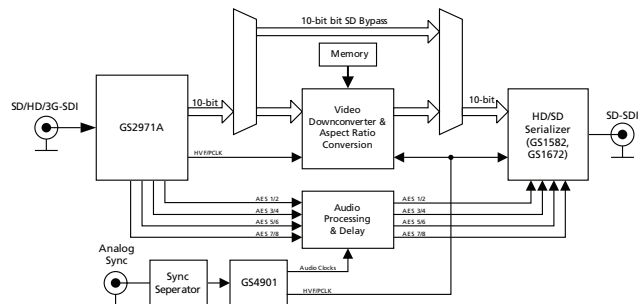
Application: Single Link (3G-SDI) to Dual Link (HD-SDI) Converter



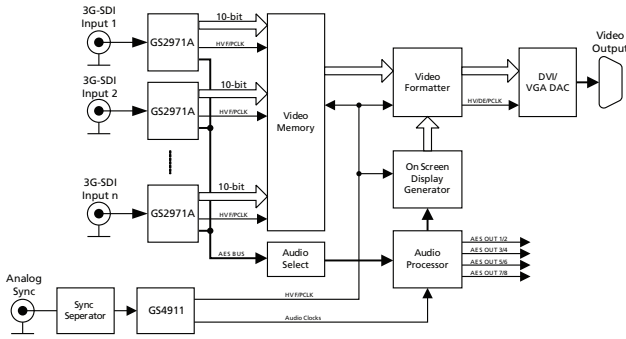
Application: 1080p50/60 Monitor



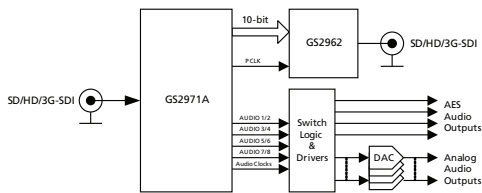
Application: Multi-format Downconverter



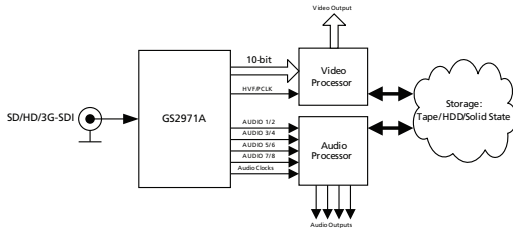
Application: Multi-input Video Monitoring System



Application: Multi-format Audio De-embedder Module



Application: Multi-format Digital VTR/Video Server



Description

The GS2971A is a multi-rate SDI integrated Receiver which includes complete SMPTE processing, as per SMPTE ST 425, SMPTE ST 292 and SMPTE ST 259-C. The SMPTE processing features can be bypassed to support signals with other coding schemes.

The GS2971A integrates Semtech's adaptive cable equalizer technology, achieving unprecedented cable lengths and jitter tolerance. It features DC restoration to compensate for the DC content of SMPTE pathological signals.

The device features an Integrated Reclocker with an internal VCO and a wide Input Jitter Tolerance (IJT) of 0.7UI.

A serial digital loop-through output is provided, which can be configured to output either reclocked or non-reclocked serial digital data. The serial digital output can be connected to an external cable driver.

The device operates in one of four basic modes: SMPTE mode, DVB-ASI mode, Data-Through mode or Standby mode.

In SMPTE mode (the default operating mode), the GS2971A performs full SMPTE processing, and features a number of data integrity checks and measurement capabilities.

The device also supports ancillary data extraction, and can provide entire ancillary data packets through host-accessible registers. It also provides a variety of other packet detection and error handling features. All of these processing features are optional, and may be individually enabled or disabled through register programming.

Both SMPTE ST 425 Level A and Level B inputs are supported with optional conversion from Level B to Level A for 1080p 50/59.94/60 4:2:2 10-bit inputs.

In DVB-ASI mode, sync word detection, alignment and 8b/10b decoding is applied to the received data stream.

In Data-Through mode all forms of SMPTE and DVB-ASI processing are disabled, and the device can be used as a simple serial to parallel converter.

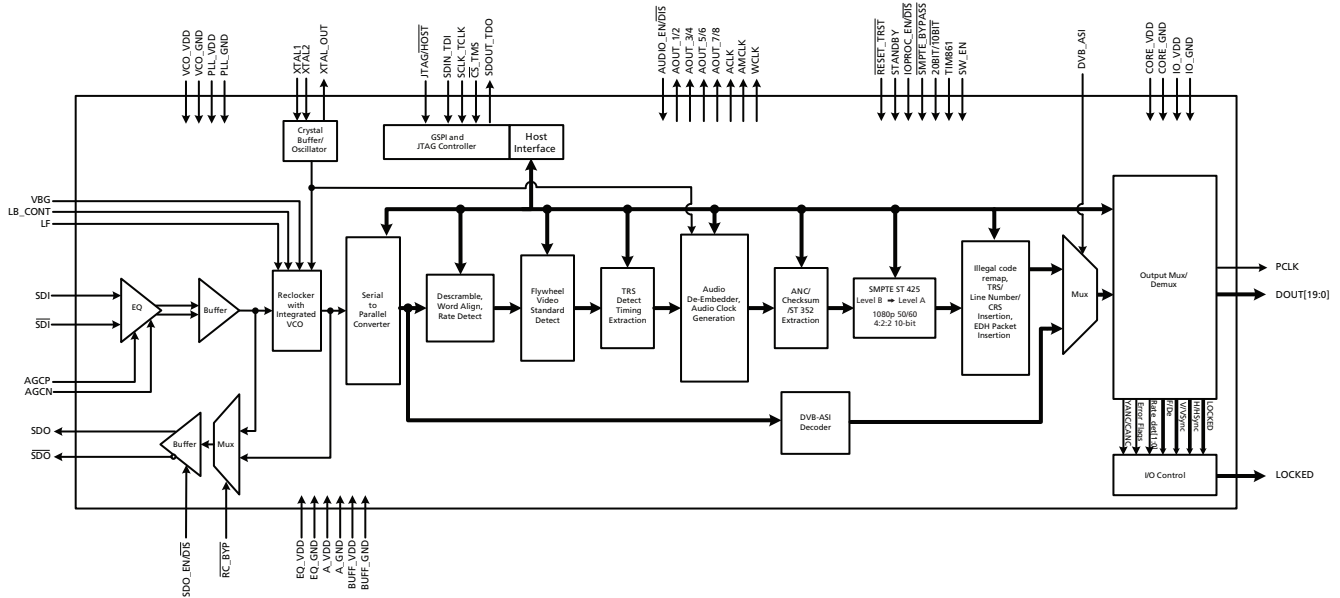
The device can also operate in a lower power Standby mode. In this mode, no signal processing is carried out and the parallel output is held static.

Parallel data outputs are provided in 20-bit or 10-bit format for 3Gb/s, HD and SD video rates, with a variety of mapping options. As such, this parallel bus can interface directly with video processor ICs, and output data can be multiplexed onto 10 bits for a low pin count interface.

Up to eight channels (two audio groups) of serial digital audio may be extracted from the video data stream, in accordance with SMPTE ST 272-C and SMPTE ST 299.

The output audio formats supported by the device include AES/EBU and I²S, and two other industry standard serial digital formats. A variety of audio processing features are provided to ease implementation. Audio clocks are internally generated and provided by the device.

Functional Block Diagram



GS2971A Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
3	014961	-	August 2013	Clarified IOPROC_EN/DS register configuration throughout Section 4. Added note to Section 4.20. Updated SMPTE format throughout document.
2	158578	-	September 2012	Added back the Typ column in the Table 2-4: AC Electrical Characteristics
1	158083	-	June 2012	Updates throughout the document
0	154391	-	July 2010	New Document

Contents

1. Pin Out.....	9
1.1 Pin Assignment	9
1.2 Pin Descriptions	9
2. Electrical Characteristics	16
2.1 Absolute Maximum Ratings	16
2.2 Recommended Operating Conditions	16
2.3 DC Electrical Characteristics	17
2.4 AC Electrical Characteristics	19
3. Input/Output Circuits	25
4. Detailed Description.....	28
4.1 Functional Overview	28
4.2 SMPTE ST 425 Mapping - 3G Level A and Level B Formats	29
4.2.1 Level A Mapping.....	29
4.2.2 Level B Mapping	29
4.3 Serial Digital Input	30
4.3.1 Integrated Adaptive Cable Equalizer.....	30
4.4 Serial Digital Loop-Through Output	31
4.5 Serial Digital Reclocker	32
4.5.1 PLL Loop Bandwidth	32
4.6 External Crystal / Reference Clock	33
4.7 Lock Detect	34
4.7.1 Asynchronous Lock	35
4.7.2 Signal Interruption	35
4.8 SMPTE Functionality	35
4.8.1 Descrambling and Word Alignment	35
4.9 Parallel Data Outputs	36
4.9.1 Parallel Data Bus Buffers.....	36
4.9.2 Parallel Output in SMPTE Mode	39
4.9.3 Parallel Output in DVB-ASI Mode	39
4.9.4 Parallel Output in Data-Through Mode	39
4.9.5 Parallel Output Clock (PCLK).....	39
4.9.6 DDR Parallel Clock Timing	40
4.10 Timing Signal Generator	42
4.10.1 Manual Switch Line Lock Handling	43
4.10.2 Automatic Switch Line Lock Handling	44
4.10.3 Switch Line Lock Handling During Level B to Level A Conversion	44
4.11 Programmable Multi-function Outputs	47
4.12 H:V:F Timing Signal Generation	47
4.12.1 CEA-861 Timing Generation	49
4.13 Automatic Video Standards Detection	56
4.13.1 2K Support.....	60
4.14 Data Format Detection & Indication	60
4.15 EDH Detection	61

4.15.1 EDH Packet Detection	61
4.15.2 EDH Flag Detection	62
4.16 Video Signal Error Detection & Indication	62
4.16.1 TRS Error Detection	64
4.16.2 Line Based CRC Error Detection	64
4.16.3 EDH CRC Error Detection.....	65
4.16.4 HD & 3G Line Number Error Detection	65
4.17 Ancillary Data Detection & Indication	65
4.17.1 Programmable Ancillary Data Detection.....	67
4.17.2 SMPTE ST 352 Payload Identifier.....	68
4.17.3 Ancillary Data Checksum Error	69
4.17.4 Video Standard Error	70
4.18 Signal Processing	71
4.18.1 TRS Correction & Insertion.....	72
4.18.2 Line Based CRC Correction & Insertion	72
4.18.3 Line Number Error Correction & Insertion	72
4.18.4 ANC Data Checksum Error Correction & Insertion	73
4.18.5 EDH CRC Correction & Insertion	73
4.18.6 Illegal Word Re-mapping	73
4.18.7 TRS and Ancillary Data Preamble Remapping.....	73
4.18.8 Ancillary Data Extraction.....	74
4.18.9 Level B to Level A Conversion	78
4.19 Audio De-embedder	79
4.19.1 Serial Audio Data I/O Signals.....	79
4.19.2 Serial Audio Data Format Support	81
4.19.3 Audio Processing.....	85
4.19.4 Error Reporting	92
4.20 GSPI - HOST Interface	93
4.20.1 Command Word Description.....	94
4.20.2 Data Read or Write Access.....	94
4.20.3 GSPI Timing.....	95
4.21 Host Interface Register Maps	97
4.21.1 Video Core Registers.....	97
4.21.2 SD Audio Core Registers.....	111
4.21.3 HD and 3G Audio Core Registers.....	126
4.22 JTAG Test Operation	141
4.23 Device Power-up	143
4.24 Device Reset	143
4.25 Standby Mode	143
5. Application Reference Design	144
5.1 High Gain Adaptive Cable Equalizers	144
5.2 PCB Layout	144
5.3 Typical Application Circuit	145
6. References & Relevant Standards	146

7. Package & Ordering Information	147
7.1 Package Dimensions	147
7.2 Packaging Data	148
7.3 Marking Diagram	148
7.4 Solder Reflow Profiles	149
7.5 Ordering Information	149

List of Figures

Figure 3-1: Digital Input Pin with Schmitt Trigger	25
Figure 3-2: Bidirectional Digital Input/Output Pin	25
Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength.....	26
Figure 3-4: XTAL1/XTAL2/XTAL-OUT	26
Figure 3-5: VBG	26
Figure 3-6: LB_CONT	27
Figure 3-7: Loop Filter	27
Figure 3-8: SDO/ $\overline{\text{SDO}}$	27
Figure 3-9: Equalizer Input Equivalent Circuit	27
Figure 4-1: Level A Mapping	29
Figure 4-2: Level B Mapping	29
Figure 4-3: GS2971A Integrated EQ Block Diagram	31
Figure 4-4: 27MHz Clock Sources	33
Figure 4-5: PCLK to Data and Control Signal Output Timing - SDR Mode 1	36
Figure 4-6: PCLK to Data and Control Signal Output Timing - SDR Mode 2	37
Figure 4-7: PCLK to Data and Control Signal Output Timing - DDR Mode	37
Figure 4-8: DDR Video Interface - 3G Level A	41
Figure 4-9: DDR Video Interface - 3G Level B	41
Figure 4-10: Delay Adjustment Ranges	42
Figure 4-11: Switch Line Locking on a Non-Standard Switch Line	43
Figure 4-12: H:V:F Output Timing - 3G Level A and HDTV 20-bit Mode	48
Figure 4-13: H:V:F Output Timing - 3G Level A and HDTV 10-bit Mode 3G Level B 20-bit Mode, each 10-bit stream	48
Figure 4-14: H:V:F Output Timing - 3G Level B 10-bit Mode	48
Figure 4-15: H:V:F Output Timing - HD 20-bit Output Mode	48
Figure 4-16: H:V:F Output Timing - HD 10-bit Output Mode	49
Figure 4-17: H:V:F Output Timing - SD 20-bit Output Mode	49
Figure 4-18: H:V:F Output Timing - SD 10-bit Output Mode	49
Figure 4-19: H:V:DE Output Timing 1280 x 720p @ 59.94/60 (Format 4)	51
Figure 4-20: H:V:DE Output Timing 1920 x 1080i @ 59.94/60 (Format 5)	51
Figure 4-21: H:V:DE Output Timing 720 (1440) x 480i @ 59.94/60 (Format 6&7)	52
Figure 4-22: H:V:DE Output Timing 1280 x 720p @ 50 (Format 19)	52
Figure 4-23: H:V:DE Output Timing 1920 x 1080i @ 50 (Format 20)	53
Figure 4-24: H:V:DE Output Timing 720 (1440) x 576 @ 50 (Format 21 & 22)	54
Figure 4-25: H:V:DE Output Timing 1920 x 1080p @ 59.94/60 (Format 16)	54
Figure 4-26: H:V:DE Output Timing 1920 x 1080p @ 50 (Format 31)	55
Figure 4-27: H:V:DE Output Timing 1920 x 1080p @ 23.94/24 (Format 32)	55
Figure 4-28: H:V:DE Output Timing 1920 x 1080p @ 25 (Format 33)	56
Figure 4-29: H:V:DE Output Timing 1920 x 1080p @ 29.97/30 (Format 34)	56
Figure 4-30: 2K Feature Enhancement	60
Figure 4-31: Y/1ANC and C/2ANC Signal Timing	67

Figure 4-32: Ancillary Data Extraction - Step A	75
Figure 4-33: Ancillary Data Extraction - Step B	76
Figure 4-34: Ancillary Data Extraction - Step C	76
Figure 4-35: Ancillary Data Extraction - Step D	77
Figure 4-36: ACLK to Data Signal Output Timing	80
Figure 4-37: I ² S Audio Output Format	81
Figure 4-38: AES/EBU Audio Output Format	81
Figure 4-39: Serial Audio, Left Justified, MSB First	82
Figure 4-40: Serial Audio, Left Justified, LSB First	82
Figure 4-41: Serial Audio, Right Justified, MSB First	82
Figure 4-42: Serial Audio, Right Justified, LSB First	82
Figure 4-43: AES/EBU Audio Output to Bit Clock Timing	82
Figure 4-44: ECC 24-bit Array and Examples	85
Figure 4-45: Sample Distribution over 5 Video Frames (525-line Systems)	87
Figure 4-46: Audio Buffer After Initial 26 Sample Write	87
Figure 4-47: Audio Buffer Pointer Boundary Checking	88
Figure 4-48: GSPI Application Interface Connection	93
Figure 4-49: Command Word Format	94
Figure 4-50: Data Word Format	95
Figure 4-51: Write Mode	95
Figure 4-52: Read Mode	95
Figure 4-53: GSPI Time Delay	95
Figure 4-54: In-Circuit JTAG	142
Figure 4-55: System JTAG	142
Figure 4-56: Reset Pulse	143
Figure 5-1: Typical Application Circuit	145
Figure 7-1: Package Dimensions	147
Figure 7-2: GS2971A Marking Diagram	148
Figure 7-3: Pb-free Solder Reflow Profile	149

List of Tables

Table 1-1: Pin Description	9
Table 2-1: Absolute Maximum Ratings.....	16
Table 2-2: Recommended Operating Conditions.....	16
Table 2-3: DC Electrical Characteristics	17
Table 2-4: AC Electrical Characteristics	19
Table 4-1: Serial Digital Output.....	31
Table 4-2: PLL Loop Bandwidth	32
Table 4-3: Input Clock Requirements.....	33
Table 4-4: Lock Detect Conditions.....	34
Table 4-5: GS2971A Output Video Data Format Selections	38
Table 4-6: GS2971A PCLK Output Rates	40
Table 4-7: Switch Line Position for Digital Systems	45
Table 4-8: Output Signals Available on Programmable Multi-Function Pins.....	47
Table 4-9: Supported CEA-861 Formats.....	49
Table 4-10: CEA861 Timing Formats	50
Table 4-11: Supported Video Standard Codes	57
Table 4-12: Data Format Register Codes	61
Table 4-13: Error Status Register and Error Mask Register	63
Table 4-14: SMPTE ST 352 Packet Data.....	69

Table 4-15: IOPROC_1 and IOPROC_2 Register Bits.....	71
Table 4-16: Serial Audio Pin Descriptions	79
Table 4-17: Audio Output Formats.....	81
Table 4-18: Audio Data Packet Detect Register	83
Table 4-19: Audio Group DID Host Interface Settings.....	84
Table 4-20: Audio Data and Control Packet DID Setting Register	84
Table 4-21: Audio Buffer Pointer Offset Settings	88
Table 4-22: Audio Channel Mapping Codes	89
Table 4-23: Audio Sample Word Lengths	90
Table 4-24: Audio Channel Status Information Registers	91
Table 4-25: Audio Channel Status Block for Regenerate Mode Default Settings	91
Table 4-26: Audio Mute Control Bits	92
Table 4-27: GSPI Time Delay	95
Table 4-28: GSPI Timing Parameters (50% levels; 3.3V or 1.8V operation)	96
Table 4-29: Video Core Configuration and Status Registers.....	97
Table 4-30: SD Audio Core Configuration and Status Registers.....	111
Table 4-31: HD and 3G Audio Core Configuration and Status Registers	126
Table 4-32: ANC Extraction FIFO Access Registers.....	141
Table 6-1: SMPTE Standards Reference.....	146
Table 7-1: Packaging Data.....	148

1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_CONT	VCO_VDD	STAT0	STAT1	IO_VDD	PCLK	DOUT18	DOUT17
B	A_VDD	PLL_VDD	RSV	VCO_GND	STAT2	STAT3	IO_GND	DOUT19	DOUT16	DOUT15
C	SDI	A_GND	PLL_VDD	PLL_VDD	STAT4	STAT5	$\overline{\text{RESET_TRST}}$	DOUT12	DOUT14	DOUT13
D	$\overline{\text{SDI}}$	A_GND	A_GND	PLL_GND	CORE_GND	CORE_VDD	SW_EN	JTAG/HOST	IO_GND	IO_VDD
E	EQ_VDD	EQ_GND	A_GND	PLL_GND	CORE_GND	CORE_VDD	SDOUT_TDO	SDIN_TDI	DOUT10	DOUT11
F	AGCP	RSV	A_GND	PLL_GND	CORE_GND	CORE_VDD	$\overline{\text{CS_TMS}}$	SCLK_TCK	DOUT8	DOUT9
G	AGCN	A_GND	$\overline{\text{RC_BYP}}$	CORE_GND	CORE_GND	CORE_VDD	$\overline{\text{SMPTE_BYPASS}}$	DVB_ASI	IO_GND	IO_VDD
H	BUFF_VDD	BUFF_GND	AUDIO_EN/ $\overline{\text{DIS}}$	WCLK	TIM_861	XTAL_OUT	20bit/ 10bit	IOPROC_EN/ $\overline{\text{DIS}}$	DOUT6	DOUT7
J	SDO	SDO_EN/ $\overline{\text{DIS}}$	AOUT_1/2	ACLK	AOUT_5/6	XTAL2	IO_GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{SDO}}$	STANDBY	AOUT_3/4	AMCLK	AOUT_7/8	XTAL1	IO_VDD	DOUT0	DOUT2	DOUT3

1.2 Pin Descriptions

Table 1-1: Pin Description

Pin Number	Name	Type	Description
A1	VBG	Analog Input	Band Gap voltage filter connection.
A2	LF	Analog Input	Loop Filter component connection.
A3	LB_CONT	Analog Input	Connection for loop bandwidth control resistor.
A4	VCO_VDD	Input Power	POWER pin for the VCO. Connect to a 1.2V±5% analog supply followed by a RC filter (see 5.3 Typical Application Circuit). A 105Ω 1% resistor must be used in the RC filter circuit. VCO_VDD is nominally 0.7V.

Table 1-1: Pin Description (Continued)

Pin Number	Name	Type	Description	
A5, A6, B5, B6, C5, C6	STAT[0:5]	Output	MULTI-FUNCTIONAL OUTPUT PORT. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Each of the STAT [0:5] pins can be configured individually to output one of the following signals:	
			Signal	Default
			H/HSYNC	STAT0
			V/VSYNC	STAT1
			F/DE	STAT2
			LOCKED	STAT3
			Y/1ANC	STAT4
			C/2ANC	–
			<u>DATA ERROR</u>	STAT5
			<u>VIDEO ERROR</u>	–
			<u>AUDIO ERROR</u>	–
			EDH DETECTED	–
			CARRIER DETECT	–
RATE_DET0	–			
RATE_DET1	–			
A7, D10, G10, K7	IO_VDD	Input Power	POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.	
A8	PCLK	Output	PARALLEL DATA BUS CLOCK Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.	
			3G 10-bit or 20-bit mode	PCLK @ 148.5 or 148.5/1.001MHz
			HD 10-bit mode	PCLK @ 148.5 or 148.5/1.001MHz
			HD 20-bit mode	PCLK @ 74.25 or 74.25/1.001MHz
			SD 10-bit mode	PCLK @ 27MHz
			SD 20-bit mode	PCLK @ 13.5MHz

Table 1-1: Pin Description (Continued)

Pin Number	Name	Type	Description
			<p>PARALLEL DATA BUS</p> <p>Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p>
A9, A10, B8, B9, B10, C8, C9, C10, E9, E10	DOUT18, 17, 19, 16, 15, 12, 14, 13, 10, 11	Output	<p>20-bit mode 20bit/10bit = HIGH</p> <p>SMPTE mode ($\overline{\text{SMPTE_BYPASS}} = \text{HIGH}$ and $\text{DVB_ASI} = \text{LOW}$): Luma data output for SD and HD data rates; Data Stream 1 for 3G data rate</p> <p>DVB-ASI mode ($\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ and $\text{DVB_ASI} = \text{HIGH}$): Not defined</p> <p>Data-Through mode ($\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ and $\text{DVB_ASI} = \text{LOW}$): Data output</p>
			<p>10-bit mode 20bit/10bit = LOW</p> <p>SMPTE mode ($\overline{\text{SMPTE_BYPASS}} = \text{HIGH}$ and $\text{DVB_ASI} = \text{LOW}$): Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1&2 for 3G data rate</p> <p>DVB-ASI mode ($\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ and $\text{DVB_ASI} = \text{HIGH}$): 8b/10b decoded DVB-ASI data</p> <p>Data-Through mode ($\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ and $\text{DVB_ASI} = \text{LOW}$): Data output</p>
B1	A_VDD	Input Power	POWER pin for analog circuitry. Connect to 3.3V DC analog.
B2, C3, C4	PLL_VDD	Input Power	POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.
B3, F2	RSV		These pins must be left unconnected.
B4	VCO_GND	Input Power	GND pin for the VCO. Connect to analog GND.
B7, D9, G9, J7	IO_GND	Input Power	GND connection for digital I/O. Connect to digital GND.
C1, D1	SDI, $\overline{\text{SDI}}$	Analog Input	Serial Digital Differential Input.
C2, D2, D3, E3, F3, G2	A_GND	Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.
			<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to reset the internal operating conditions to default settings and to reset the JTAG sequence.</p> <p>Normal mode ($\text{JTAG}/\overline{\text{HOST}} = \text{LOW}$):</p> <p>When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance.</p> <p>When HIGH, normal operation of the device resumes.</p> <p>JTAG test mode ($\text{JTAG}/\overline{\text{HOST}} = \text{HIGH}$):</p> <p>When LOW, all functional blocks are set to default and the JTAG test sequence is reset.</p> <p>When HIGH, normal operation of the JTAG test sequence resumes after $\overline{\text{RESET_TRST}}$ is de-asserted.</p>
C7	$\overline{\text{RESET_TRST}}$	Input	

Table 1-1: Pin Description (Continued)

Pin Number	Name	Type	Description
D4, E4, F4	PLL_GND	Input Power	GND pins for the Reclocker PLL. Connect to analog GND.
D5, E5, F5, G4, G5	CORE_GND	Input Power	GND connection for device core. Connect to digital GND.
D6, E6, F6, G6	CORE_VDD	Input Power	POWER connection for device core. Connect to 1.2V DC digital.
D7	SW_EN	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable switch-line locking, as described in Section 4.10.1 .
D8	JTAG/ $\overline{\text{HOST}}$	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to select JTAG test mode or host interface mode. When JTAG/ $\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test. When JTAG/ $\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes.
E1	EQ_VDD	Input Power	POWER pin for SDI buffer. Connect to 3.3V DC analog.
E2	EQ_GND	Input Power	GND pin for SDI buffer. Connect to analog GND.
E7	SDOUT_TDO	Output	COMMUNICATION SIGNAL OUTPUT Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. GSPI serial data output/test data out. In JTAG mode (JTAG/ $\overline{\text{HOST}}$ = HIGH), this pin is used to shift test results from the device. In host interface mode, this pin is used to read status and configuration data from the device.
E8	SDIN_TDI	Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. GSPI serial data in/test data in. In JTAG mode (JTAG/ $\overline{\text{HOST}}$ = HIGH), this pin is used to shift test data into the device. In host interface mode, this pin is used to write address and configuration data words into the device.
F1, G1	AGCP, AGCN		Automatic Gain Control for the equalizer. Attach the AGC capacitor between these pins.
F7	$\overline{\text{CS}}$ _TMS	Input	COMMUNICATION SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Chip select / test mode start. In JTAG mode (JTAG/ $\overline{\text{HOST}}$ = HIGH), this pin is Test Mode Start, used to control the operation of the JTAG test. In host interface mode (JTAG/ $\overline{\text{HOST}}$ = LOW), this pin operates as the host interface chip select and is active LOW.

Table 1-1: Pin Description (Continued)

Pin Number	Name	Type	Description
F8	SCLK_TCK	Input	<p>COMMUNICATION SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Serial data clock signal.</p> <p>In JTAG mode ($\overline{\text{JTAG/HOST}} = \text{HIGH}$), this pin is the JTAG clock.</p> <p>In host interface mode ($\overline{\text{JTAG/HOST}} = \text{LOW}$), this pin is the host interface serial bit clock.</p> <p>All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.</p>
F9, F10, H9, H10, J8, J9, J10, K8, K9, K10	DOUT8, 9, 6, 7, 1, 4, 5, 0, 2, 3	Output	<p>PARALLEL DATA BUS</p> <p>Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <hr/> <p>SMPTE mode ($\overline{\text{SMPTE_BYPASS}} = \text{HIGH}$ and $\text{DVB_ASI} = \text{LOW}$): Chroma data output for SD and HD data rates; Data Stream 2 for 3G data rate</p> <p>DVB-ASI mode ($\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ and $\text{DVB_ASI} = \text{HIGH}$): Not defined</p> <p>Data-Through mode ($\overline{\text{SMPTE_BYPASS}} = \text{LOW}$ and $\text{DVB_ASI} = \text{LOW}$): Data output</p> <hr/> <p>10-bit mode $20\text{bit}/10\text{bit} = \text{LOW}$</p> <p>Forced LOW</p>
G3	$\overline{\text{RC_BYP}}$	Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.</p>
G7	$\overline{\text{SMPTE_BYPASS}}$	Input/Output	<p>CONTROL SIGNAL INPUT/OUTPUT</p> <p>Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Indicates the presence of valid SMPTE data.</p> <p>When the $\overline{\text{AUTO/MAN}}$ bit in the host interface register is HIGH (Default), this pin is an OUTPUT. $\overline{\text{SMPTE_BYPASS}}$ is HIGH when the device locks to a SMPTE compliant input. $\overline{\text{SMPTE_BYPASS}}$ is LOW under all other conditions.</p> <p>When the $\overline{\text{AUTO/MAN}}$ bit in the host interface register is LOW, this pin is an INPUT:</p> <p>No SMPTE scrambling takes place, and none of the I/O processing features of the device are available when $\overline{\text{SMPTE_BYPASS}}$ is set LOW.</p> <p>When $\overline{\text{SMPTE_BYPASS}}$ is set HIGH, the device carries out SMPTE scrambling and I/O processing.</p> <p>When $\overline{\text{SMPTE_BYPASS}}$ and DVB_ASI are both set LOW, the device operates in Data-Through mode.</p>

Table 1-1: Pin Description (Continued)

Pin Number	Name	Type	Description
G8	DVB_ASI	Input/Output	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input/Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to enable/disable DVB-ASI data extraction in manual mode.</p> <p>When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is LOW, this pin is an input and when the DVB_ASI pin is set HIGH the device will carry out DVB_ASI data extraction and processing. The $\overline{\text{SMPTE_BYPASS}}$ pin must be set LOW. When SMPTE_BYPASS and DVB_ASI are both set LOW, the device operates in Data-Through mode.</p> <p>When the AUTO/$\overline{\text{MAN}}$ bit in the host interface is HIGH (default), DVB-ASI is configured as a status output (set LOW), and DVB-ASI input streams are not supported or recognized.</p>
H1	BUFF_VDD	Input Power	POWER pin for the serial digital output 50 Ω buffer. Connect to 3.3V DC analog.
H2	BUFF_GND	Input Power	GND pin for the cable driver buffer. Connect to analog GND.
H3	AUDIO_EN/ $\overline{\text{DIS}}$	Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Enables or disables audio extraction.</p>
H4	WCLK	Output	<p>48kHz word clock for Audio.</p> <p>Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p>
H5	TIM_861	Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to select CEA-861 timing mode.</p> <p>When TIM_861 is HIGH, the device outputs CEA 861 timing signals (HSYNC/VSYNC/DE) instead of H:V:F digital timing signals.</p>
H6	XTAL_OUT	Digital Output	Buffered 27MHz crystal output. Can be used to cascade the crystal signal.
H7	20bit/ $\overline{10\text{bit}}$	Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to select the output bus width.</p> <p>HIGH = 20-bit, LOW = 10-bit.</p>
H8	IOPROC_EN/ $\overline{\text{DIS}}$	Input	<p>CONTROL SIGNAL INPUT</p> <p>Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.</p> <p>Used to enable or disable audio and video processing features.</p> <p>When IOPROC_EN is HIGH, the audio and video processing features of the device are enabled. When IOPROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.</p>

Table 1-1: Pin Description (Continued)

Pin Number	Name	Type	Description
J1, K1	SDO, $\overline{\text{SDO}}$	Output	Serial Data Output Signal. 50Ω CML buffer for interfacing to an external cable driver. Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.
J2	SDO_EN/ $\overline{\text{DIS}}$	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. Used to enable/disable the serial digital output stage. When SDO_EN/ $\overline{\text{DIS}}$ is LOW, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH. When SDO_EN/ $\overline{\text{DIS}}$ is HIGH, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are enabled.
J3	AOUT_1/2	Output	Serial Audio Output; Channels 1 and 2. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
J4	ACLK	Output	64fs sample clock for audio. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
J5	AOUT_5/6	Output	Serial Audio Output; Channels 5 and 6. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
J6, K6	XTAL2, XTAL1	Analog Input	Input connection for 27MHz crystal.
K2	STANDBY	Input	CONTROL SIGNAL INPUT Please refer to the Input Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility. When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down. In this mode, the serial digital output signals, SDO and $\overline{\text{SDO}}$, are both pulled HIGH.
K3	AOUT_3/4	Output	Serial Audio Output; Channels 3 and 4. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
K4	AMCLK	Output	Oversampled master clock for audio (128fs, 256fs, 512fs selectable). Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.
K5	AOUT_7/8	Output	Serial Audio Output; Channels 7 and 8. Please refer to the Output Logic parameters in the DC Electrical Characteristics table for logic level threshold and compatibility.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +4.0V
Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (EQ_VDD, BUFF_VDD, A_VDD)	-0.3V to +4.0V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Operating Temperature Range	-20°C to +85°C
Functional Temperature Range	-40°C to +85°C
Storage Temperature Range	-50°C to +125°C
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

Note:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

T_A = -20°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Analog	A_VDD	–	3.13	3.3	3.47	V	1
Supply Voltage, Serial Digital Input	EQ_VDD	–	3.13	3.3	3.47	V	1
Supply Voltage, CD Buffer	BUFF_VDD	–	3.13	3.3	3.47	V	1

Note:

1. The 3.3V supplies must track the 3.3V supply of an external CD.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10bit 3G	–	220	265	mA	–
		20bit 3G	–	210	265	mA	–
		10/20bit HD	–	170	220	mA	–
		10/20bit SD	–	140	185	mA	–
		DVB_ASI	–	130	170	mA	–
+1.8V Supply Current	I_{1V8}	10bit 3G	–	37	45	mA	–
		20bit 3G	–	16	20	mA	–
		10/20bit HD	–	15	21	mA	–
		10/20bit SD	–	4	7	mA	–
		DVB_ASI	–	4	6	mA	–
+3.3V Supply Current	I_{3V3}	10bit 3G	–	150	180	mA	–
		20bit 3G	–	115	130	mA	–
		10/20bit HD	–	110	135	mA	–
		10/20bit SD	–	90	100	mA	–
		DVB_ASI	–	90	95	mA	–
Total Device Power (IO_VDD = 1.8V)	P_{1D8}	10bit 3G	–	560	680	mW	–
		20bit 3G	–	525	640	mW	–
		10/20bit HD	–	480	590	mW	–
		10/20bit SD	–	420	520	mW	–
		DVB_ASI	–	410	500	mW	–
		Reset	–	390	–	mW	–
		Standby	–	23	45	mW	–
Total Device Power (IO_VDD = 3.3V)	P_{3D3}	10bit 3G	–	750	930	mW	–
		20bit 3G	–	620	760	mW	–
		10/20bit HD	–	570	730	mW	–
		10/20bit SD	–	460	560	mW	–
		DVB_ASI	–	440	540	mW	–
		Reset	–	410	–	mW	–
		Standby	–	23	45	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_VSS -0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD +0.3	V	–

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Output Logic LOW	V_{OL}	IOL = 5mA, 1.8V operation	–	–	0.2	V	–
		IOL = 8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	IOH = 5mA, 1.8V operation	1.4	–	–	V	–
		IOH = 8mA, 3.3V operation	2.4	–	–	V	–
Serial Input							
Serial Input Common Mode Voltage	–	75Ω load	–	2.2	–	V	–
Serial Output							
Serial Output Common Mode Voltage	–	50Ω load	BUFF_VDD -(0.6/2)	BUFF_VDD -(0.45/2)	BUFF_VDD -(0.35/2)	V	–

Note:

The output drive strength of the digital outputs can be programmed through the host interface. please see [Table 4-29: Video Core Configuration and Status Registers](#), register 06Dh for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Device Latency: AUDIO_EN = 1, SMPTE mode, IOPROC_EN = 1	-	3G (Level A)	80	-	83	PCLK	-
		3G (Level B)	143	-	151	PCLK	-
		HD	80	-	83	PCLK	-
		SD	50	-	55	PCLK	-
Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 1	-	3G (Level A)	44	-	48	PCLK	-
		3G (Level B)	108	-	116	PCLK	-
		HD	44	-	48	PCLK	-
		SD	44	-	48	PCLK	-
Device Latency: AUDIO_EN = 0, SMPTE mode, IOPROC_EN = 0	-	3G (Level A)	33	-	36	PCLK	-
		HD	33	-	36	PCLK	-
		SD	32	-	35	PCLK	-
Device Latency: AUDIO_EN = 0, SMPTE bypass, IOPROC_EN = 0	-	3G (Level A)	6	-	9	PCLK	-
		HD	6	-	9	PCLK	-
		SD	5	-	9	PCLK	-
Device Latency: DVB-ASI	-	SD	12	-	16	PCLK	-
Reset Pulse Width	t_{reset}	-	1	-	-	ms	-
Parallel Output							
Parallel Clock Frequency	f_{PCLK}	-	13.5	-	148.5	MHz	-
Parallel Clock Duty Cycle	DC_{PCLK}	-	40	-	60	%	-

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	
Output Data Hold Time (1.8V)	t_{oh}	SPI	1.5	–	–	ns	1	
		3G 10-bit 6pF C_{LOAD}	AUDIO	1.5	–	–	ns	1
			DBUS	0.3	–	–	ns	1
			STAT	0.3	–	–	ns	1
			DBUS	1.0	–	–	ns	1
		3G 20-bit 6pF C_{LOAD}	STAT	1.0	–	–	ns	1
			DBUS	1.0	–	–	ns	1
		HD 10-bit 6pF C_{LOAD}	STAT	1.0	–	–	ns	1
			DBUS	1.0	–	–	ns	1
		HD 20-bit 6pF C_{LOAD}	STAT	1.0	–	–	ns	1
			DBUS	1.0	–	–	ns	1
		SD 10-bit 6pF C_{LOAD}	STAT	19.4	–	–	ns	1
			DBUS	19.4	–	–	ns	1
		SD 20-bit 6pF C_{LOAD}	STAT	38.0	–	–	ns	1
			DBUS	38.0	–	–	ns	1
		Output Data Hold Time (3.3V)	t_{oh}	SPI	1.5	–	–	ns
3G 10-bit 6pF C_{LOAD}	AUDIO			1.5	–	–	ns	2
	DBUS			0.3	–	–	ns	2
	STAT			0.3	–	–	ns	2
	DBUS			1.0	–	–	ns	2
3G 20-bit 6pF C_{LOAD}	STAT			1.0	–	–	ns	2
	DBUS			1.0	–	–	ns	2
HD 10-bit 6pF C_{LOAD}	STAT			1.0	–	–	ns	2
	DBUS			1.0	–	–	ns	2
HD 20-bit 6pF C_{LOAD}	STAT			1.0	–	–	ns	2
	DBUS			1.0	–	–	ns	2
SD 10-bit 6pF C_{LOAD}	STAT			19.4	–	–	ns	2
	DBUS			19.4	–	–	ns	2
SD 20-bit 6pF C_{LOAD}	STAT			38.0	–	–	ns	2
	DBUS			38.0	–	–	ns	2

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes	
Output Data Delay Time (1.8V)	t_{od}	SPI	–	–	14.0	ns	3	
		3G 10-bit 15pF C_{LOAD}	AUDIO	–	–	7.0	ns	3
			DBUS	–	–	1.8	ns	3
			STAT	–	–	2.5	ns	3
			DBUS	–	–	3.7	ns	3
		3G 20-bit 15pF C_{LOAD}	STAT	–	–	4.4	ns	3
			DBUS	–	–	3.7	ns	3
		HD 10-bit 15pF C_{LOAD}	STAT	–	–	4.4	ns	3
			DBUS	–	–	3.7	ns	3
		HD 20-bit 15pF C_{LOAD}	STAT	–	–	4.4	ns	3
			DBUS	–	–	3.7	ns	3
		SD 10-bit 15pF C_{LOAD}	STAT	–	–	22.2	ns	3
			DBUS	–	–	22.2	ns	3
		SD 20-bit 15pF C_{LOAD}	STAT	–	–	41.0	ns	3
			DBUS	–	–	41.0	ns	3
		Output Data Delay Time (3.3V)	t_{od}	SPI	–	–	14.0	ns
3G 10-bit 15pF C_{LOAD}	AUDIO			–	–	7.0	ns	4
	DBUS			–	–	1.9	ns	4
	STAT			–	–	2.2	ns	4
	DBUS			–	–	3.7	ns	4
3G 20-bit 15pF C_{LOAD}	STAT			–	–	4.1	ns	4
	DBUS			–	–	3.7	ns	4
HD 10-bit 15pF C_{LOAD}	STAT			–	–	4.1	ns	4
	DBUS			–	–	3.7	ns	4
HD 20-bit 15pF C_{LOAD}	STAT			–	–	4.1	ns	4
	DBUS			–	–	3.7	ns	4
SD 10-bit 15pF C_{LOAD}	STAT			–	–	22.2	ns	4
	DBUS			–	–	22.2	ns	4
SD 20-bit 15pF C_{LOAD}	STAT			–	–	41.0	ns	4
	DBUS			–	–	41.0	ns	4

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes		
Output Data Rise/Fall Time (1.8V)	t_r/t_f	3G 10-bit 6pF C_{LOAD}	STAT	–	–	0.4	ns	1	
			DBUS	–	–	0.3	ns	1	
			AUDIO	–	–	0.6	ns	1	
		All other modes 6pF C_{LOAD}	STAT	–	–	0.4	ns	1	
			DBUS	–	–	0.4	ns	1	
			AUDIO	–	–	0.6	ns	1	
		3G 10-bit 15pF C_{LOAD}	STAT	–	–	1.5	ns	3	
			DBUS	–	–	1.1	ns	3	
			AUDIO	–	–	2.3	ns	3	
			All other modes 15pF C_{LOAD}	STAT	–	–	1.5	ns	3
				DBUS	–	–	1.4	ns	3
				AUDIO	–	–	2.3	ns	3
Output Data Rise/Fall Time (3.3V)	t_r/t_f	3G 10-bit 6pF C_{LOAD}	STAT	–	–	0.5	ns	2	
			DBUS	–	–	0.4	ns	2	
			AUDIO	–	–	0.6	ns	2	
		All other modes 6pF C_{LOAD}	STAT	–	–	0.5	ns	2	
			DBUS	–	–	0.4	ns	2	
			AUDIO	–	–	0.6	ns	2	
Output Data Rise/Fall Time (3.3V)	t_r/t_f	3G 10-bit 15pF C_{LOAD}	STAT	–	–	1.6	ns	4	
			DBUS	–	–	1.5	ns	4	
			AUDIO	–	–	2.2	ns	4	
		All other modes 15pF C_{LOAD}	STAT	–	–	1.6	ns	4	
			DBUS	–	–	1.4	ns	4	
			AUDIO	–	–	2.2	ns	4	
Serial Digital Input									
Serial Input Data Rate	DR_{SDI}	–	0.27	–	2.97	Gb/s	–		
Serial Input Voltage Swing	ΔV_{SDI}	$T_A = 25^\circ\text{C}$, differential, 270Mb/s & 1.485Gb/s	720	800	950	mV _{p-p}	6		
		$T_A = 25^\circ\text{C}$, differential, 2.97Gb/s	720	800	880	mV _{p-p}	6		
Achievable Cable Length	–	Belden 1694A cable, 3G	–	150	–	m	–		
		Belden 1694A cable, HD	–	230	–	m	–		
		Belden 1694A cable, SD	–	460	–	m	–		

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Input Return Loss	–	single ended	15	21	–	dB	7
Input Resistance	–	single ended	–	1.52	–	k Ω	–
Input Capacitance	–	single ended	–	1	–	pF	–
Serial Digital Output							
Serial Output Data Rate	DR _{SDO}	–	0.27	–	2.97	Gb/s	–
Serial Output Swing	ΔV_{SDO}	Differential with 100 Ω load	320	–	600	mV _{p-p}	–
Serial Output Rise Time 20% ~ 80%	tr _{SDO}	–	–	–	180	ps	–
Serial Output Fall Time 20% ~ 80%	tf _{SDO}	–	–	–	180	ps	–
Serial Output Jitter with loop-through mode	t _{OJ}	3G, PRBS23, Belden 1694A cable, 140m	–	–	100	ps	–
		HD, PRBS23, Belden 1694A cable, 210m	–	–	100	ps	–
		SD, PRBS23, Belden 1694A cable, 440m	–	–	470	ps	–
Serial Output Duty Cycle Distortion	DCD _{SDD}	3G	–	10	–	ps	–
		HD	–	10	–	ps	–
		SD	–	20	–	ps	–
Synchronous lock time	–	–	–	–	25	μ s	–
Asynchronous lock time	–	–	0.1	–	20	ms	–
Lock time from power-up	–	After 20 minutes at -20°C	–	–	5	s	–
GSPI							
GSPI Input Clock Frequency	f _{SCLK}		–	–	60	MHz	5
GSPI Input Clock Duty Cycle	DC _{SCLK}		40	50	60	%	5
GSPI Input Data Setup Time	–		1.5	–	–	ns	5
GSPI Input Data Hold Time	–		1.5	–	–	ns	5
GSPI Output Data Hold Time	–	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	5
\overline{CS} low before SCLK rising edge	–		1.5	–	–	ns	5
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	–		37.1	–	–	ns	5

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	–	50% levels 3.3V or 1.8V operation	148.4	–	–	ns	5
\overline{CS} high after SCLK falling edge	–		37.1	–	–	ns	5

Notes:

1. 1.89V and 0°C.
2. 3.47V and 0°C.
3. 1.71V and 85°C
4. 3.13V and 85°C
5. Timing parameters defined in [Section 4.20.3](#)
6. 0m cable length
7. Tested on a 2971 board from 5MHz to 3GHz.

3. Input/Output Circuits

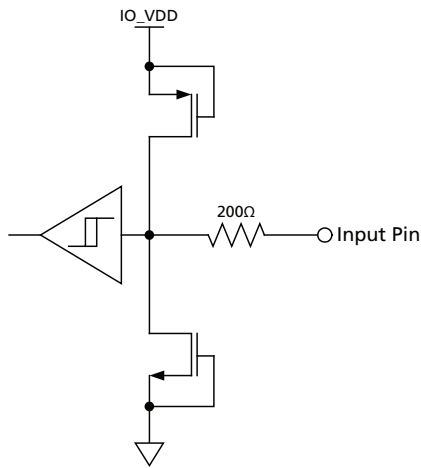


Figure 3-1: Digital Input Pin with Schmitt Trigger (20BIT/10BIT, AUDIO_EN/DIS, CS_TMS, SW_EN, IOPROC_EN/DIS, JTAG/HOST, RC_BYP, RESET_TRST, SCLK_TCK, SDIN_TDI, SDO_EN/DIS, STANDBY, TIM_861)

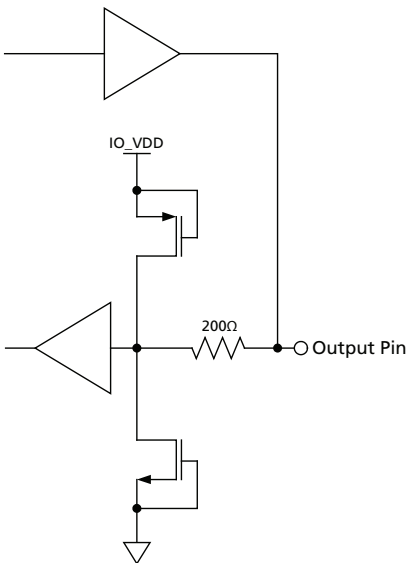


Figure 3-2: Bidirectional Digital Input/Output Pin - Configured to Output unless in Reset Mode. (ACLK, AMCLK, AOUT_1/2, AOUT_3/4, AOUT_5/6, AOUT_7/8, DVB_ASI, SMPTE_BYPASS, WCLK)