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SEMTECH
GENNUM PRODUCTS

GS9092A

GenLINX® III 270Mb/s Serializer for SDI and DVB-ASI

Key Features

- SMPTE 259M-C compliant scrambling and NRZI to NRZ encoding (with bypass)
- DVB-ASI sync word insertion and 8b/10b encoding
- Integrated Cable Driver
- Integrated line-based FIFO for data alignment/delay, clock phase interchange, DVB-ASI data packet insertion, and ancillary data packet insertion
- User selectable additional processing features including:
  - ANC data checksum, and line number calculation and insertion
  - TRS and EDH packet generation and insertion
  - illegal code remapping
- Enhanced Gennum Serial Peripheral Interface (GSPI)
- JTAG test interface
- +1.8V internal cable driver and core power supply
- Optional +1.8V or +3.3V digital I/O power supply
- Small footprint (8mm x 8mm)
- Low power operation (typically 200mW)
- Pb-free and RoHS compliant

Applications

- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

Description

The GS9092A is a 270Mb/s serializer with an internal FIFO and an integrated cable driver. It contains all the necessary blocks to realize a transmit solution for SD-SDI and DVB-ASI applications.

In addition to serializing the input data stream, the GS9092A performs NRZI-to-NRZ encoding and scrambling as per SMPTE 259M-C when operating in SMPTE mode. When operating in DVB-ASI mode, the device will insert K28.5 sync characters and 8b/10b encode the data prior to serialization.

Parallel data inputs are provided for 10-bit multiplexed formats at SD signal rates. A 27MHz parallel clock input signal is also required.

The integrated cable driver features an adjustable signal swing and common mode operating point offering fully compliant SMPTE 259M-C cable driver connectivity.

The GS9092A includes a range of data processing functions such as automatic standards detection and EDH support. The device can also insert TRS signals, re-map illegal code words, and generate and insert SMPTE 352M payload identifier packets. All processing features are optional and may be enabled/disabled via external control pin(s) and/or host interface programming.

The GS9092A also incorporates a video line-based FIFO. This FIFO may be used in four user-selectable modes to carry out tasks such as data delay, clock phase interchange, MPEG packet insertion and clock rate interchange, and ancillary data packet insertion.

The device may also be used as a low-latency parallel-to-serial converter where the SMPTE scrambling block will be the only processing feature enabled.

The GS9092A is Pb-free, and the encapsulation compound does not contain halogenated flame retardant (RoHS compliant).

GS9092A Functional Block Diagram

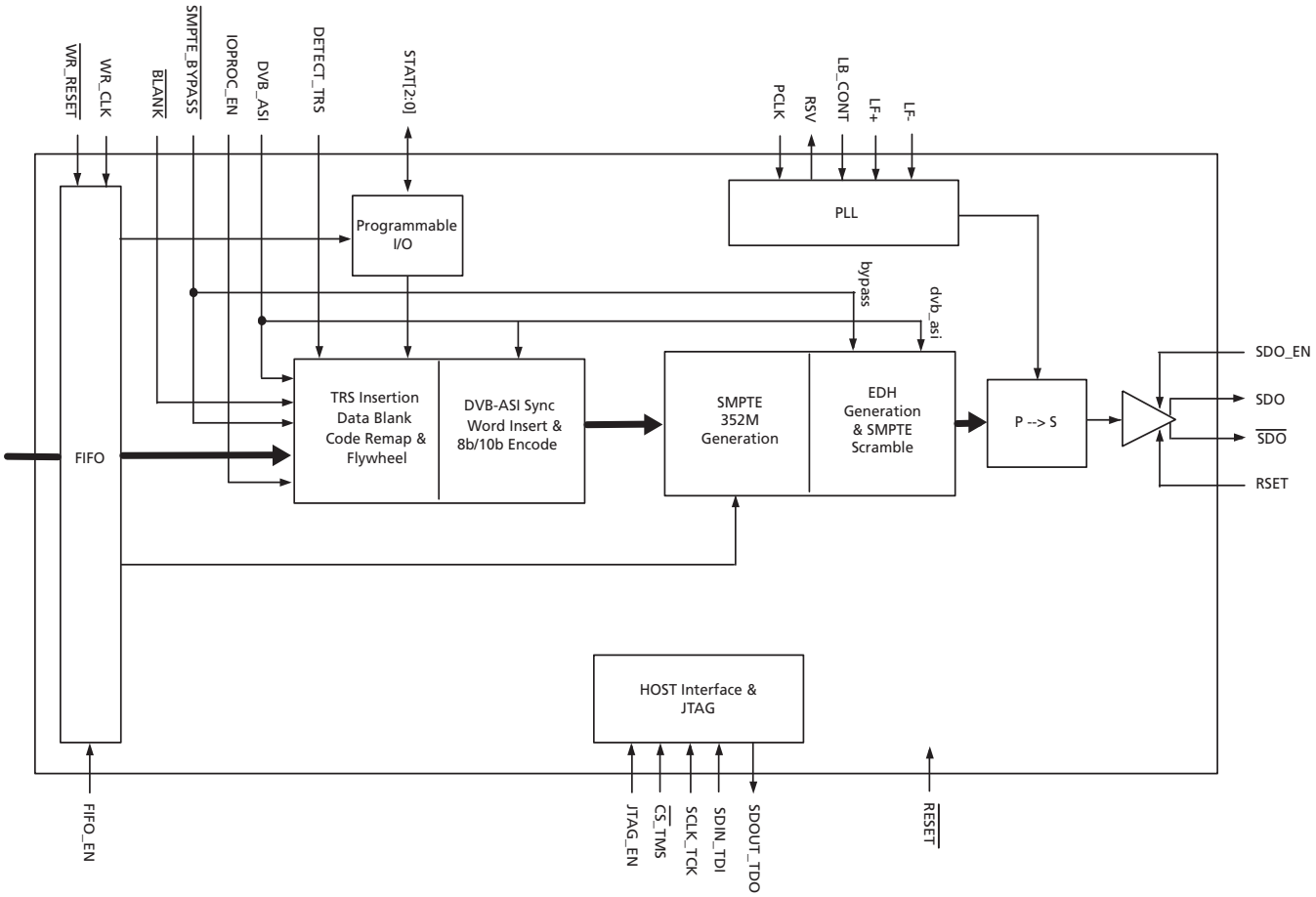

Figure A: GS9092A Functional Block Diagram

Contents

1. Pin Out

1.1 Pin Assignment

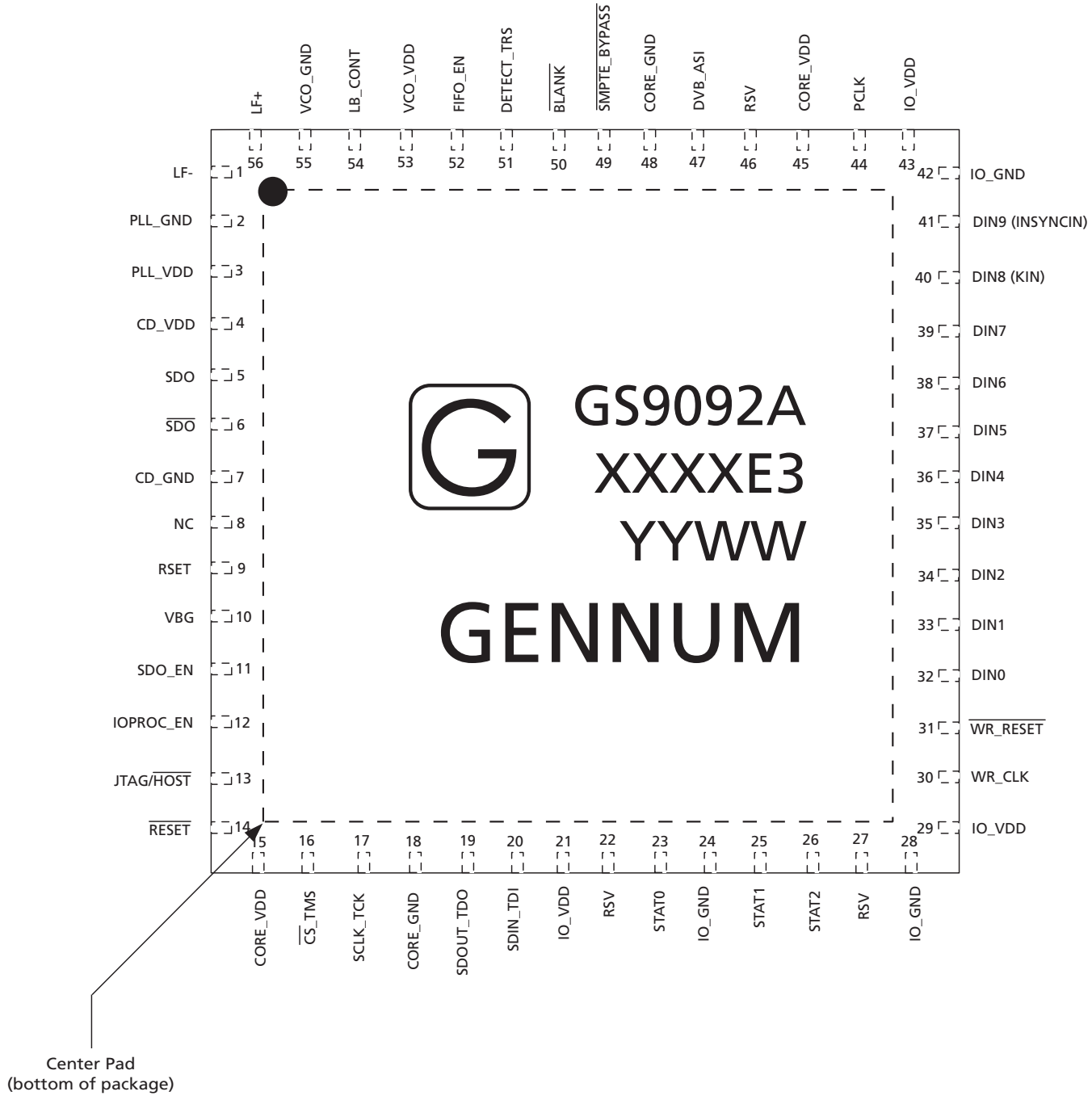

Figure 1-1: Pin Assignment

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	LF-	Analog	Input	Loop filter component connection. Connect to LF+ through a capacitor. See Typical Application Circuit on page 57.
2	PLL_GND	Analog	Input Power	Ground connection for phase-locked loop. Connect to GND.
3	PLL_VDD	Analog	Input Power	Power supply connection for phase-locked loop. Connect to +1.8V DC.
4	CD_VDD	Analog	Input Power	Power supply connection for serial digital cable driver. Connect to +1.8V DC
5, 6	SDO, $\overline{\text{SDO}}$	Analog	Output	Serial digital differential output pair. **Note:** these output signals will be forced into a mute state if $\overline{\text{RESET}}$ is LOW.
7	CD_GND	Analog	Input Power	Ground connection for serial digital cable driver. Connect to GND.
8	NC	–	–	No connect.
9	RSET	Analog	Input	An external 1% resistor connected between this input and CD_VDD is used to set the SDO / $\overline{\text{SDO}}$ output amplitude.
10	VBG	Analog	Input	Bandgap filter capacitor. Connect as shown in the Typical Application Circuit on page 57
11	SDO_EN	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible Used to enable or disable the serial digital output. When set LOW by the application layer, the serial digital output signals SDO and $\overline{\text{SDO}}$ are muted. When set HIGH by the application layer, the serial digital output signals are enabled. SDO and $\overline{\text{SDO}}$ outputs will also be high impedance when the $\overline{\text{RESET}}$ pin is LOW.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
12	IOPROC_EN	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal Levels are LVCMOS / LVTTL compatible. Used to enable or disable the I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • SMPTE 352M Payload Identifier Packet Generation and Insertion • Illegal Code Remapping • EDH Generation and Insertion • Ancillary Data Checksum Insertion • TRS Generation and Insertion To enable a subset of these features, keep the IOPROC_EN pin HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the host interface. When this pin is set LOW, the device will enter low-latency mode. **Note:** When the internal FIFO is configured for video mode or ancillary data insertion mode, the IOPROC_EN pin must be set HIGH.
13	JTAG/$\overline{\text{HOST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{\text{CS}}$_TMS, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured for JTAG boundary scan testing. When set LOW, $\overline{\text{CS}}$_TMS, SCLK_TCK, SDOUT_TDO, and SDIN_TDI are configured as GSPI pins for normal host interface operation.
14	$\overline{\text{RESET}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to reset the internal operating conditions to default setting or to reset the JTAG test sequence. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW): When asserted LOW, all functional blocks will be set to default conditions ,SDO and $\overline{\text{SDO}}$ are muted, and all input signals become high impedance with the exception of the STAT pins which will be driven LOW. When set HIGH, normal operation of the device resumes 10usec after the LOW-to-HIGH transition of the $\overline{\text{RESET}}$ signal. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH): When asserted LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes. **Note:** For power on reset requirements please see Device Power Up on page 56.
15, 45	CORE_VDD	Non Synchronous	Input Power	Power supply for digital logic blocks. Connect to +1.8V DC. **Note:** For power sequencing requirements please see Device Power Up on page 56.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
16	$\overline{CS}$_TMS	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Chip Select / Test Mode Select Host Mode (JTAG/$\overline{HOST}$ = LOW): $\overline{CS}$/TMS operates as the host interface chip select, $\overline{CS}$, and is active LOW. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH): $\overline{CS}$/TMS operates as the JTAG test mode select, TMS, and is active HIGH. **Note:** If this pin is unused it should be pulled up to VCC_IO.
17	SCLK_TCK	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Clock / Test Clock. All JTAG / Host Interface address and data is shifted into / out of the device synchronously with this clock. Host Mode (JTAG/$\overline{HOST}$ = LOW): SCLK_TCK operates as the host interface serial data clock, SCLK. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH): SCLK_TCK operates as the JTAG test clock, TCK. **Note:** If this pin is unused it should be pulled up to VCC_IO.
18, 48	CORE_GND	Non Synchronous	Input Power	Ground connection for digital logic blocks. Connect to GND.
19	SDOUT_TDO	Synchronous with SCLK_TCK	Output	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Output / Test Data Output Host Mode (JTAG/$\overline{HOST}$ = LOW): SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH): SDOUT_TDO operates as the JTAG test data output, TDO.
20	SDIN_TDI	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Serial Data Input / Test Data Input Host Mode (JTAG/$\overline{HOST}$ = LOW): SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH): SDIN_TDI operates as the JTAG test data input, TDI. **Note:** If this pin is unused it should be pulled up to VCC_IO.
21, 29, 43	IO_VDD	Non Synchronous	Input Power	Power supply for digital I/O. For a 3.3V tolerant I/O, connect pins to either +1.8V DC or +3.3V DC. For a 5V tolerant I/O, connect pins to a +3.3V DC. **Note:** For power sequencing requirements please see Device Power Up on page 56.
22, 27	RSV	–	–	Reserved. Do Not Connect.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
23, 25, 26	STAT[2:0]	Synchronous with PCLK or WR_CLK	Input/ Output	MULTI FUNCTION I/O PORT Signal levels are LVCMOS / LVTTL compatible. Programmable multi-function I/O. By programming the bits in the IO_CONFIG register, each pin can act as an output for one of the following signals: • H • V • F • FIFO_FULL • FIFO_EMPTY Each pin may also act as an input for an external H, V, or F signal if the DETECT_TRS pin is set LOW by the application layer These pins are set to certain default values depending on the configuration of the device and the internal FIFO mode selected. See Programmable Multi-function I/O on page 49 for details.
24, 28, 42	IO_GND	Non Synchronous	Input Power	Ground connection for digital I/O. Connect to GND.
30	WR_CLK		Input	FIFO WRITE CLOCK Signal levels are LVCMOS / LVTTL compatible. The application layer clocks the parallel data into the device on the rising edge of WR_CLK when the internal FIFO is configured for video mode or DVB-ASI mode. **Note:** If this pin is unused it should be pulled up to GND.
31	WR_RESET	Synchronous with WR_CLK	Input	FIFO WRITE RESET Signal levels are LVCMOS / LVTTL compatible. Valid input only when the device is in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH, DVB-ASI = LOW) and the internal FIFO is configured for video mode (Video Mode on page 26). A HIGH to LOW transition will reset the FIFO write pointer to address zero of the memory. **Note:** If this pin is unused it should be pulled up to GND.
32 - 41	DIN[9:0]	Synchronous with WR_CLK or PCLK	Input	PARALLEL VIDEO DATA BUS Signal levels are LVCMOS / LVTTL compatible. When the internal FIFO is enabled and configured for either video mode or DVB-ASI mode, parallel data will be clocked into the device on the rising edge of WR_CLK. When the internal FIFO is in bypass mode, parallel data will be clocked into the device on the rising edge of PCLK. DIN9 is the MSB and DIN0 is the LSB.
44	PCLK		Input	PIXEL CLOCK INPUT Signal levels are LVCMOS / LVTTL compatible. 27MHz parallel clock input.
46	RSV	–	–	Reserved. Do Not Connect.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
47	DVB_ASI	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. When set HIGH by the application layer, the device will be configured for the transmission of DVB-ASI data.The setting of the $\overline{\text{SMPTE\_BYPASS}}$ pin will be ignored. When set LOW by the application layer, the device will not support the encoding of DVB-ASI data.
49	$\overline{\text{SMPTE\_BYPASS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. When set HIGH in conjunction with DVB_ASI = LOW, the device will be configured to operate in SMPTE mode. All I/O processing features may be enabled in this mode. When set LOW, the device will not support the scrambling, encoding or packet insertion of received SMPTE data. No I/O processing features will be available and the device will enter a low-latency mode.
50	BLANK	Synchronous with PCLK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Functional only when chip is in SMPTE mode. When set LOW by the application layer, the luma and chroma input data is set to the appropriate blanking levels (TRS words will be unaltered at all times) When set HIGH by the application layer, the input data will pass into the device unaltered.
51	DETECT_TRS	Non Synchronous	Input	CONTOL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to select external H,V, and F timing mode or TRS extraction timing mode. When set LOW by the application layer, the device will extract all internal timing from the supplied H, V, and F timing signals. When set HIGH by the application layer, the device will extract all internal timing from the TRS signals embedded in the supplied video stream. The H, V, and F signals will become outputs that can be accessed via the STAT[2:0] pins. Both 8-bit and 10-bit TRS code words will be identified by the device.
52	FIFO_EN	Non Synchronous	Input	CONTOL SIGNAL INPUT Signal levels are LVCMOS / LVTTL compatible. Used to enable / disable the internal FIFO. When FIFO_EN is HIGH, the internal FIFO will be enabled. Data will be clocked into the device on the rising edge of the WR_CLK input pin if the FIFO is in video mode or DVB-ASI mode. When FIFO_EN is LOW, the internal FIFO is bypassed and parallel data is clocked into the device on the rising edge of the PCLK input.
53	VCO_VDD	Analog	Input Power	Power supply connection for Voltage-Controlled-Oscillator. Connect to +1.8V DC.
54	LB_CONT	Analog	Input	CONTROL SIGNAL INPUT Control voltage to fine-tune the loop bandwidth of the PLL.
55	VCO_GND	Analog	Input Power	Ground connection for Voltage-Controlled-Oscillator. Connect to GND.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
56	LF+	Analog	Input	Loop filter component connection. Connect to LF- through a capacitor. See Typical Application Circuit on page 57.
–	Center Pad	–	Power	Connect to GND following recommendations in Recommended PCB Footprint on page 59.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage Core	-0.3V to +2.1V
Supply Voltage I/O	-0.3V to +3.47V
Input Voltage Range (any input)	-2.0V to +5.25V
Ambient Operating Temperature	$-20°C \leq T_A \leq 85°C$
Storage Temperature	$-40°C \leq T_{STG} \leq 125°C$
ESD protection on all pins (see 1)	500 V

Note:

1. HBM, per JESDA - 114B

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
System							
Operating Temperature Range	T_A	–	0	25	70	°C	1
Core power supply voltage	CORE_VDD	–	1.71	1.8	1.89	V	–
Digital I/O Buffer Power Supply Voltage	IO_VDD	1.8V Operation	1.71	1.8	1.89	V	–
	IO_VDD	3.3V Operation	3.13	3.3	3.47	V	–
PLL Power Supply Voltage	PLL_VDD	–	1.71	1.8	1.89	V	–
VCO Power Supply Voltage	VCO_VDD	–	1.71	1.8	1.89	V	–

Table 2-1: DC Electrical Characteristics (Continued)

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
Serial Cable Driver Power Supply Voltage	CD_VDD	–	1.71	1.8	1.89	V	–
Typical System Power	P_D	CORE_VDD = 1.80V IO_VDD = 1.80V	–	200	–	mW	–
Max. System Power	P_D	CORE_VDD = 1.89V IO_VDD = 3.47V	–	–	300	mW	–
Digital I/O							
Input Voltage, Logic LOW	V_{IL}	1.8V or 3.3V Operation	–	–	0.35 x IO_VDD	V	–
Input Voltage, Logic HIGH	V_{IH}	1.8V or 3.3V Operation	0.65 x IO_VDD	–	–	V	–
Output Voltage, Logic LOW	V_{OL}	I_{OL} = 8mA @ 3.3V, 4mA @ 1.8V	–	–	0.4	V	–
Output Voltage, Logic HIGH	V_{OH}	I_{OL} = -8mA @ 3.3V, -4mA @ 1.8V	IO_VDD - 0.4	–	–	V	–
Serial Digital Outputs							
Output Common Mode Voltage Range	V_{CMOUT}	1.8V Pull-Up Reference Voltage	–	CD_VDD - V_{ODIFF}	–	V	–
Serial Driver Output Voltage Swing	V_{SDO}	1.8V Pull-up Reference Voltage, Single Ended 75Ω load	0	–	850	mV_{p-p}	2
Output Voltage Variation From Nominal	–	Over cable driver voltage supply range. RSET = 281Ω ($800mV_{p-p}$ single ended output)	-8.5	–	+8.5	%	–
	–	Output voltage variation from nominal (at 1.8V). RSET = 281Ω ($800mV_{p-p}$ single ended output)	-5	–	+5	%	–

Notes:

1. All DC and AC electrical parameters within specification.
2. Set by the value of the RSET resistor.

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
System							
Output High Impedance Response Time	t_{RHIGHZ}	SDO_EN = HIGH to LOW	–	20	–	ns	–
Digital I/O							
Input Data Setup Time	t_{SU}	50% PCLK vs. V_{IL}/V_{IH} data	3	–	–	ns	1
Input Data Hold Time	t_{IH}	50% PCLK vs. V_{IL}/V_{IH} data	1	–	–	ns	1
Output Data Hold Time	t_{OH}	With 15pF load	3	–	–	ns	2
Output Delay Time	t_{OD}	With 15pF load	–	–	11	ns	2
Serial Digital Output							
Serial Output Data Rate	BR_{SDO}	–	–	270	–	Mb/s	–
Serial Output Jitter	–	270Mb/s, V_{SDO} = 800mV, 75Ω load including rise/fall mismatch, PCLK input from GS9090A	–	360	555	ps_{p-p}	3
	–	PCLK input from the Agilent E4422B Signal Generator	–	225	–	ps_{p-p}	3,4
Serial Output Rise Time (20% ~ 80%)	SDO_{TR}	Return loss compensation recommended circuit - SMPTE 259M signal	400	500	1000	ps	–
Serial Output Fall Time (20% ~ 80%)	SDO_{TF}	Return loss compensation recommended circuit - SMPTE 259M signal	400	500	1000	ps	–
Mismatch in Rise/Fall Time	–	V_{ODIFF} = 1600mV, 100Ω differential load	–	–	30	ps	–
Serial Output Overshoot	–	V_{ODIFF} = 1600mV, 100Ω differential load	–	0	8	%	–

Table 2-2: AC Electrical Characteristics (Continued)

V_{DD} = 1.8V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units	Notes
Output Return Loss	ORL	@ 270Mb/s Using Semtech Evaluation board. Measured at the BNC with matching network.	15	–	–	dB	5, 6
Output Capacitance	C_{OUT}	Including pin and bonding parasitics	–	–	5	pF	–
GSPI							
GSPI Input Clock Frequency	f_{GSPI}	–	–	–	54.0	MHz	–
GSPI Clock Duty Cycle	DC_{GSPI}	–	40	–	60	%	–
GSPI Setup Time	t_{GS}	–	1.5	–	–	ns	–
GSPI Hold Time	t_{GH}	–	–	–	1.5	ns	–

Notes:

1. Timing includes the following inputs: DIN[9:0], H, V, F, WR_CLK, $\overline{\text{WR\_RESET}}$, $\overline{\text{BLANK}}$. When the FIFO is enabled, the following signals are measured with respect to WR_CLK: $\overline{\text{WR\_RESET}}$, DIN[9:0], INSSYNCIN, KIN.
2. Refers to when H, V, and F are output pins
3. Measured using pseudorandom bit sequence (2^{23}-1) over full input voltage range.
4. PCLK = 27MHz driven from the Agilent E4422B Signal Generator and serial output jitter measured using the Tektronix CSA8000 Oscilloscope.
5. 5MHz to 270MHz.
6. See 'Output Return Loss Measurement" on page 47.

2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-1. The recommended standard eutectic reflow profile is shown in Figure 2-2.

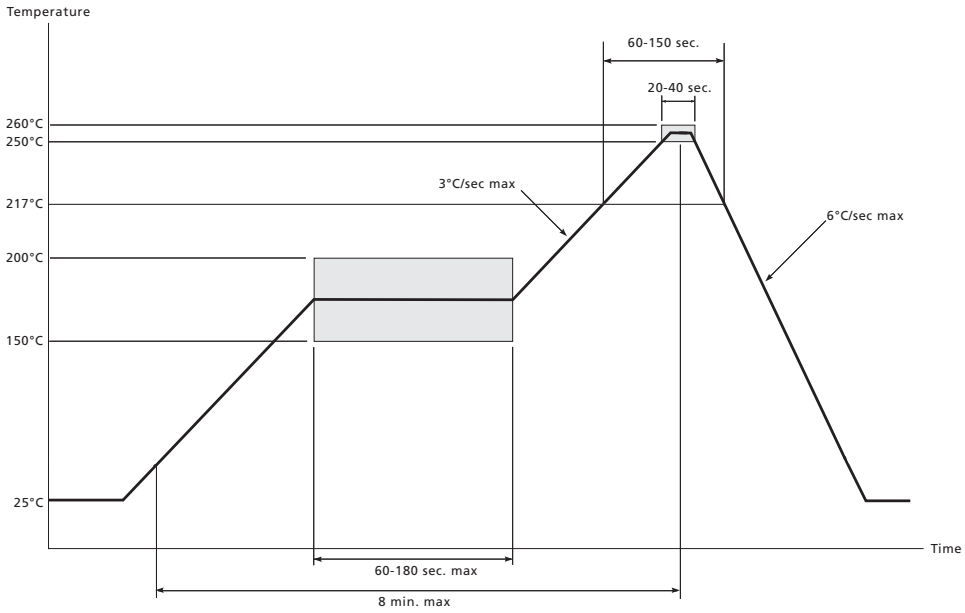

Figure 2-1: Maximum Pb-free Solder Reflow Profile (Preferred)

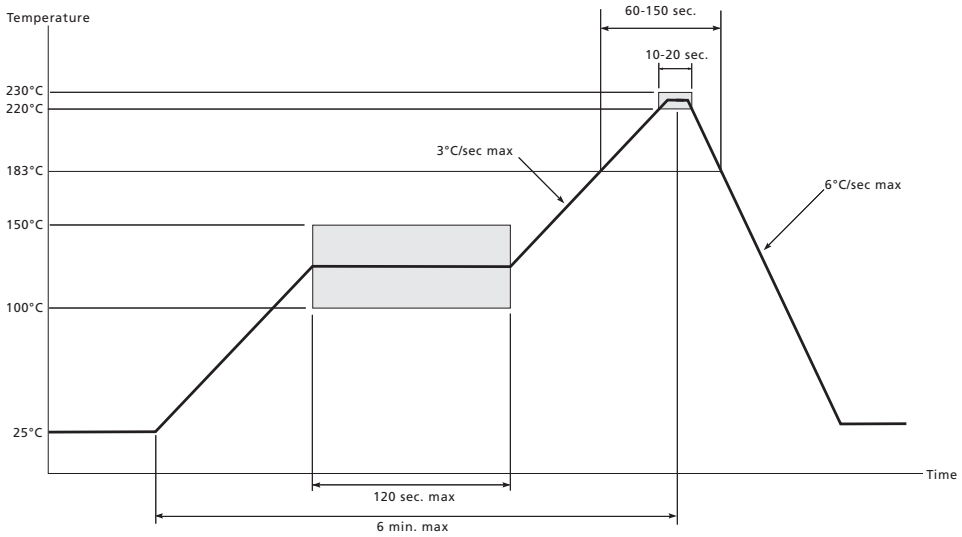

Figure 2-2: Standard Eutectic Solder Reflow Profile

2.5 Host Interface Maps

Table 2-3: Host Interface Maps

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANC_WORDS[10:0]	28h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
352M_LINE_2[10:0]	27h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
352M_LINE_1[10:0]	26h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	25h																
FF_PIXEL_END_F1[12:0]	24h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	1Ah	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE4[10:0]	14h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2[12:0]	12h	Not Used	Not Used	Not Used	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_B	10h	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_A	0Fh	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
ANC_LINE_B[10:0]	09h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_A[10:0]	08h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Table 2-3: Host Interface Maps (Continued)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_EMPTY_OFFSET	06h	Not Used	Not Used	ANC_ DATA_ RDBACK	ANC_ FIFO_ READY	ANC_ DATA_ REPLACE	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h	Not Used	Not Used	ANC_SAV	ANC_ DATA_ SWITCH	Not Used	Not Used	Not Used	STAT2_ CONFIG b2	STAT2_ CONFIG b1	STAT2_ CONFIG b0	STAT1_ CONFIG b2	STAT1_ CONFIG b1	STAT1_ CONFIG b0	STAT0_ CONFIG b2	STAT0_ CONFIG b1	STAT0_ CONFIG b0
VIDEO_STANDARD	04h	Not Used	Not Used	Not Used	Not Used	EDH_CRC_ UPDATE	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	STD_ LOCK	Not Used	Not Used	Not Used	Not Used
	03h																
EDH_FLAG	02h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	01h																
IOPROC_DISABLE	00h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	ANC_PKT_ INS	FIFO_ MODE b1	FIFO_ MODE b0	H_ CONFIG	352M_ CALC	352M_ INS	ILLEGAL_ REMAP	EDH_CRC_ INS	ANC_ CSUM_ INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. These registers may be written to in Ancillary Data Insertion mode (see Section 3.3.3)

2.5.1 Host Interface Map (Read only registers)

Table 2-4: Host Interface Map (Read only registers)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	28h																
	27h																
	26h																
	25h																
	24h																
	23h																
	22h																
	21h																
	20h																
	1Fh																
	1Eh																
	1Dh																
	1Ch																
	1Bh																
	1Ah																
	19h																
	18h																
	17h																
	16h																
	15h																
RASTER_STRUCTURE4[10:0]	14h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3[12:0]	13h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2[12:0]	12h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1[10:0]	11h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	10h																
	0Fh																
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
	09h																
	08h																
	07h																

Table 2-4: Host Interface Map (Read only registers) (Continued)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_EMPTY_OFFSET	06h				ANC_ FIFO_ READY												
	05h																
VIDEO_STANDARD	04h												STD_ LOCK				
	03h																
	02h																
	01h																
	00h																

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. These registers may be written to in Ancillary Data Insertion mode (see Section 3.3.3)

2.5.2 Host Interface Map (R/W configurable registers)

Table 2-5: Host Interface Map (R/W configurable registers)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANC_WORDS[10:0]	28h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
352M_LINE_2[10:0]	27h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
352M_LINE_1[10:0]	26h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	25h																
FF_PIXEL_END_F1[12:0]	24h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F1[12:0]	23h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_END_F0[12:0]	22h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_PIXEL_START_F0[12:0]	21h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F1[12:0]	20h				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F1[12:0]	1Fh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_END_F0[12:0]	1Eh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_PIXEL_START_F0[12:0]	1Dh				b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F1[10:0]	1Ch						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1[10:0]	1Bh						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0[10:0]	1Ah						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0[10:0]	19h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1[10:0]	18h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1[10:0]	17h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0[10:0]	16h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0[10:0]	15h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	14h																
	13h																
	12h																
	11h																
VIDEO_FORMAT_B	10h	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_A	0Fh	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
ANC_LINE_B[10:0]	09h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_LINE_A[10:0]	08h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FIFO_FULL_OFFSET	07h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Table 2-5: Host Interface Map (R/W configurable registers) (Continued)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO_EMPTY_OFFSET	06h			ANC_ DATA_ RDBACK		ANC_ DATA_ REPLACE		b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
IO_CONFIG	05h	Not Used	Not Used	ANC_SAV	ANC_ DATA_ SWITCH	Not Used	Not Used	Not Used	STAT2_ CONFIG b2	STAT2_ CONFIG b1	STAT2_ CONFIG b0	STAT1_ CONFIG b2	STAT1_ CONFIG b1	STAT1_ CONFIG b0	STAT0_ CONFIG b2	STAT0_ CONFIG b1	STAT0_ CONFIG b0
VIDEO_STANDARD	04h	Not Used	Not Used	Not Used	Not Used	EDH_CRC_ UPDATE	Not Used	Not Used									
	03h																
EDH_FLAG	02h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	01h																
IOPROC_DISABLE	00h							ANC_PKT_ INS	FIFO_ MODE b1	FIFO_ MODE b0	H_ CONFIG	352M_ CALC	352M_ INS	ILLEGAL_ REMAP	EDH_CRC_ INS	ANC_ CSUM_ INS	TRS_IN

NOTE: Addresses 02Ch to 42Bh store the contents of the internal FIFO. These registers may be written to in Ancillary Data Insertion mode (see Section 3.3.3).

3. Detailed Description

3.1 Functional Overview

The GS9092A is a 270Mb/s serializer with an internal FIFO and a programmable multi-function I/O port. The device has 3 different modes of operation which must be set by the application layer through external device pins.

When SMPTE mode is enabled, the device will accept 10-bit multiplexed SMPTE compliant data at 27MHz. The device's additional processing features are also enabled in this mode.

In DVB-ASI mode, the GS9092A will accept an 8-bit parallel DVB-ASI compliant transport stream. The serial output data stream will be 8b/10b encoded and padded with K28.5 fill characters.

The GS9092A's third mode allows for the serializing of data not conforming to SMPTE or DVB-ASI streams.

The serial digital outputs feature a high impedance mode and adjustable signal swing.

In the digital signal processing core, several data processing functions are implemented including SMPTE 352M and EDH data packet generation and insertion, and automatic video standards detection. These features are all enabled by default, but may be individually disabled via internal registers accessible through the GSPI host interface.

The provided programmable multi-function I/O pins may be configured to input and output various status signals including H, V, and F timing, a FIFO_FULL, and a FIFO_EMPTY pulse. The internal FIFO supports 4 modes of operation, which may be used for data delay, MPEG packet insertion, or ancillary data insertion.

Finally, the GS9092A contains a JTAG interface for boundary scan test implementations.

3.2 Parallel Data Inputs

Data inputs enter the device on the rising edge of either PCLK or WR_CLK, depending on the configuration of the internal FIFO.

When the internal FIFO is bypassed or in ancillary data insertion mode (see Ancillary Data Insertion Mode on page 30), data enters the device on the rising edge of PCLK as shown in Figure 3-1. When the internal FIFO is configured for video mode, data enters the device on the rising edge of WR_CLK (see Video Mode on page 26).

The input data format is defined by the setting of the external $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins (Table 3-1). Input data must be presented in 10-bit format.

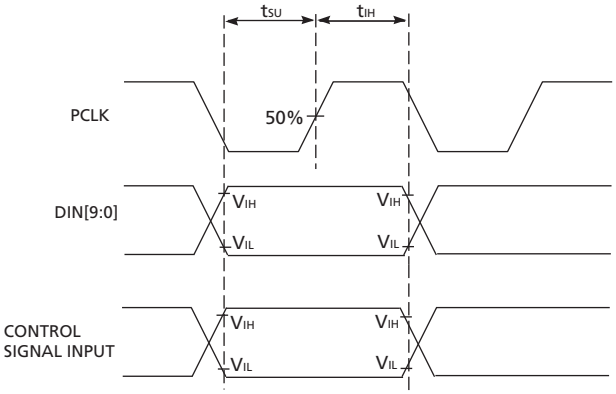

Figure 3-1: PCLK to Input Data Timing

Note: For a SMPTE compliant serial output, the jitter on the input PCLK across the frequency spectrum should not exceed 350ps.

3.2.1 Parallel Input in SMPTE Mode

When the device is operating in SMPTE mode (see SMPTE Mode on page 34), SD data is presented to the input bus in 10-bit multiplexed format. The input data format must be word aligned, multiplexed luma and chroma data.

Note: When operating the device in an 8-bit SMPTE system, the 2 LSBs (DIN [1:0]) must be set to 0.

Table 3-1: Input Data Format Selection

		Pin Settings	
Input Data Format	**DIN[9:0]**	**$\overline{\text{SMPTE\_BYPASS}}$**	**DVB_ASI**
10-bit Data	DATA	LOW	LOW
10-bit Multiplexed SD	Luma/Chroma	HIGH	LOW
10-bit DVB-ASI	DVB-ASI data	X	HIGH

3.2.2 Parallel Input in DVB-ASI Mode

When operating in DVB-ASI mode (see DVB-ASI Mode on page 35), the device will accept 8-bit data words on DIN[7:0] such that DIN7 = HIN is the most significant bit of the encoded transport stream data and DIN0 = AIN is the least significant bit.

In addition, DIN9 and DIN8 will be configured as the DVB-ASI control signals INSSYNCIN and K_IN respectively. See Control Signal Inputs on page 35 for a description of these DVB-ASI specific input signals.

3.2.3 Parallel Input in Data-Through Mode

When operating in Data-Through mode (see Data-Through Mode on page 36), the GS9092A passes data presented to the parallel input bus to the serial output without performing any encoding, scrambling, or word-alignment.

3.2.4 I/O Buffers

The parallel data bus, status signal outputs, and control signal input pins are all connected to high-impedance buffers. These buffers use either +1.8V or +3.3V DC, supplied at the IO_VDD and IO_GND pins. For a +3.3V tolerant I/O, the IO_VDD pins can be connected to either +1.8V or +3.3V. For a +5V tolerant I/O, the IO_VDD pins must be supplied with +3.3V.

While $\overline{\text{RESET}}$ is LOW, STAT output pins are muted and all other output pins become high impedance.

3.3 Internal FIFO Operation

The GS9092A contains an internal video line-based FIFO, which can be programmed by the application layer to work in any of the following modes:

1. Video Mode

2. DVB-ASI Mode
3. Ancillary Data Insertion Mode
4. Bypass Mode

The FIFO can be configured to one of the four modes by setting the FIFO_MODE[1:0] bits of the IOPROC_DISABLE register via the host interface (see Table 3-4 in Packet Generation and Insertion on page 37). The setting of these bits is shown in Table 3-2. To enable the FIFO, the application layer must also set the FIFO_EN pin HIGH. Additionally, if the FIFO is configured for video mode or ancillary data insertion mode, the IOPROC_EN pin must be set HIGH.

The FIFO is fully asynchronous, allowing simultaneous read and write access. It has a depth of 2048 words, and can store up to 1 full line of SD video for both 525 and 625 standards.

Note: The F, V, and H signals will be ignored when the FIFO is configured for DVB-ASI mode or bypass mode.

Table 3-2: FIFO Configuration Bit Settings

FIFO Mode	FIFO_MODE[1:0] Register Setting	FIFO_EN Pin Setting	IOPROC_EN Pin Setting
Video Mode	00b	HIGH	HIGH
DVB-ASI Mode	01b	HIGH	X
Ancillary Data Insertion Mode	10b	HIGH	HIGH
Bypass Mode	11b	X	X

Note: 'X' signifies 'don't care'. The pin is ignored and may be set HIGH or LOW.