Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

WT41u

DATA SHEET

Monday, 12 December 2016

Version 0.8.7

VERSION HISTORY

Version	Comment
0.8	First version
0.8.1	Table reformatting, value updates etc
0.8.2	Replaced “Bluecore4” with “chipset”, added ordering codes
0.8.3	Rest of table reformatting, added antenna & connector dimension drawings
0.8.4	Added current consumption, RF characteristics
0.8.5	Added certification texts
0.8.6	Added current consumption results, edit TX power variation over VDD range.
0.8.7	Slight edits to specifications

TABLE OF CONTENTS

1 Ordering Information 6
2 Pinout and Terminal Description 7
3 Electrical Characteristics 11
3.1 Absolute Maximum Ratings 11
3.2 Recommended Operating Conditions 11
3.3 Input / Output Terminal Characteristics 12
3.3.1 Input/Output Terminal Characteristics (Digital) 12
3.3.2 Input/Output Terminal Characteristics (USB) 13
3.4 PIO Current Sink and Source Capability 13
3.5 Transmitter Performance For BDR 14
3.6 Receiver Performance 15
3.7 Current Consumption 15
4 Physical Dimensions 16
5 Layout Guidelines 19
6 UART Interface 20
6.1 UART Bypass 22
6.2 UART Configuration While Reset is Active 22
6.3 UART Bypass Mode 22
7 USB Interface 23
7.1 USB Data Connections 23
7.2 USB Pull-Up resistor 23
7.3 USB Power Supply 23
7.4 Self-Powered Mode 23
7.5 Bus-Powered Mode 24
7.6 USB Suspend Current 25
7.7 USB Detach and Wake-Up Signaling 25
7.8 USB Driver 26
7.9 USB v2.0 Compliance and Compatibility 26
8 Serial Peripheral Interface (SPI) 27
9 PCM Codec Interface 28
9.1 PCM Interface Master/Slave 28
9.2 Long Frame Sync 29
9.3 Short Frame Sync 29
9.4 Multi-slot Operation 30
9.5 GCI Interface 30
9.6 Slots and Sample Formats 31
9.7 Additional Features 32

9.8 PCM_CLK and PCM_SYNC Generation 32
9.9 PCM Configuration 33
10 I/O Parallel Ports 36
10.1 PIO Defaults 36
11 Reset 37
11.1 Pin States on Reset 38
12 Certifications 39
12.1 Bluetooth 39
12.2 FCC 39
12.3 ISEDC 40
12.3.1 ISEDC (Français) 40
12.4 CE 41
12.5 MIC Japan 42
12.6 Qualified Antenna Types for WT41u-E and WT41u-N 43
12.7 Moisture Sensitivity Level (MSL) 43

WT41u *Bluetooth®* Module

DESCRIPTION

WT41u is a long range class 1, Bluetooth® 2.1 + EDR module. WT41u is a highly integrated and sophisticated Bluetooth® module, containing all the necessary elements from Bluetooth® radio and a fully implemented protocol stack. Therefore WT41u provides an ideal solution for developers who want to integrate Bluetooth® wireless technology into their design with limited knowledge of Bluetooth® and RF technologies. WT41u is optimized for long range applications is available with an integrated chip antenna, an RF pin for a custom on-board antenna or a U.FL connector for an external 2dBi dipole antenna.

By default WT41u module is equipped with powerful and easy-to-use iWRAP firmware. iWRAP enables users to access Bluetooth® functionality with simple ASCII commands delivered to the module over serial interface - it's just like a Bluetooth® modem.

APPLICATIONS:

- Hand held terminals
- Industrial devices
- Point-of-Sale systems
- PCs
- Personal Digital Assistants (PDAs)
- Computer Accessories
- Access Points
- Automotive Diagnostics Units

FEATURES:

- Fully Qualified Bluetooth v2.1 + EDR end product
- CE qualified
- Full modular certification for FCC and IC
- MIC Japan compatibility fully tested with ARIB STD-T66
- TX power : 17 dBm
- RX sensitivity : -94 dBm
- Integrated chip antenna, RF pin or U.FL antenna connector
- Class 1, range up to 650 meters with chip antenna or up to 1km with an external dipole
- Industrial temperature range from -40ºC to +85ºC
- RoHS Compliant
- USB interface (USB 2.0 compatible)
- UART with bypass mode
- 6 x GPIO
- 1 x 8-bit AIO
- Integrated iWRAP™ Bluetooth stack or HCI firmware

1 Ordering Information

Firmware	U.FL Connector	Internal chip antenna
iWRAP 5.6 firmware	WT41u-E-AI56	WT41u-A-AI56
iWRAP 5.5 firmware	WT41u-E-AI55	WT41u-A-AI55
iWRAP 5.0.1 firmware	WT41u-E-AI5	WT41u-A-AI5
HCI firmware, BT2.1 + EDR	WT41u-E-HCI21	WT41u-A-HCI21

Table 1: Ordering information

2 Pinout and Terminal Description

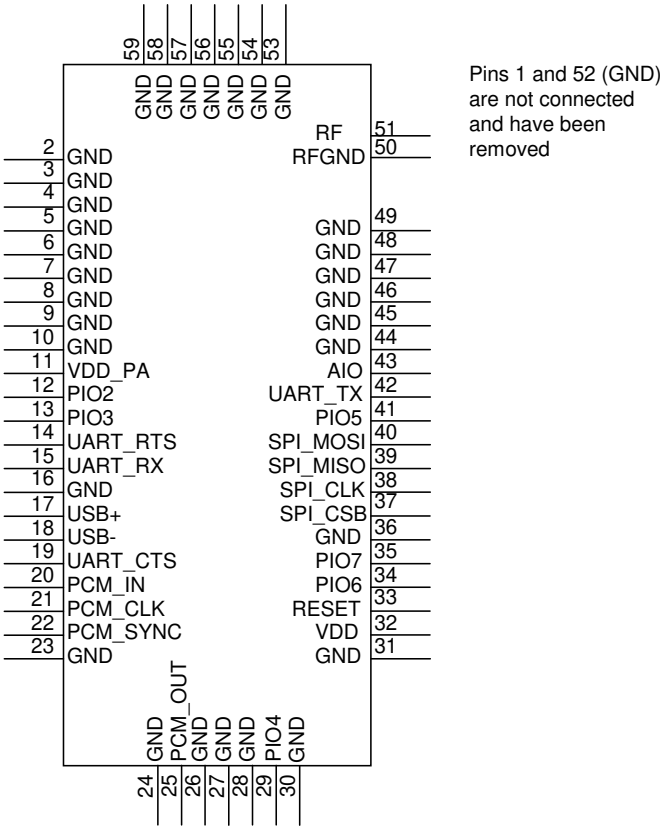

Figure 1: WT41u pin out

Pad name	Pad number	Pad type	Description
NC	1, 52	Not connected	Pins 1 and 52 are not present on the footprint
RESET	33	Digital input	Active low reset with weak internal pull-up. Keep low for >5ms to reset module
GND	2-10, 16, 23, 24, 26-28, 30, 31, 36, 44-49, 53-59	Ground	Ground pads should all be connected to a ground plane with minimum trace length, especially on the antenna end of the module
RF	51	Not connected	No internal connection
RFGND	50	Ground	Connect to ground plane
VDD_PA	11	Supply voltage	Supply voltage for the RF power amplifier and low noise amplifier
VDD	32	Supply voltage	Supply voltage for the Bluetooth chipset

Table 2: Supply and RF Terminal Descriptions

PIO signal	Pad number	Description
PIO[2]	12	Bi-directional digital in/out with programmable strength and pull-up/pull-down
PIO[3]	13	Bi-directional digital in/out with programmable strength and pull-up/pull-down
PIO[4]	29	Bi-directional digital in/out with programmable strength and pull-up/pull-down
PIO[5]	41	Bi-directional digital in/out with programmable strength and pull-up/pull-down
PIO[6]	34	Bi-directional digital in/out with programmable strength and pull-up/pull-down
PIO[7]	35	Bi-directional digital in/out with programmable strength and pull-up/pull-down
AIO[1]	43	Bi-directional analog in/out

Table 3: GPIO Terminal Descriptions

PCM signal	Pad number	Pad type	Description
PCM_OUT	25	Output, weak internal pull-down	Synchronous data output
PCM_IN	20	Input, weak internal pull-down	Synchronous data input
PCM_SYNC	22	Bi-directional, weak internal pull-down	Synchronous data sync
PCM_CLK	21	Bi-directional, weak internal pull-down	Synchronous data clock

Table 4: PCM Terminal Descriptions

UART signal	Pad number	Pad type	Description
UART_TX	42	Output, weak internal pull-up	UART data output, active high
UART_RTS#	14	Output, weak internal pull-up	UART request to send, active low
UART_RX	15	Input, weak internal pull-down	UART data input, active high
UART_CTS#	19	Input, weak internal pull-down	UART clear to send, active low

Table 5: UART Terminal Descriptions

USB signal	Pad number	Pad type	Description
USB+	17	Bidirectional	USB data line with internal 1.5kohm pull-up
USB-	18	Bidirectional	USB data line

Table 6: USB Terminal Descriptions

SPI signal	Pad number	Pad type	Description
SPI_MOSI	40	Input, weak internal pull-down	SPI data input
SPI_CS#	37	Input, weak internal pull-up	Chip select, active low
SPI_CLK	38	Input, weak internal pull-down	SPI clock
SPI_MISO	39	Output, weak internal pull-down	SPI data output

Table 7: Terminal Descriptions

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Specification	Min	Max	Unit
Storage temperature	-40	85	°C
VDD_PA, VDD	-0.4	3.7	V
Other terminal voltages	VSS-0.4	VDD+0.4	V

Table 8: Absolute Maximum Ratings

3.2 Recommended Operating Conditions

Specification	Min	Max	Unit
Operating temperature	-40	85	°C
VDD_PA, VDD	3.0	3.6	V

Table 9: Recommended Operating Conditions

3.3 Input / Output Terminal Characteristics

3.3.1 Input/Output Terminal Characteristics (Digital)

Digital Terminals		Min	Typ	Max	Unit
Input Voltage Levels					
V_{IL} input logic level low	2.7 V ≤ VDD ≤ 3.0 V	-0.4	-	0.8	V
	1.7 V ≤ VDD ≤ 1.9 V	-0.4	-	0.4	V
V_{IH} input logic level high		0.7 VDD	-	VDD + 0.4	V
Output Voltage Levels					
V_{OL} output logic level low (I_O = 4.0 mA) 2.7V ≤ VDD ≤ 3.0 V		-	-	0.2	V
VOL output logic level low (I_O = 4.0 mA) 1.7V ≤ VDD ≤ 1.9		-	-	0.4	V
VOL output logic level high (I_O = 4.0 mA) 2.7V ≤ VDD ≤ 3.0		VDD - 0.2	-		V
VOL output logic level high (I_O = 4.0 mA) 1.7V ≤ VDD ≤ 1.9		VDD - 0.4	-		V
Input and Tristate Current with					
Strong pull-up		-100	-40	-10	µA
Strong pull-down		10	40	100	µA
Weak pull-up		-5.0	-1.0	-0.2	µA
Weak pull-down		0.2	1.0	5.0	µA
I/O pad leakage current		-1	0	1	µA
C_I input capacitance		1.0	-	5.0	pF

3.3.2 Input/Output Terminal Characteristics (USB)

USB Terminals	Min	Typ	Max	Unit
VDD_USB for correct USB operation	3.1		3.6	V
Input Threshold				
V_{IL} input logic level log	-	-	0.3VDD_USB	V
V_{IH} input logic level high	0.7VDD_USB	-	-	V

3.4 PIO Current Sink and Source Capability

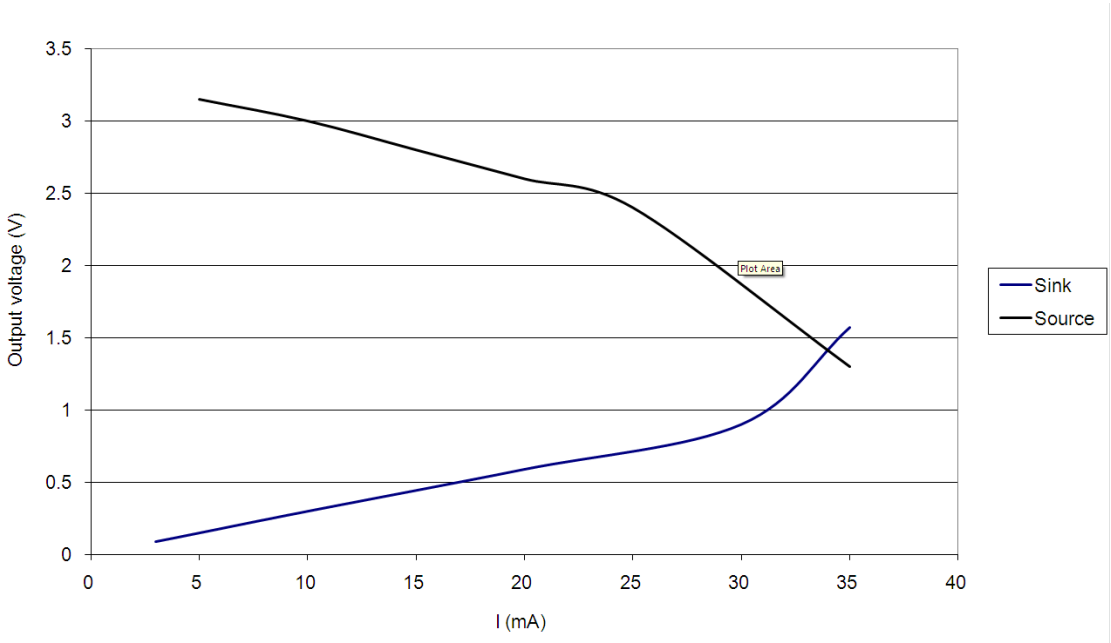

Figure 2: WT41u PIO Current Drive Capability

3.5 Transmitter Performance For BDR

RF characteristic	Min	Typ	Max	Bluetooth specification	Unit
Max transmit power	16	17	18	<20	dBm
Transmit power variation over temperature range	-2		2		dB
Transmit power variation over supply voltage range	-0.5		0.5		dB
Transmit power variation over frequency range	-0.5		0.5		dB
Transmit power control range	-13		17		dBm
20dB bandwidth for modulated carrier		998		<1000	kHz
Avg drift	-11		6	±40	kHz
ΔF1avg		165		140 to 175	kHz

3.6 Receiver Performance

Antenna gain not taken into account

Characteristic, VDD=3.3V, room temperature	Packet type	Typ	Bluetooth specification	Unit
Sensitivity for 0.1% BER	DH1	-94.1	-70	dBm
	DH5	-90.5		dBm
	2-DH1	-96.5		dBm
	2-DH5	-94.5		dBm
	3-DH1	-89.5		dBm
	3-DH5	-86		dBm
Sensitivity variation over temperature range		+/-2		dB

Table 10: Receiver sensitivity

3.7 Current Consumption

Operating mode	Peak	Average	Unit
Stand-by, page mode 0 2000 1		2	mA
TX 3-DH5	108	85	mA
TX 2-DH5	108	85	mA
TX DH5	184	136	mA
RX	50	44	mA
Deep sleep, page mode 0 2000 1		0.36	mA
Inquiry	113	58	mA

Table 11: Current consumption

4 Physical Dimensions

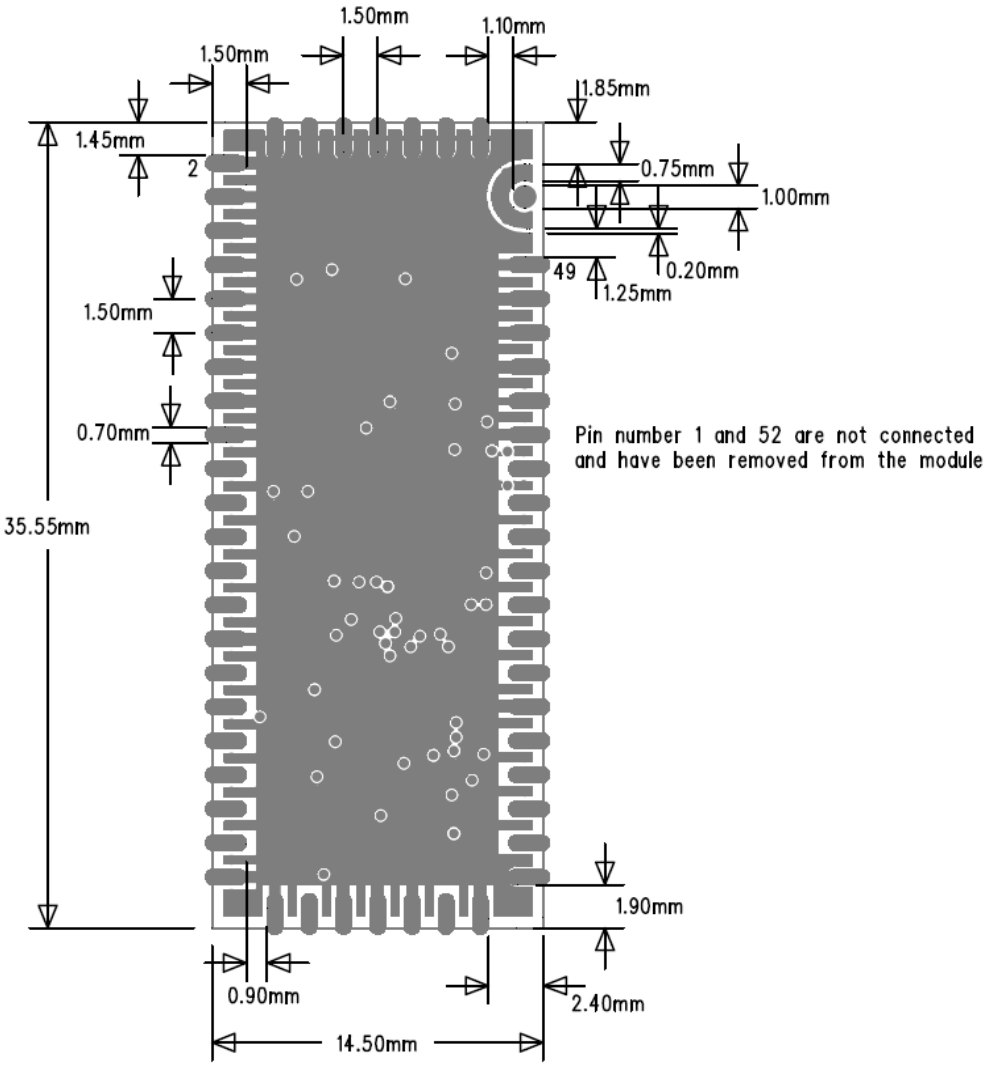

Figure 3: Physical dimensions (top view)

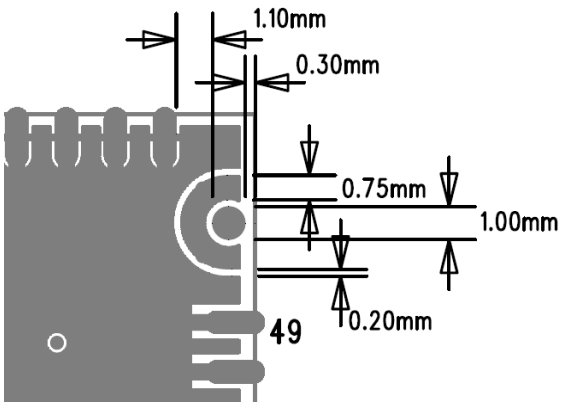

Figure 4: Dimensions for the RF pin used as antenna connection on WT41u-N (top view)

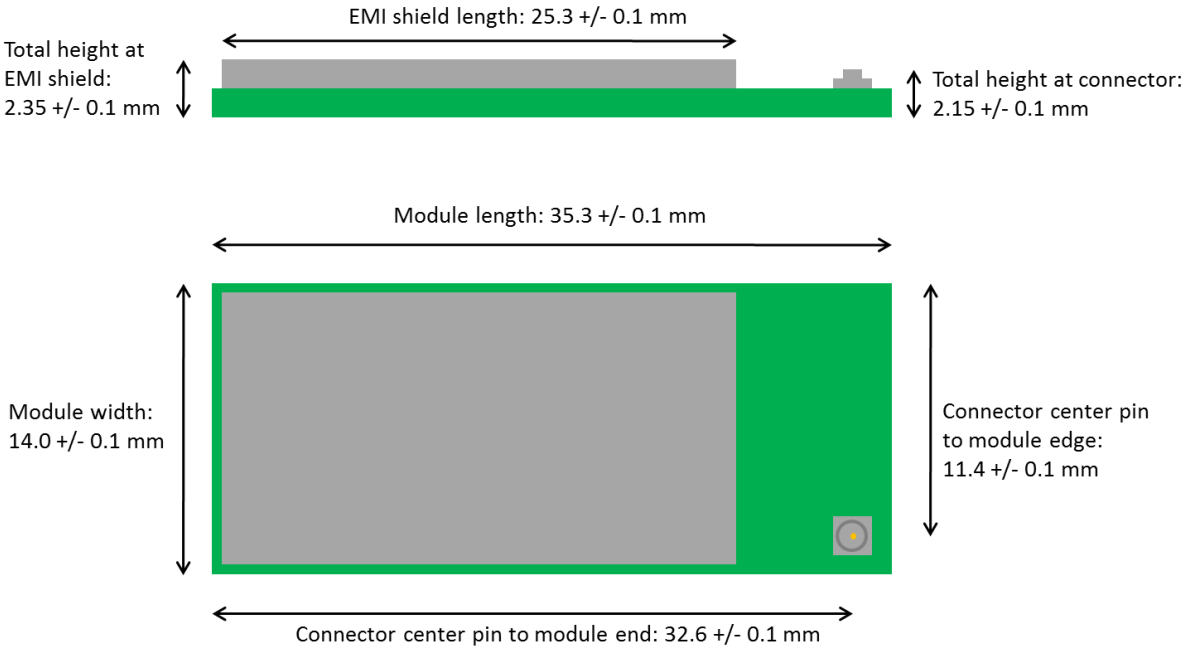

Figure 5: Dimensions of WT41u-E

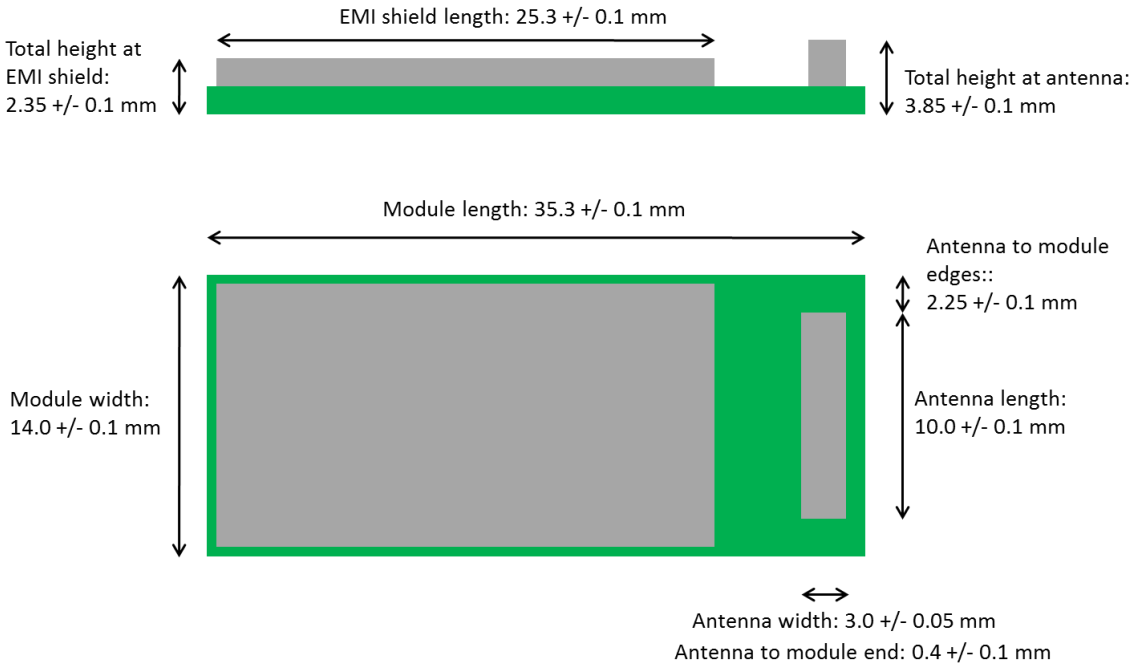

Figure 6: Dimensions of WT41u-A

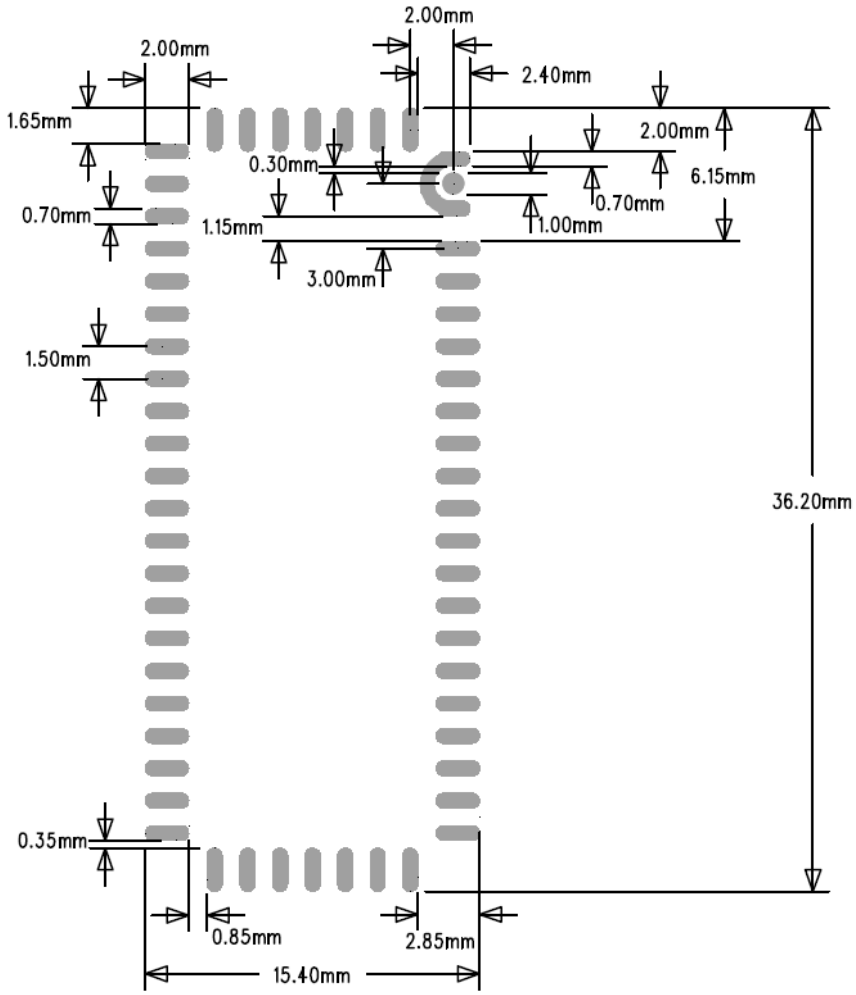

Figure 7: Recommended land pattern

5 Layout Guidelines

Use good layout practices to avoid excessive noise coupling to supply voltage traces or sensitive analog signal traces, such as analog audio signals. If using overlapping ground planes use stitching vias separated by max 3 mm to avoid emission from the edges of the PCB. Connect all the GND pins directly to a solid GND plane and make sure that there is a low impedance path for the return current following the signal and supply traces all the way from start to the end.

A good practice is to dedicate one of the inner layers to a solid GND plane and one of the inner layers to supply voltage planes and traces and route all the signals on top and bottom layers of the PCB. This arrangement will make sure that any return current follows the forward current as close as possible and any loops are minimized.

Figure 8: Typical 4-layer PCB construction

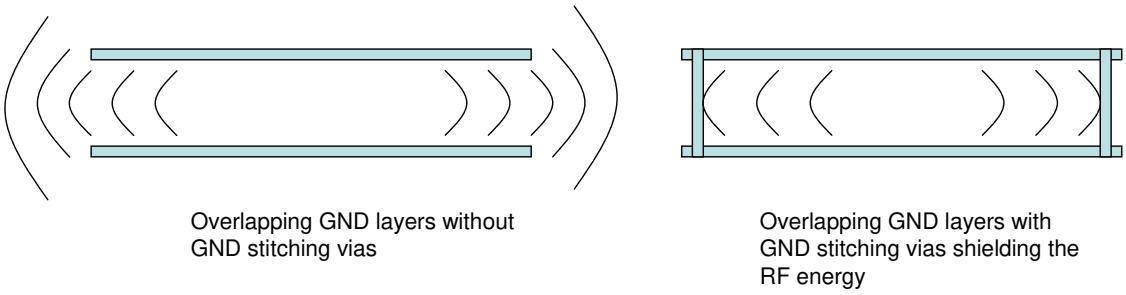

Figure 9: Use of stitching vias to avoid emissions from the edges of the PCB

6 UART Interface

This is a standard UART interface for communicating with other serial devices.WT41u UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

Four signals are used to implement the UART function. When WT41u is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. All UART connections are implemented using CMOS technology and have signalling levels of 0V and VDD.

UART configuration parameters, such as data rate and packet format, are set using WT41u software.

Note:

In order to communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter	Possible values	
Data rate	Minimum	1200bps (2% error)
		9600bps (1% error)
	Maximum	3Mbps (1% error)
Flow control	RTS/CTS or None	
Parity	None, Odd or Even	
Number of stop bits	1 or 2	
Bits per channel	8	

Table 12: Possible UART Settings

The UART interface is capable of resetting WT41u upon reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as shown in Figure 10. If tBRK is longer than the value, defined by PSKEY_HOST_IO_UART_RESET_TIMEOUT, (0x1a4), a reset will occur. This feature allows a host to initialise the system to a known state. Also, WT41u can emit a break character that may be used to wake the host.

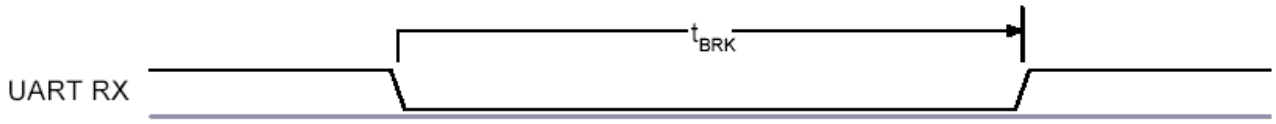

Figure 10: Break Signal

Table 17 shows a list of commonly used data rates and their associated values for PSKEY_UART_BAUD_RATE (0x204). There is no requirement to use these standard values. Any data rate within the supported range can be set in the PS Key according to the formula in Equation 1.

$$\text{Data Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 1: Data Rate

Data rate [bits/s]	Persistent store value (Hex)	Error [bits/s]	Error [%]
1200	0x0005	5	1.73
2400	0x000A	10	1.73
4800	0x0014	20	1.73
9600	0x0027	39	-0.82
19200	0x004F	79	0.45
38400	0x009D	157	-0.18
57600	0x00EC	236	0.03
76800	0x013B	315	0.14
115200	0x01D8	472	0.03
230400	0x03B0	944	0.03
460800	0x075F	1887	-0.02
921600	0x0EBF	3775	0
1382400	0x161E	5662	-0.01
1843200	0x1D7E	7550	0
2764800	0x2C3D	11325	0

Table 13: Standard Data Rates

6.1 UART Bypass

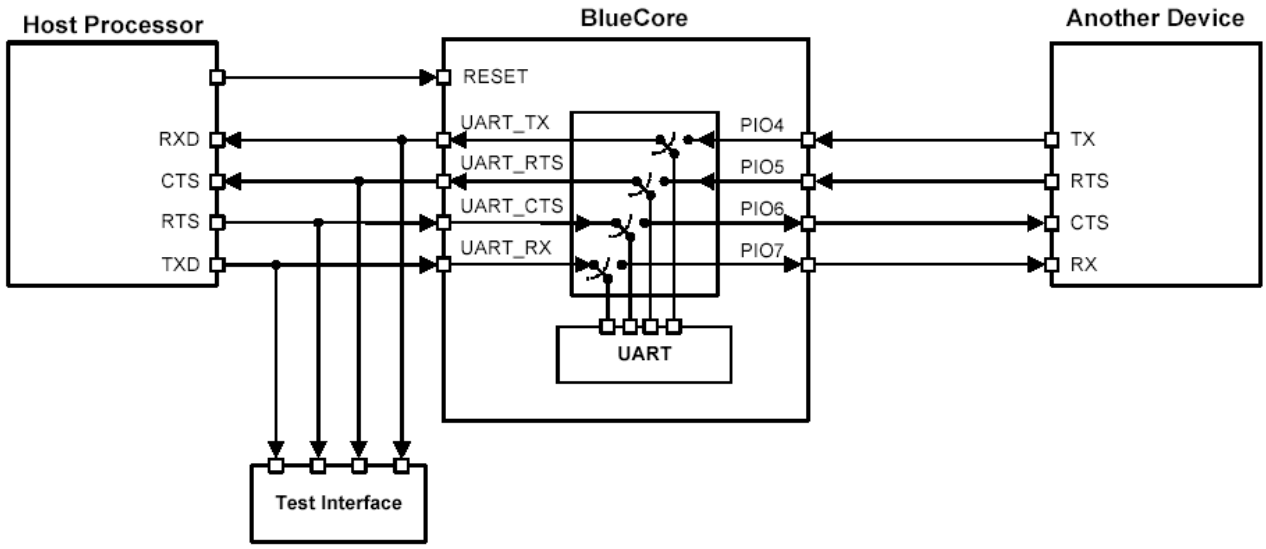

Figure 11: UART Bypass Architecture

6.2 UART Configuration While Reset is Active

The UART interface for WT41u while the chip is being held in reset is tristate. This will allow the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tristate when WT41u reset is de-asserted and the firmware begins to run.

6.3 UART Bypass Mode

Alternatively, for devices that do not tristate the UART bus, the UART bypass mode on the chipset can be used. The default state of the chipset after reset is de-asserted; this is for the host UART bus to be connected to the chipset UART, thereby allowing communication to the chipset via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD.

In order to apply the UART bypass mode, a BCCMD command will be issued to the chipset. Upon this issue, it will switch the bypass to PIO[7:4] as Figure 11 indicates. Once the bypass mode has been invoked, WT41u will enter the Deep Sleep state indefinitely.

In order to re-establish communication with WT41u, the chip must be reset so that the default configuration takes effect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore, it is not possible to have active Bluetooth links while operating the bypass mode.

The current consumption for a device in UART bypass mode is equal to the values quoted for a device in standby mode.

7 USB Interface

This is a full speed (12Mbits/s) USB interface for communicating with other compatible digital devices. WT41u acts as a USB peripheral, responding to requests from a master host controller such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth v2.1 + EDR specification or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

As USB is a master/slave oriented system (in common with other USB peripherals), WT41u only supports USB Slave operation.

7.1 USB Data Connections

The USB data lines emerge as pins USB_DP and USB_DN. These terminals are connected to the internal USB I/O buffers of the the chipset, therefore, have a low output impedance. To match the connection to the characteristic impedance of the USB cable, resistors must be placed in series with USB_DP/USB_DN and the cable.

7.2 USB Pull-Up resistor

WT41u features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when WT41u is ready to enumerate. It signals to the PC that it is a full speed (12Mbits/s) USB device.

The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ 5% pull-down resistor (in the hub/host) when VDD_PADS = 3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and D+ on the USB cable. The firmware must be alerted to which mode is used by setting PSKEY_USB_PIO_PULLUP appropriately. The default setting uses the internal pull-up resistor.

7.3 USB Power Supply

The USB specification dictates that the minimum output high voltage for USB data lines is 2.8V. To safely meet the USB specification, the voltage on the VDD supply terminal must be an absolute minimum of 3.1V. Silicon Labs recommends 3.3V for optimal USB signal quality.

7.4 Self-Powered Mode

In self-powered mode, the circuit is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to WT41u via a resistor network (R_{vb1} and R_{vb2}), so WT41u can detect when VBUS is powered up. The chipset will not pull USB_DP high when VBUS is off.

Self-powered USB designs (powered from a battery or PSU) must ensure that a PIO line is allocated for USB pullup purposes. A 1.5kΩ 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The internal pull-up in the chipset is only suitable for bus-powered USB devices, e.g., dongles.

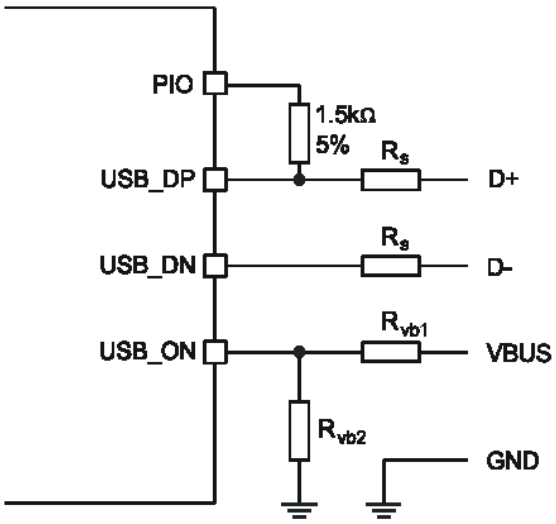

Figure 12: USB Connections for Self-Powered Mode

The terminal marked USB_ON can be any free PIO pin. The PIO pin selected must be registered by setting PSKEY_USB_PIO_VBUS to the corresponding pin number.

Identifier	Value	Function
R_s	27Ω nominal	Impedance matching to USB cable
R_{vb1}	22kΩ 5%	VBUS ON sense divider
R_{vb2}	47kΩ 5%	VBUS ON sense divider

Figure 13: USB Interface Component Values

7.5 Bus-Powered Mode

In bus-powered mode, the application circuit draws its current from the 5V VBUS supply on the USB cable. WT41u negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume. On power-up the device must not draw more than 100 mA but after being configured it can draw up to 500 mA.

For WT41u, the USB power descriptor should be altered to reflect the amount of power required. This is accomplished by setting PSKEY_USB_MAX_POWER (0x2c6). This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA. By default for WT41u the setting is 300 mA.

When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification. See the USB Specification. Some applications may require soft start circuitry to limit inrush current if more than 10uF is present between VBUS and GND. The 5V VBUS line emerging from a PC is often electrically noisy. As well as regulation down to 3.3V and 1.8V, applications should include careful filtering of the 5V line to attenuate noise that is above the voltage regulator bandwidth. Excessive noise on WT41u supply pins will result in reduced receiver sensitivity and a distorted RF transmit signal.

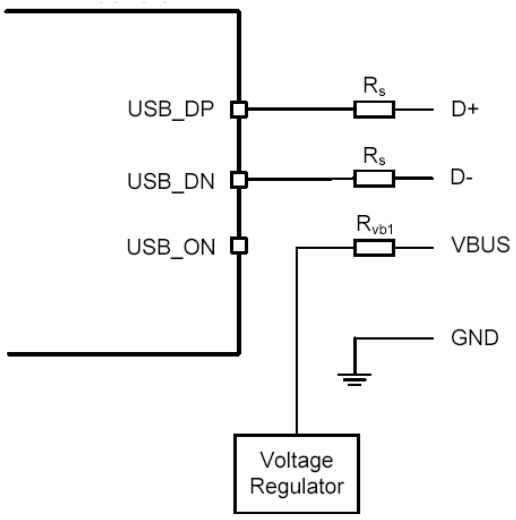

Figure 14: USB Connections for Bus-Powered Mode

7.6 USB Suspend Current

All USB devices must permit the USB controller to place them in a USB suspend mode. While in USB Suspend, bus-powered devices must not draw more than 2.5mA from USB VBUS (self-powered devices may draw more than 2.5mA from their own supply). This current draw requirement prevents operation of the radio by bus-powered devices during USB Suspend.

When computing suspend current, the current from VBUS through the bus pull-up and pull-down resistors must be included. The pull-up resistor at the device is 1.5 kΩ. (nominal). The pull-down resistor at the hub is 14.25kΩ. to 24.80kΩ. The pull-up voltage is nominally 3.3V, which means that holding one of the signal lines high takes approximately 200uA, leaving only 2.3mA available from a 2.5mA budget. Ensure that external LEDs and/or amplifiers can be turned off by the chipset. The entire circuit must be able to enter the suspend mode.

7.7 USB Detach and Wake-Up Signaling

WT41u can provide out-of-band signaling to a host controller by using the control lines called USB_DETACH and USB_WAKE_UP. These are outside the USB specification (no wires exist for them inside the USB cable), but can be useful when embedding WT41u into a circuit where no external USB is visible to the user. Both control lines are shared with PIO pins and can be assigned to any PIO pin by setting PSKEY_USB_PIO_DETACH and PSKEY_USB_PIO_WAKEUP to the selected PIO number.

USB_DETACH is an input which, when asserted high, causes WT41u to put USB_DN and USB_DP in high impedance state and turns off the pull-up resistor on DP. This detaches the device from the bus and is logically equivalent to unplugging the device. When USB_DETACH is taken low, WT41u will connect back to USB and await enumeration by the USB host.

USB_WAKE_UP is an active high output (used only when USB_DETACH is active) to wake up the host and allow USB communication to recommence. It replaces the function of the software USB WAKE_UP message (which runs over the USB cable) and cannot be sent while the chipset is effectively disconnected from the bus.