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FEATURES

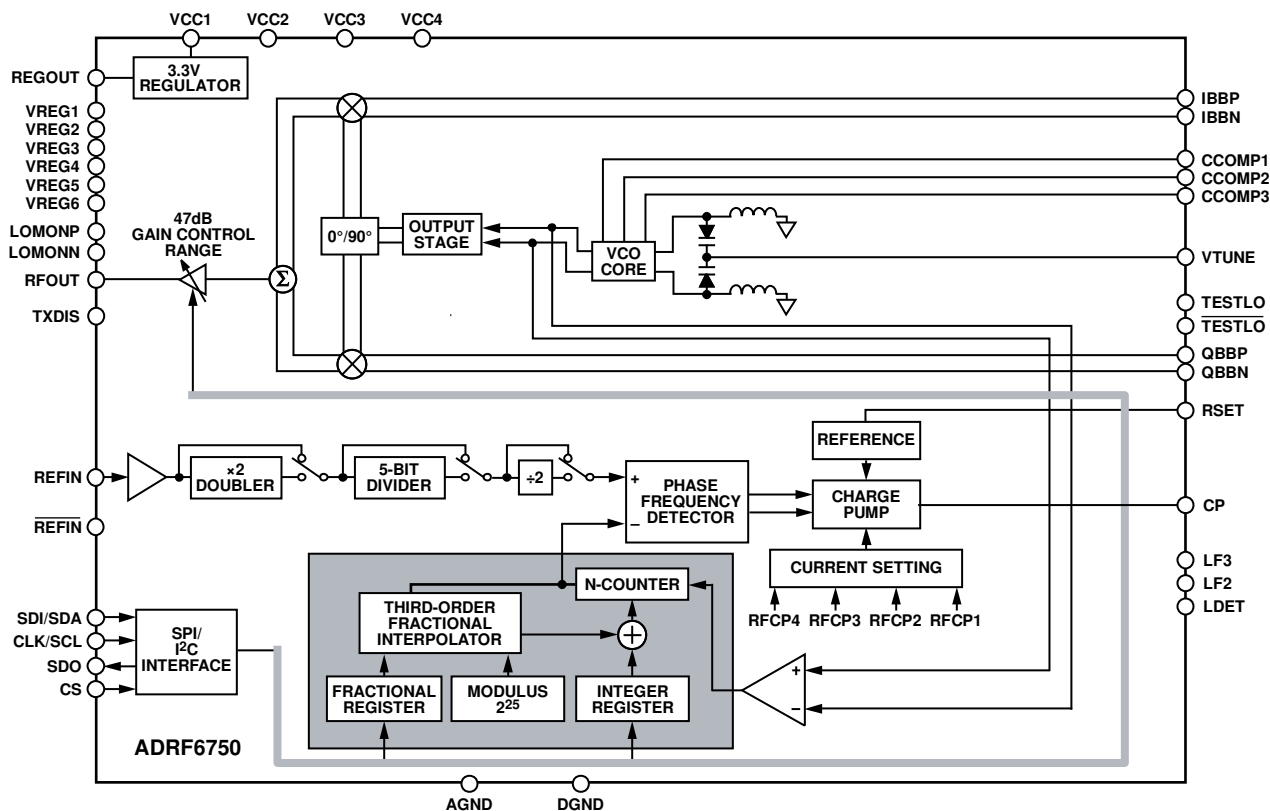
I/Q modulator with integrated fractional-N PLL and VCO
Gain control span: 47 dB in 1 dB steps
Output frequency range: 950 MHz to 1575 MHz
Output 1 dB compression: 8.5 dBm
Output IP3: 23 dBm
Noise floor: -162 dBm/Hz
Baseband modulation bandwidth: 250 MHz (1 dB)
Output frequency resolution: 1 Hz
Functions with external VCO for extended frequency range
SPI and I²C-compatible serial interfaces
Power supply: 5 V/310 mA

GENERAL DESCRIPTION

The ADRF6750 is a highly integrated quadrature modulator, frequency synthesizer, and programmable attenuator. The device covers an operating frequency range from 950 MHz to 1575 MHz for use in satellite, cellular and broadband communications.

The ADRF6750 modulator includes a high modulus fractional-N frequency synthesizer with integrated VCO, providing better than 1 Hz frequency resolution, and a 47 dB digitally controlled output attenuator with 1 dB steps.

Control of all the on-chip registers is through a user-selected SPI interface or I²C interface. The device operates from a single power supply ranging from 4.75 V to 5.25 V.

FUNCTIONAL BLOCK DIAGRAM*Figure 1.***Rev. A**

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ADRF6750* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADRF6750 Evaluation Board

DOCUMENTATION

Data Sheet

- ADRF6750: 950 MHz to 1575 MHz Quadrature Modulator with Integrated Fractional-N PLL and VCO Data Sheet

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- ADRF6750 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADRF6750 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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TABLE OF CONTENTS

Features	1	I ² C Interface	21
General Description	1	SPI Interface	23
Functional Block Diagram	1	Program Modes	25
Revision History	2	Register Map	27
Specifications.....	3	Register Map Summary	27
Timing Characteristics	5	Register Bit Descriptions.....	28
Absolute Maximum Ratings.....	7	Suggested Power-Up Sequence.....	31
ESD Caution.....	7	Initial Register Write Sequence	31
Pin Configuration and Function Descriptions.....	8	Evaluation Board	32
Typical Performance Characteristics	10	General Description.....	32
Theory of Operation	18	Hardware Description	32
Overview.....	18	PCB Artwork.....	35
PLL Synthesizer and VCO.....	18	Bill of Materials.....	38
Quadrature Modulator	20	Outline Dimensions	39
Attenuator.....	21	Ordering Guide	39
Voltage Regulator	21		
EXTERNAL vco OPERATION	21		

REVISION HISTORY

4/10—Rev. 0 to Rev. A

Changes to Table 5.....	9
Changes to LOMON Outputs Section.....	33
Changes to Ordering Guide	39

1/10—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, I/Q inputs = 0.9 V p-p differential sine waves in quadrature on a 500 mV dc bias, baseband frequency = 1 MHz, REFIN = 10 MHz, PFD = 20 MHz, loop bandwidth = 50 kHz, and LOMONx is off, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF OUTPUT					
Operating Frequency Range	RFOUT pin	950		1575	MHz
Nominal Output Power	$V_{IQ} = 0.9\text{ V}$ p-p differential		-1.6		dBm
Gain Flatness	Any 40 MHz		± 0.5		dB
Output P1dB			8.5		dBm
Output IP3	$f_{1BB} = 3.5\text{ MHz}$, $f_{2BB} = 4.5\text{ MHz}$, $P_{OUT} = -6\text{ dBm}$ per tone		23		dBm
Output Return Loss	Attenuator setting = 0 dB		-12		dB
LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		-45		dBc
2× LO Carrier Feedthrough	Attenuator setting = 0 dB to 47 dB		-45		dBm
Sideband Suppression			-45		dBc
Noise Floor	I/Q inputs = 0 V p-p differential, Attenuator setting = 0 dB		-162		dBm/Hz
	Attenuator setting = 0 dB to 21 dB, carrier offset = 15 MHz		-147		dBc/Hz
	Attenuator setting = 21 dB to 47 dB, carrier offset = 15 MHz		-170		dBm/Hz
Harmonics			-60		dBc
REFERENCE CHARACTERISTICS					
Input Frequency	REFIN pin				
	With R/2 divider enabled	10		300	MHz
	With R/2 divider disabled	10		165	MHz
Input Sensitivity	AC-coupled	0.4		VREG	V p-p
Input Capacitance				10	pF
Input Current				± 100	μA
CHARGE PUMP					
I_{CP} Sink/Source	Programmable				
High Value	With RSET = 4.7 k Ω		5		mA
Low Value			312.5		μA
Absolute Accuracy	With RSET = 4.7 k Ω		4.0		%
RSET Value			4.7		k Ω
VCO Gain	K_{VCO}		25		MHz/V
SYNTHESIZER SPECIFICATIONS					
Frequency Resolution				1	Hz
Spurs	Integer boundary < loop bandwidth		-55		dBc
	>10 MHz offset from carrier		-85		dBc
Phase Noise ¹	Frequency = 950 MHz to 1575 MHz				
	100 Hz offset		-80		dBc/Hz
	1 kHz offset		-88		dBc/Hz
	10 kHz offset		-93		dBc/Hz
	100 kHz offset		-107		dBc/Hz
	1 MHz offset		-133		dBc/Hz
	>15 MHz offset		-152		dBc/Hz
Integrated Phase Noise ¹	1 kHz to 8 MHz integration bandwidth		0.4		$^\circ\text{rms}$
Frequency Settling ¹	Maximum frequency error = 100 Hz		170		μs
Maximum Frequency Step for No Autocalibration	Frequency step with no autocalibration routine; Register CR24, Bit 0 = 1			100	kHz
Phase Detector Frequency		10		30	MHz

ADRF6750

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN CONTROL					
Gain Range			47		dB
Step Size			1		dB
Relative Step Accuracy	Fixed frequency, adjacent steps				
	All attenuation steps		±0.3		dB
	Over full frequency range, adjacent steps		±1.5		dB
Absolute Step Accuracy ²	47 dB attenuation step		-2.0		dB
Output Settling Time	Any step; output power settled to ±0.2 dB		10		µs
OUTPUT DISABLE					
Off Isolation	TXDIS pin				
	RF OUT, attenuator setting = 0 dB to 47 dB, TXDIS high		-110		dBm
	LO, Attenuator setting = 0 dB to 47 dB, TXDIS high		-90		dBm
	2 x LO, Attenuator setting = 0 dB to 47 dB, TXDIS high		-50		dBm
Turn-On Settling Time	TXDIS high to low (90% of envelope)		180		ns
Turn-Off Settling Time	TXDIS low to high (to -55 dBm)		270		ns
MONITOR OUTPUT					
Nominal Output Power	LOMONP, LOMONN pins		-24		dBm
BASEBAND INPUTS					
I and Q Input Bias Level	IBBP, IBBN, QBBP, QBBN pins		500		mV
1 dB Bandwidth			250		MHz
LOGIC INPUTS					
Input High Voltage, V _{INH}	CS, TXDIS pins	1.4			V
Input Low Voltage, V _{INL}	CS, TXDIS pins			0.6	V
Input High Voltage, V _{INH}	SDI/SDA, CLK/SCL pins	2.1			V
Input Low Voltage, V _{INL}	SDI/SDA, CLK/SCL pins			1.1	V
Input Current, I _{INH} /I _{INL}	CS, TXDIS, SDI/SDA, CLK/SCL pins			±1	µA
Input Capacitance, C _{IN}	CS, TXDIS, SDI/SDA, CLK/SCL pins			10	pF
LOGIC OUTPUTS					
Output High Voltage, V _{OH}	SDO, LDET pins; I _{OH} = 500 µA	2.8			V
Output Low Voltage, V _{OL}	SDO, LDET pins; I _{OL} = 500 µA			0.4	V
	SDA (SDI/SDA); I _{OL} = 3 mA			0.4	V
POWER SUPPLIES					
VCC1, VCC2, VCC3, VCC4, VREG1, VREG2, VREG3, VREG4, VREG5, VREG6, and REGOUT pins REGOUT normally connected to VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6					
Voltage Range	VCC1, VCC2, VCC3, and VCC4	4.75	5	5.25	V
	REGOUT, VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6		3.3		V
Supply Current	VCC1, VCC2, VCC3, and VCC4 combined; REGOUT connected to VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6		310	340	mA
Operating Temperature		-40		+85	°C

¹ LBW = 50 kHz at LO = 1200 MHz; I_{CP} = 2.5 mA.

² All other attenuation steps have an absolute error of <±2.0 dB.

TIMING CHARACTERISTICS

I²C Interface Timing

Table 2.

Parameter ¹	Symbol	Limit	Unit
SCL Clock Frequency	f_{SCL}	400	kHz max
SCL Pulse Width High	t_{HIGH}	600	ns min
SCL Pulse Width Low	t_{LOW}	1300	ns min
Start Condition Hold Time	$t_{HD;STA}$	600	ns min
Start Condition Setup Time	$t_{SU;STA}$	600	ns min
Data Setup Time	$t_{SU;DAT}$	100	ns min
Data Hold Time	$t_{HD;DAT}$	300	ns min
Stop Condition Setup Time	$t_{SU;STO}$	600	ns min
Data Valid Time	$t_{VD;DAT}$	900	ns max
Data Valid Acknowledge Time	$t_{VD;ACK}$	900	ns max
Bus Free Time	t_{BUF}	1300	ns min

¹ See Figure 2.

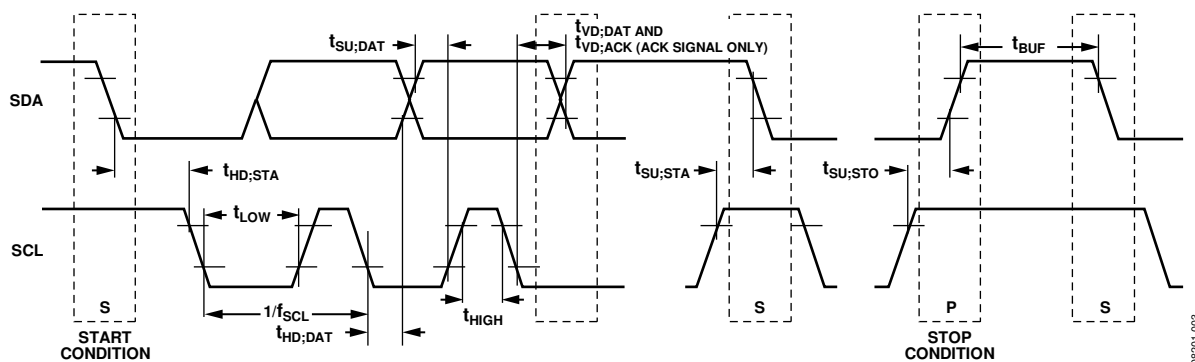


Figure 2. I²C Port Timing Diagram

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ADRF6750

SPI Interface Timing

Table 3.

Parameter ¹	Symbol	Limit	Unit
CLK Frequency	f_{CLK}	20	MHz max
CLK Pulse Width High	t_1	15	ns min
CLK Pulse Width Low	t_2	15	ns min
Start Condition Hold Time	t_3	5	ns min
Data Setup Time	t_4	10	ns min
Data Hold Time	t_5	5	ns min
Stop Condition Setup Time	t_6	5	ns min
SDO Access Time	t_7	15	ns min
CS to SDO High Impedance	t_8	25	ns max

¹ See Figure 3.

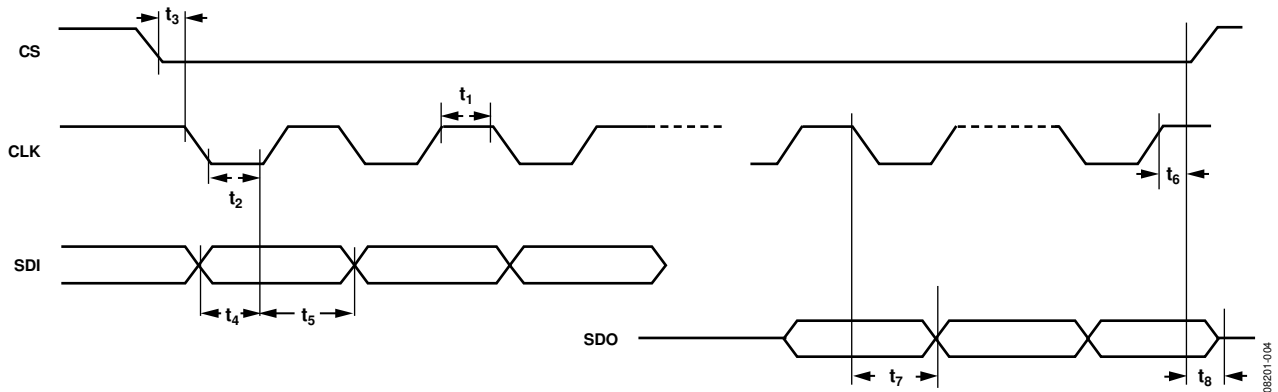


Figure 3. SPI Port Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage VCC1, VCC2, VCC3, and VCC4	-0.3 V to +6 V
Supply Voltage VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6	-0.3 V to +4 V
IBBP, IBBN, QBBP, and QBBN	0 V to 2.5 V
Digital I/O	-0.3 V to +4 V
Analog I/O (Other Than IBBP, IBBN, QBBP, and QBBN)	-0.3 V to +4 V
TESTLO, $\overline{\text{TESTLO}}$ Difference	1.5 V
θ_{JA} (Exposed Paddle Soldered Down)	26°C/W
Maximum Junction Temperature	120°C
Storage Temperature Range	-65°C to +150°C

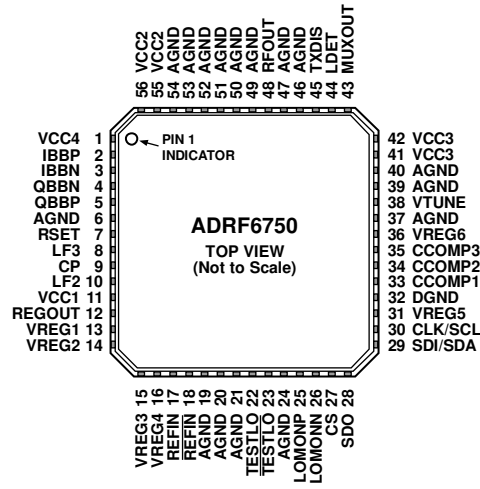
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. CONNECT EXPOSED PAD TO GROUND PLANE VIA A LOW IMPEDANCE PATH.

08201-005

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
11, 55, 56, 41, 42, 1	VCC1 to VCC4	Positive Power Supplies for I/Q Modulator. Apply a 5 V power supply to VCC1, which should be decoupled with power supply decoupling capacitors. Connect VCC2, VCC3, and VCC4 to the same 5 V power supply.
12	REGOUT	3.3 V Output Supply. Drives VREG1, VREG2, VREG3, VREG4, VREG5, and VREG6.
13, 14, 15, 16, 31, 36	VREG1 to VREG6	Positive Power Supplies for PLL Synthesizer, VCO, and Serial Port. Connect these pins to REGOUT (3.3 V) and decouple them separately.
6, 19, 20, 21, 24, 37, 39, 40, 46, 47, 49, 50, 51, 52, 53, 54	AGND	Analog Ground. Connect to a low impedance ground plane.
32	DGND	Digital Ground. Connect to the same low impedance ground plane as the AGND pins.
2, 3	IBBP, IBBN	Differential In-Phase Baseband Inputs. These high impedance inputs must be dc-biased to approximately 500 mV dc and should be driven from a low impedance source. Nominal characterized ac signal swing is 450 mV p-p on each pin. This results in a differential drive of 0.9 V p-p with a 500 mV dc bias, resulting in a single sideband output power of approximately -1.6 dBm. These inputs are not self-biased and must be externally biased.
4, 5	QBBN, QBBP	Differential Quadrature Baseband Inputs. These high impedance inputs must be dc-biased to approximately 500 mV dc and should be driven from a low impedance source. Nominal characterized ac signal swing is 450 mV p-p on each pin. This results in a differential drive of 0.9 V p-p with a 500 mV dc bias, resulting in a single sideband output power of approximately -1.6 dBm. These inputs are not self-biased and must be externally biased.
33, 34, 35	CCOMP1 to CCOMP3	Internal Compensation Nodes. These pins must be decoupled to ground with a 100 nF capacitor.
38	VTUNE	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP output voltage.
7	RSET	Charge Pump Current Set. Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is as follows: $I_{CPmax} = \frac{23.5}{R_{SET}}$
9	CP	Charge Pump Output. When enabled, this output provides $\pm I_{CP}$ to the external loop filter, which, in turn, drives the internal VCO. where $R_{SET} = 4.7 \text{ k}\Omega$ and $I_{CPmax} = 5 \text{ mA}$.

Pin No.	Mnemonic	Description
27	CS	Chip Select, CMOS Input. When CS is high, the data stored in the shift registers is loaded into one of 31 latches. In I ² C mode, when CS is high, the slave address of the device is 0x60, and when CS is low, the slave address is 0x40.
29	SDI/SDA	Serial Data Input for SPI Port/Serial Data Input/Output for I ² C Port. In SPI mode, this pin is a high impedance CMOS data input, and data is loaded in an 8-bit word. In I ² C mode, this pin is a bidirectional port.
30	CLK/SCL	Serial Clock Input for SPI/I ² C Port. This serial clock is used to clock in the serial data to the registers. This input is a high impedance CMOS input.
28	SDO	Serial Data Output for SPI Port. Register states can be read back on the SDO data output line.
17	REFIN	Reference Input. This high impedance CMOS input should be ac-coupled.
18	$\overline{\text{REFIN}}$	Reference Input Bar. This pin should be either grounded or ac-coupled to ground.
48	RFOUT	RF Output. Single-ended, 50 Ω , internally biased RF output. This pin must be ac-coupled to the load. Nominal output power is -1.6 dBm for a single sideband baseband drive of 0.9 V p-p differential on the I and Q inputs (attenuation = minimum).
45	TXDIS	Output Disable. This pin can be used to disable the RF output. Connect to high logic level to disable the output. Connect to low logic level for normal operation.
25, 26	LOMONP, LOMONN	Differential Monitor Outputs. These pins provide a replica of the internal local oscillator frequency (1 \times LO) at four different power levels: -6 dBm, -12 dBm, -18 dBm, and -24 dBm, approximately. These open-collector outputs must be terminated with external resistors to REGOUT. These outputs can be disabled through serial port programming and should be tied to REGOUT if not used.
22, 23	$\overline{\text{TESTLO}}$, $\overline{\text{TESTLO}}$	Differential Test Inputs. These inputs provide an option for an external 2 \times LO to drive the modulator. This option can be selected by serial port programming. These inputs must be externally dc-biased and should be grounded if not used.
10, 8	LF2, LF3	No connect pins.
44	LDET	Lock Detect. This output pin indicates the state of the PLL: a high level indicates a locked condition, whereas a low level indicates a loss of lock condition.
43	MUXOUT	Muxout. This output is a test output for diagnostic use only. It should be left unconnected by the customer.
Exposed Paddle	EP	Exposed Paddle. Connect to ground plane via a low impedance path.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, I/Q inputs = 0.9 V p-p differential sine waves in quadrature on a 500 mV dc bias, REFIN = 10 MHz, PFD = 20 MHz, baseband frequency = 1 MHz, LOMONx is off, unless otherwise noted. A nominal condition is defined as 25°C, 5.00 V, and worst-case frequency. A worst-case condition is defined as having the worst-case temperature, supply voltage, and frequency.

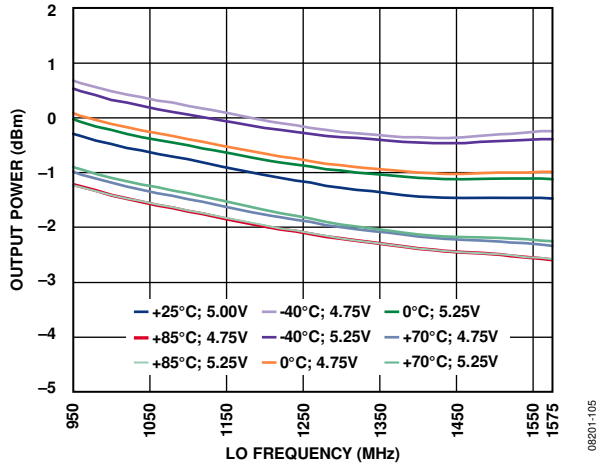


Figure 5. Output Power vs. LO Frequency, Supply, and Temperature

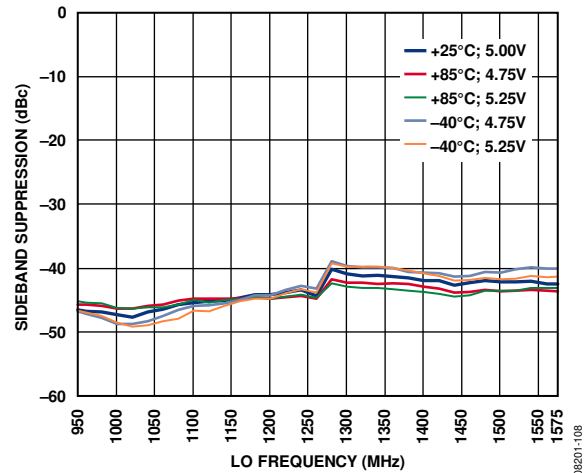


Figure 8. Sideband Suppression vs. LO Frequency, Supply, and Temperature

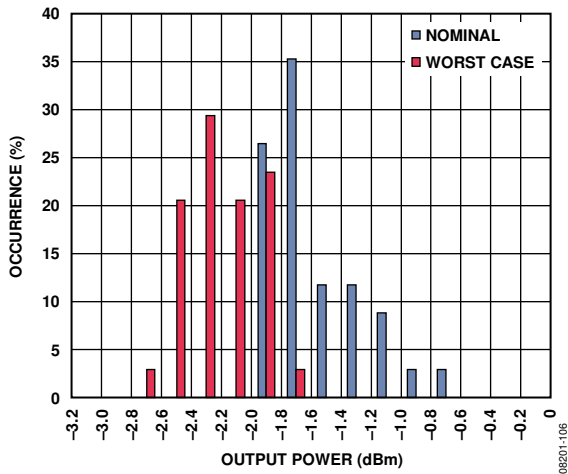


Figure 6. Output Power Distribution at Nominal and Worst-Case Conditions

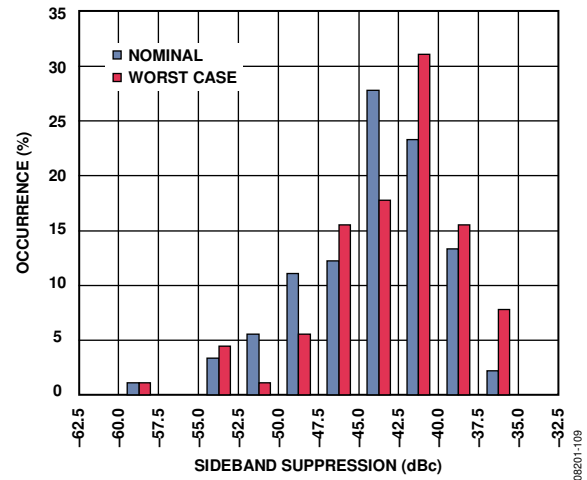


Figure 9. Sideband Suppression Distribution at Nominal and Worst-Case Conditions

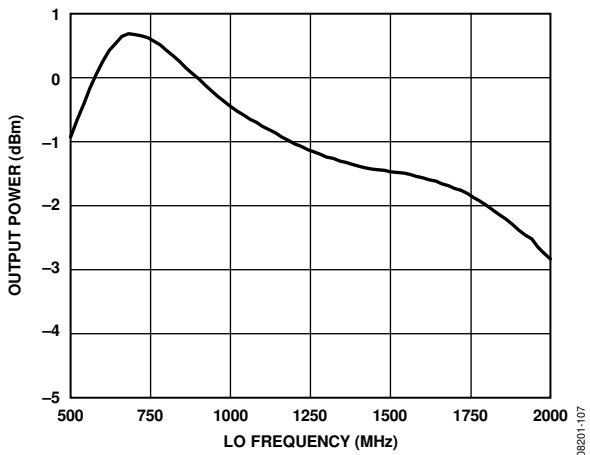


Figure 7. Output Power vs. LO Frequency for External VCO Mode at Nominal Conditions

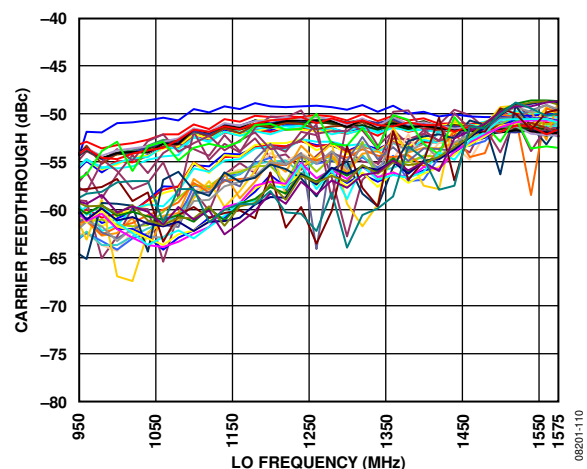


Figure 10. LO Carrier Feedthrough vs. Attenuation, LO Frequency, Supply, and Temperature

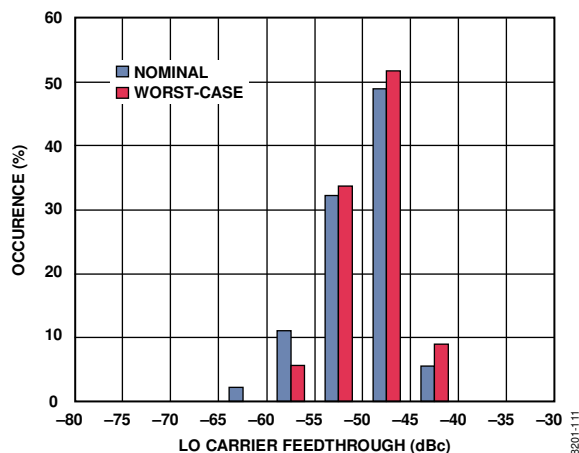


Figure 11. LO Carrier Feedthrough Distribution at Nominal and Worst-Case Conditions and Attenuation Setting

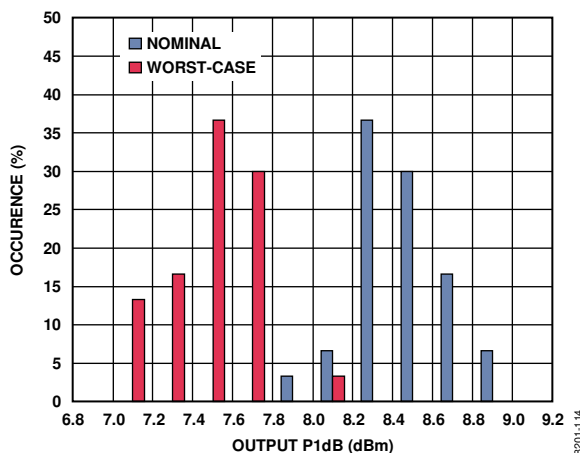


Figure 14. Output P1dB Compression Point Distribution at Nominal and Worst-Case Conditions

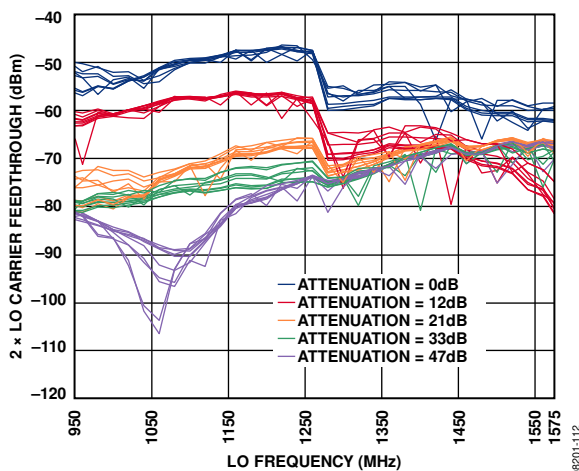


Figure 12. 2 x LO Carrier Feedthrough vs. Attenuation, LO Frequency, Supply, and Temperature

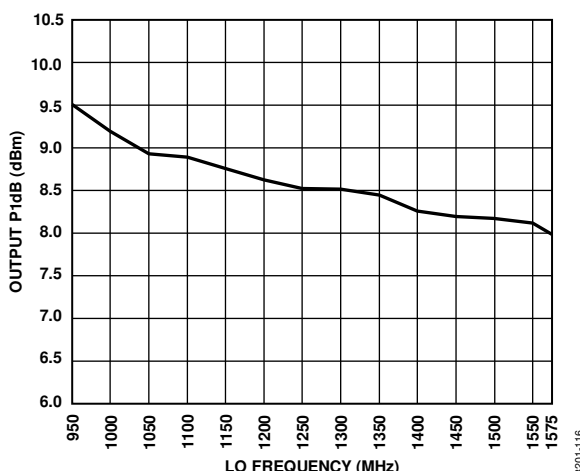


Figure 15. Output P1dB Compression Point vs. LO Frequency at Nominal Conditions

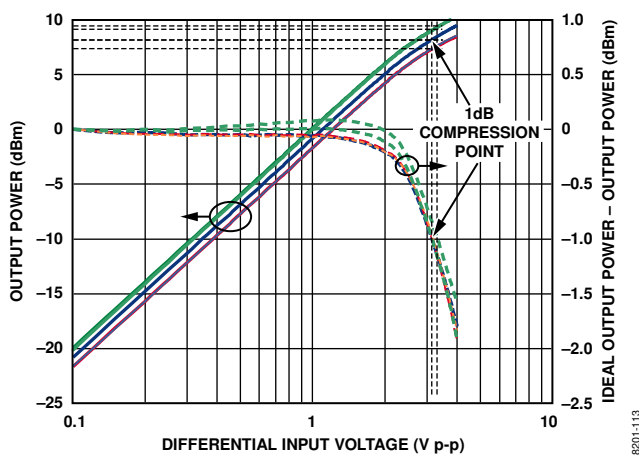


Figure 13. Output P1dB Compression Point at Worst-Case LO Frequency vs. Supply and Temperature

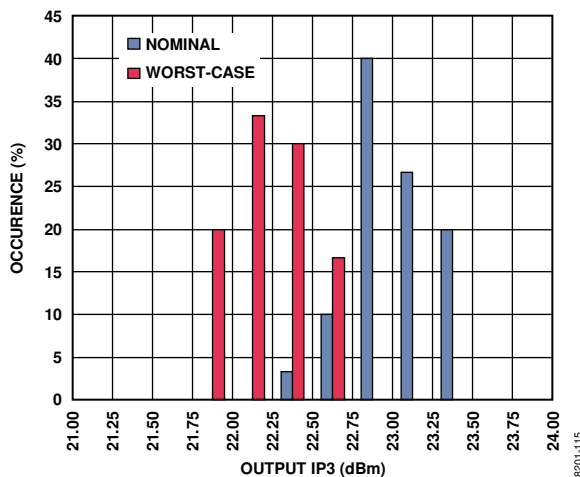


Figure 16. Output IP3 Distribution at Nominal and Worst-Case Conditions

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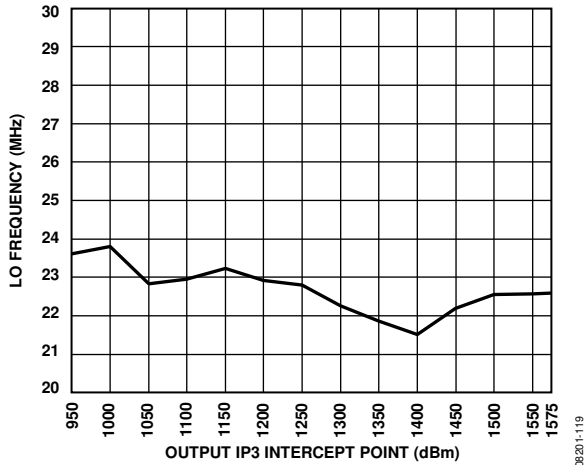


Figure 17. Output IP3 vs. LO Frequency at Nominal Conditions

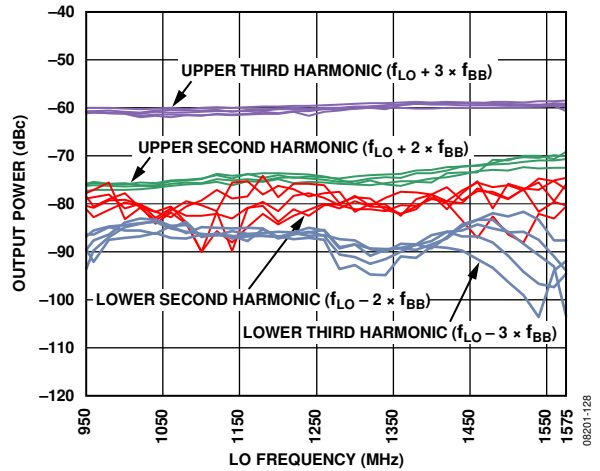


Figure 20. Second-Order and Third-Order Harmonic Distortion vs. LO Frequency, Supply, and Temperature

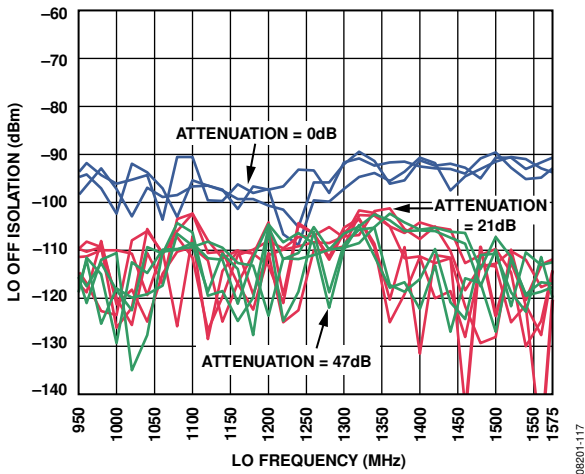


Figure 18. LO Off Isolation vs. Attenuation, LO Frequency, Supply, and Temperature

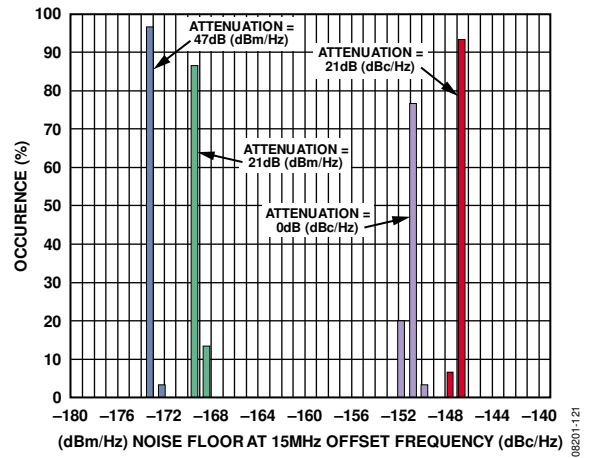


Figure 21. Noise Floor at 15 MHz Offset Frequency Distribution at Worst-Case Conditions and Different Attenuation Settings

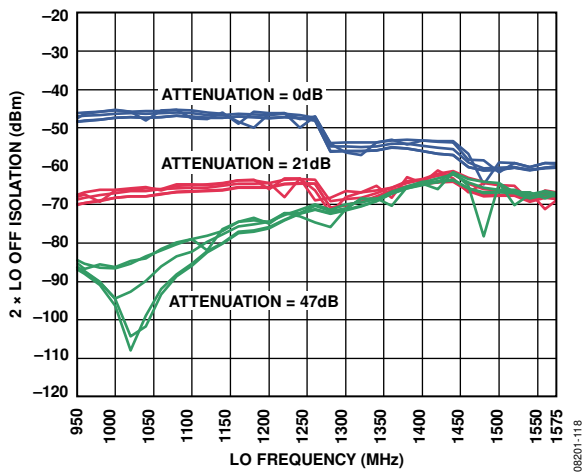


Figure 19. 2 x LO Off Isolation vs. Attenuation, LO Frequency, Supply, and Temperature

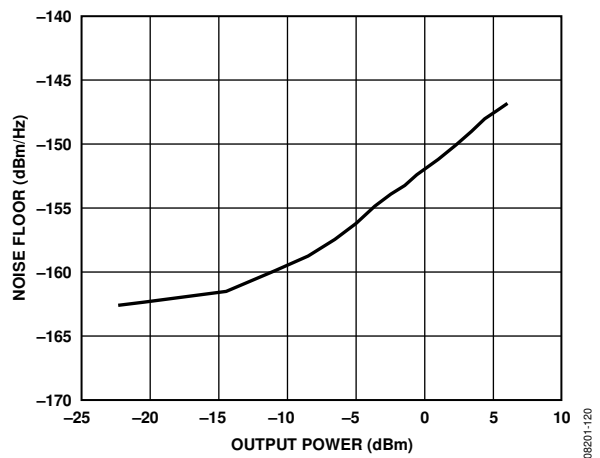


Figure 22. Noise Floor at 0 dB Attenuation vs. Output Power at Nominal Conditions

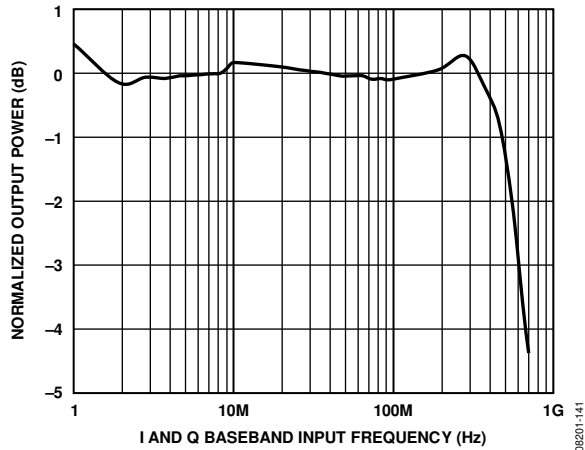


Figure 23. Normalized I and Q Input Bandwidth

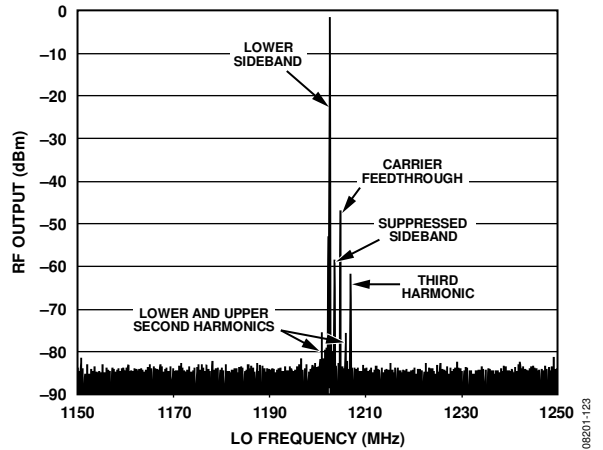


Figure 26. RF Output Spectral Plot over a 100 MHz Span

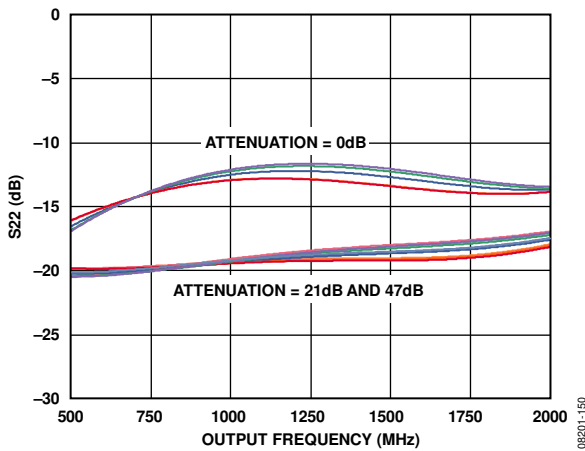


Figure 24. Output Return Loss at Worst-Case Attenuation vs. LO Frequency, Supply, and Temperature

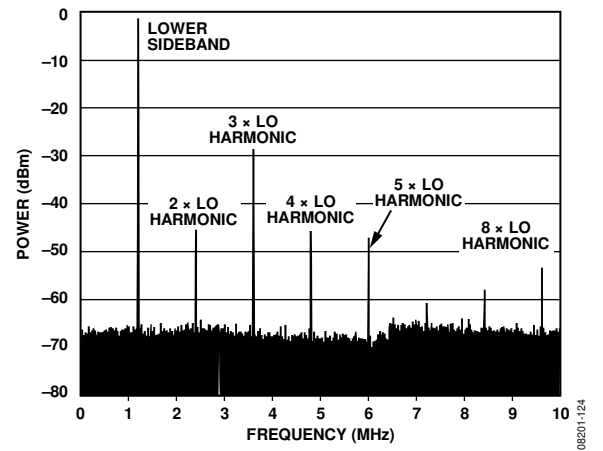


Figure 27. RF Output Spectral Plot over a Wide Span

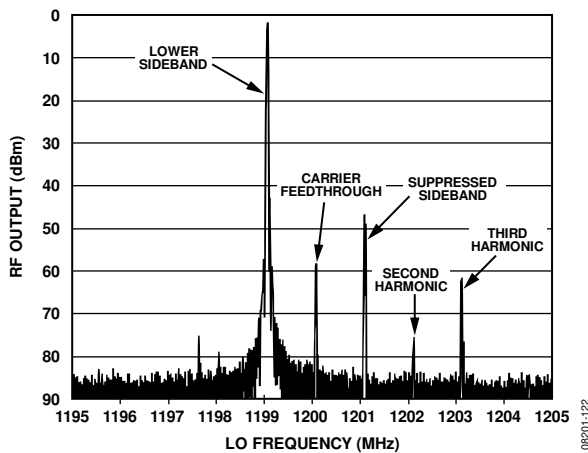


Figure 25. RF Output Spectral Plot over a 10 MHz Span

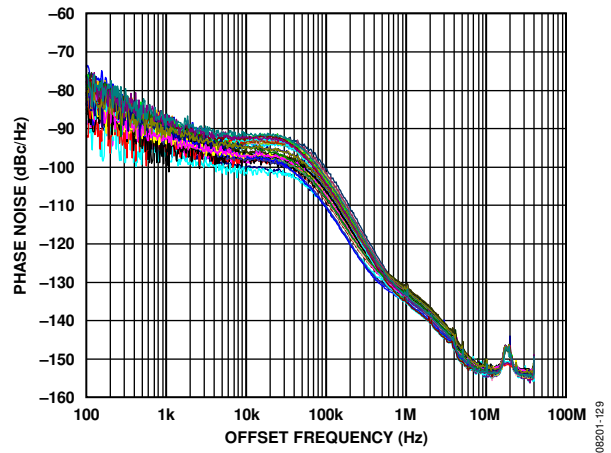


Figure 28. Phase Noise Performance vs. LO Frequency, Supply, and Temperature

ADRF6750

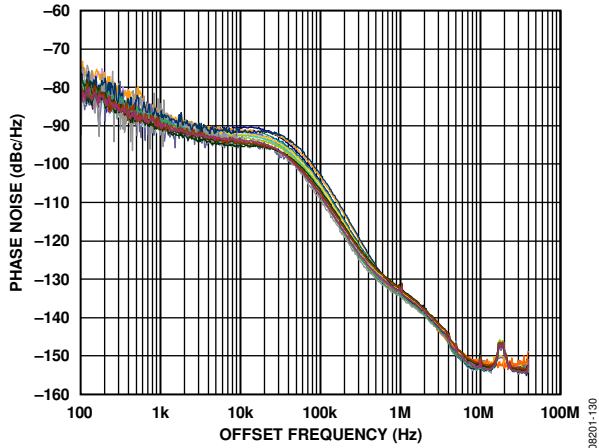


Figure 29. Phase Noise Performance Distribution at Worst-Case Conditions

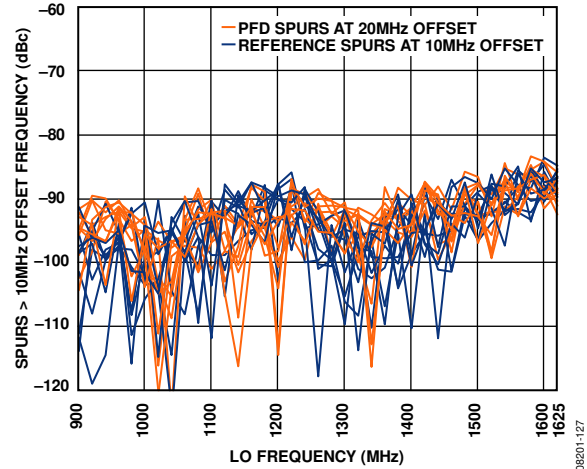


Figure 32. Spurs > 10 MHz from Carrier vs. LO Frequency, Supply, and Temperature

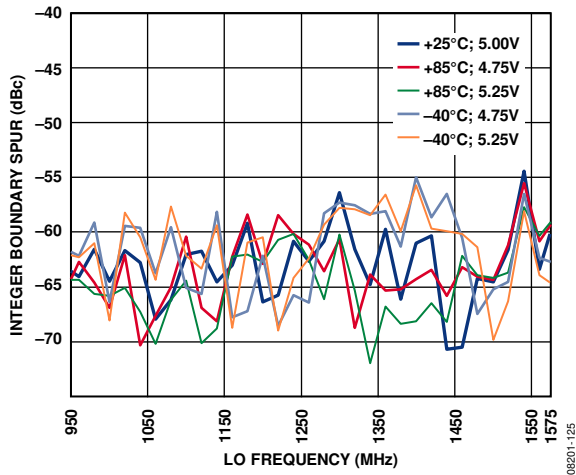


Figure 30. Integer Boundary Spur Performance vs. LO Frequency, Supply, and Temperature

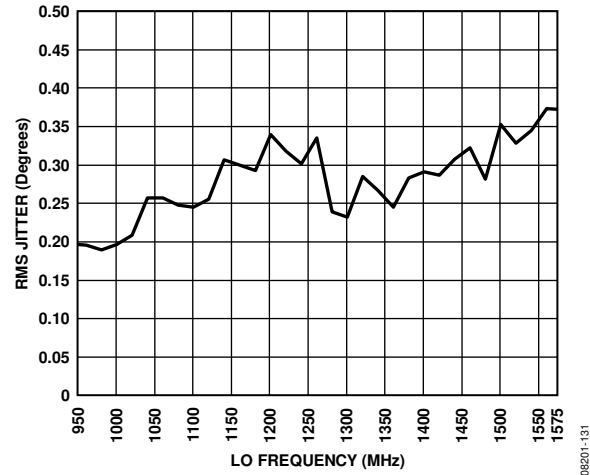


Figure 33. Integrated Phase Noise vs. LO Frequency at Nominal Conditions

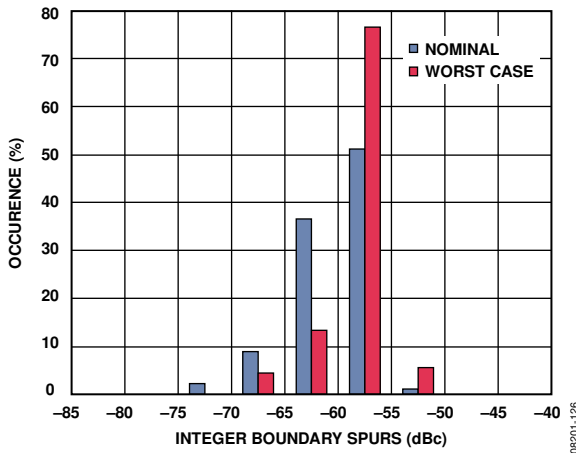


Figure 31. Integer Boundary Spur Distribution at Nominal and Worst-Case Conditions

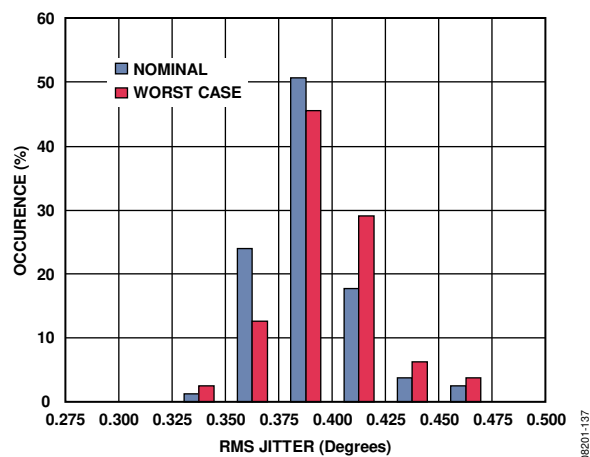


Figure 34. Integrated Phase Noise at Nominal and Worst-Case Conditions

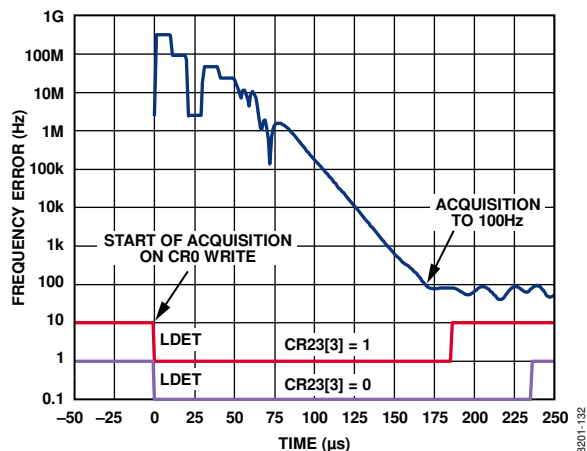


Figure 35. PLL Frequency Settling Time at Worst-Case Low Frequency with Lock Detect Shown

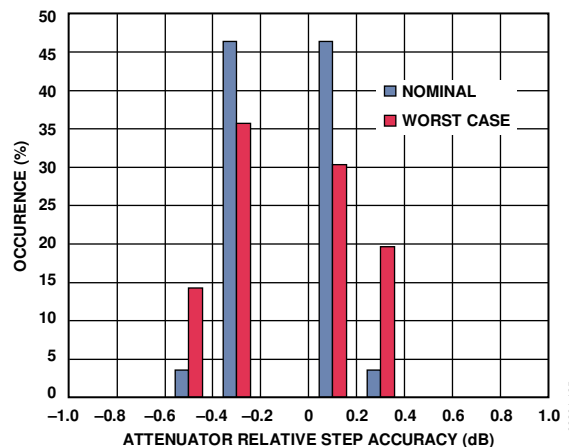


Figure 38. Attenuator Relative Step Accuracy Distribution at Nominal and Worst-Case Conditions

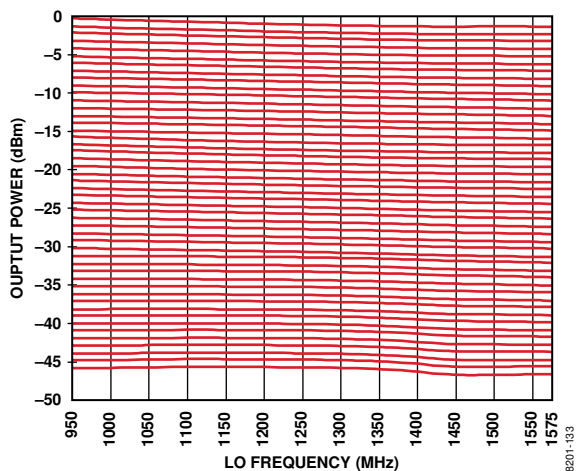


Figure 36. Attenuator Gain vs. LO Frequency by Gain Code, All Attenuator Code Steps

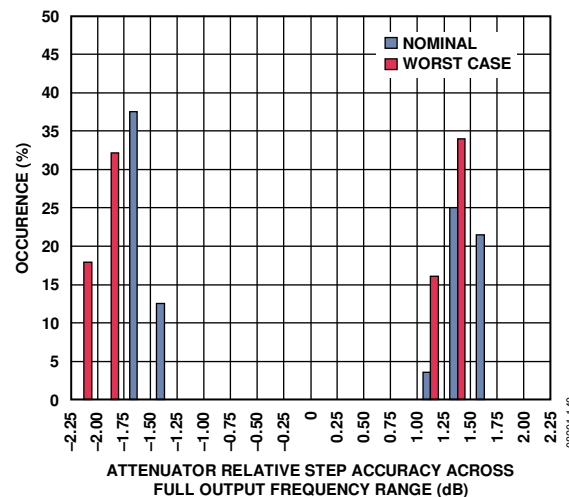


Figure 39. Attenuator Relative Step Accuracy Across Full Output Frequency Range Distribution at Nominal and Worst-Case Conditions

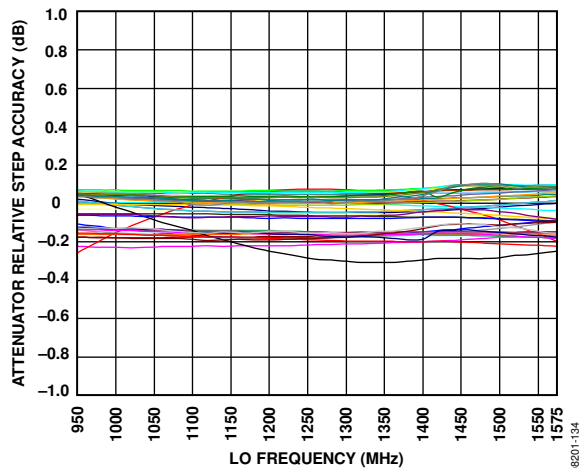


Figure 37. Attenuator Relative Step Accuracy over all Attenuation Steps vs. LO Frequency, Nominal Conditions

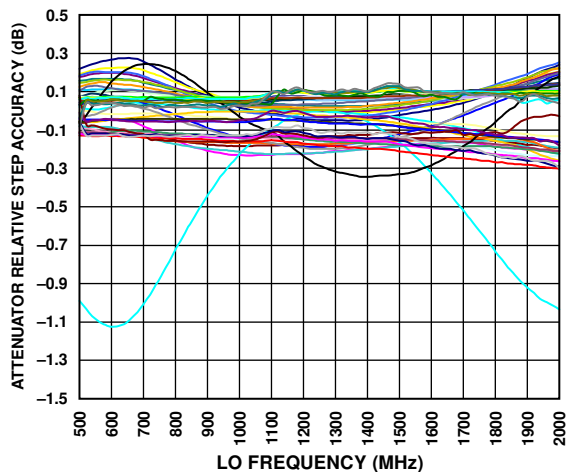


Figure 40. Attenuator Relative Step Accuracy over all Attenuation Steps vs. LO Frequency for External VCO Mode, Nominal Conditions

ADRF6750

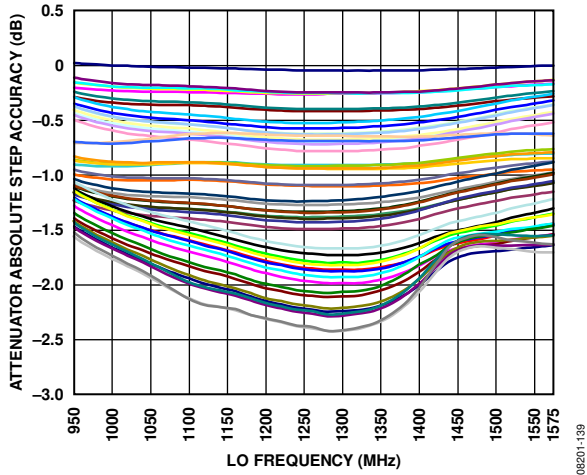


Figure 41. Attenuator Absolute Step Accuracy over all Attenuation Steps vs. LO Frequency, Nominal Conditions

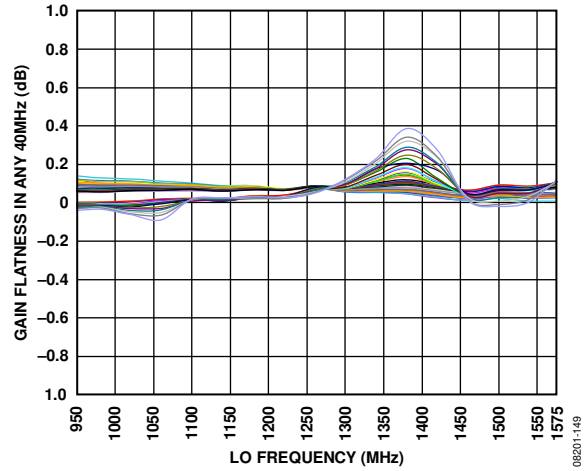


Figure 44. Gain Flatness in any 40 MHz for all Attenuation Steps vs. LO Frequency at Nominal Conditions

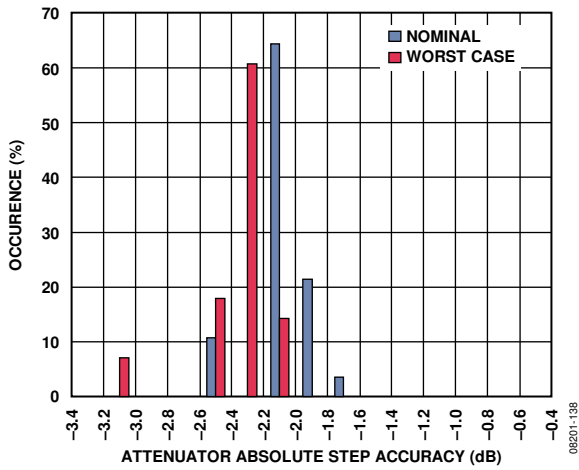


Figure 42. Attenuator Absolute Step Accuracy Distribution at Nominal and Worst-Case Conditions

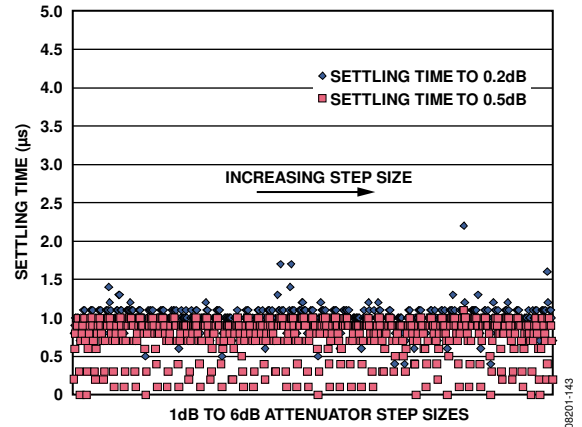


Figure 45. Attenuator Settling Time to 0.2 dB and 0.5 dB for Small Steps (1 dB to 6 dB) at Nominal Conditions

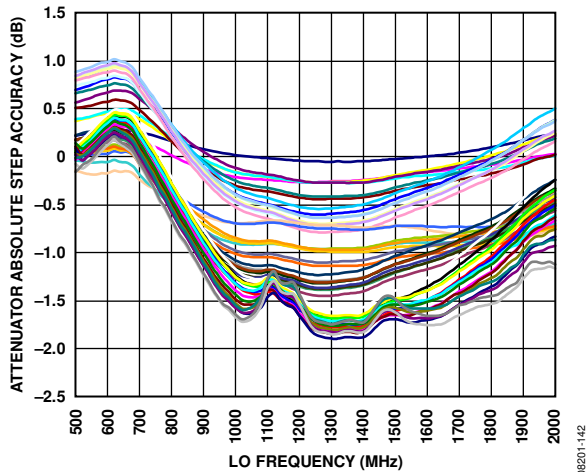


Figure 43. Attenuator Absolute Step Accuracy over all Attenuation Steps vs. LO Frequency for External VCO Mode, Nominal Conditions

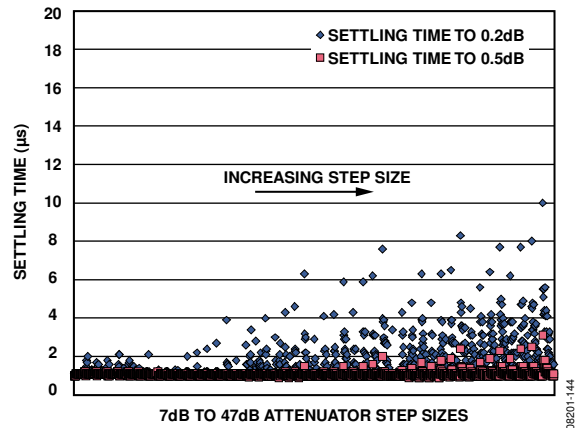


Figure 46. Attenuator Settling Time to 0.2 dB and 0.5 dB for Large Steps (7 dB to 47 dB) at Nominal Conditions

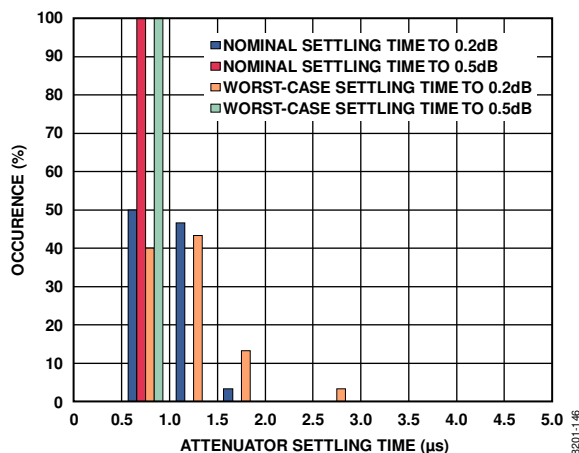


Figure 47. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Typical Small Step

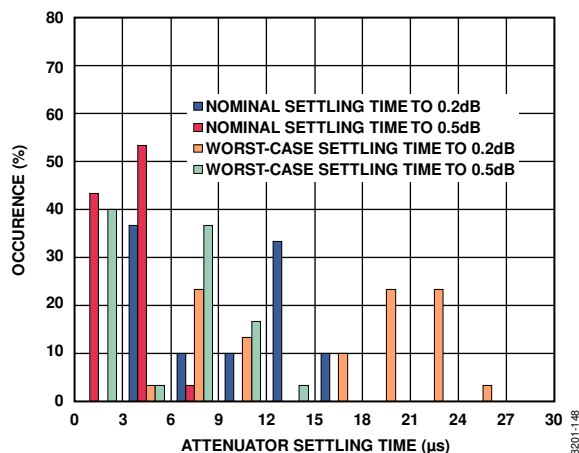


Figure 50. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Worst-Case Large Step (47 dB to 0 dB)

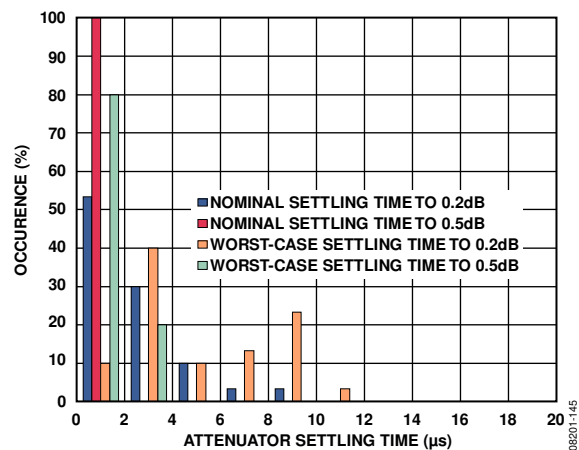


Figure 48. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Worst-Case Small Step (36 dB to 42 dB)

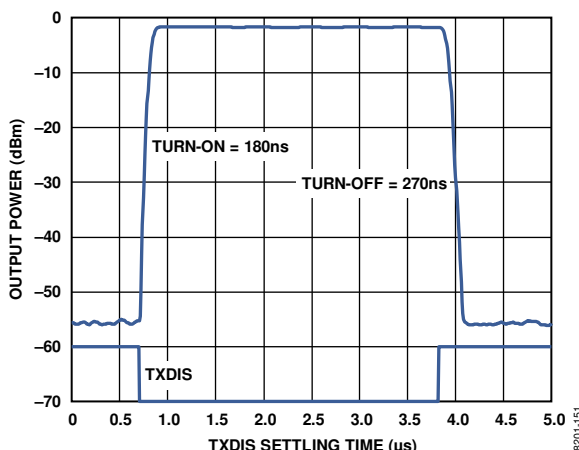


Figure 51. TXDIS Turn-On Settling Time at Worst-Case Supply and Temperature

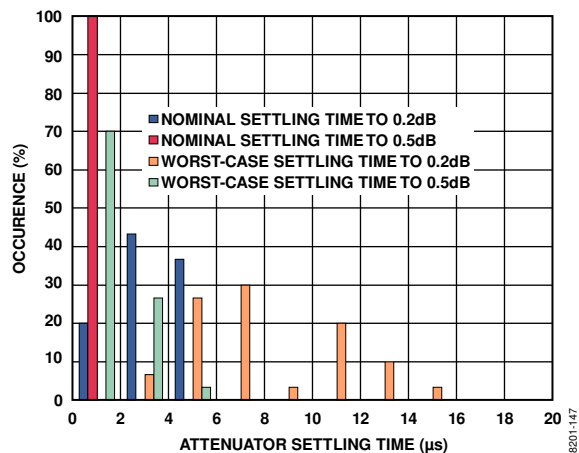


Figure 49. Attenuator Settling Time to 0.2 dB and 0.5 dB Distribution at Nominal and Worst-Case Conditions for Typical Large Step (0 dB to 47 dB)

THEORY OF OPERATION

OVERVIEW

The ADRF6750 device can be divided into the following basic building blocks:

- PLL synthesizer and VCO
- Quadrature modulator
- Attenuator
- Voltage regulator
- I²C/SPI interface

Each of these building blocks is described in detail in the sections that follow.

PLL SYNTHESIZER AND VCO

Overview

The phase-locked loop (PLL) consists of a fractional-N frequency synthesizer with a 25-bit fixed modulus, allowing a frequency resolution of less than 1 Hz over the entire frequency range. It also has an integrated voltage-controlled oscillator (VCO) with a fundamental output frequency ranging from 1900 MHz to 3150 MHz. This allows the PLL to generate a stable frequency at 2× LO, which is then divided down to provide a local oscillator (LO) frequency ranging from 950 MHz to 1575 MHz to the quadrature modulator.

Reference Input Section

The reference input stage is shown in Figure 52. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed, and SW1 and SW2 are open. This ensures that there is no loading of the REF_{IN} pin at power-down.

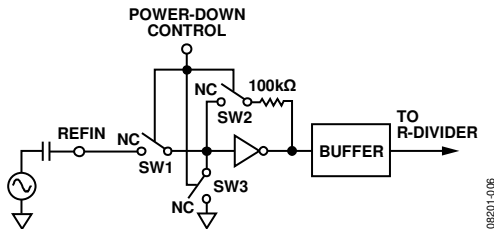


Figure 52. Reference Input Stage

Reference Input Path

The on-chip reference frequency doubler allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves the in-band phase noise performance by 3 dBc/Hz.

The 5-bit R-divider allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

An additional divide-by-2 function in the reference input path allows for a greater division range.

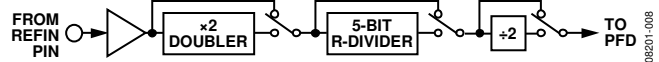


Figure 53. Reference Input Path

The PFD frequency equation is

$$f_{PFD} = f_{REFIN} \times [(1 + D)/(R \times (1 + T))] \quad (2)$$

where:

f_{REFIN} is the reference input frequency.

D is the doubler bit.

R is the programmed divide ratio of the binary 5-bit programmable reference divider (1 to 32).

T is the divide-by-2 bit (0 or 1).

RF Fractional-N Divider

The RF fractional-N divider allows a division ratio in the PLL feedback path that can range from 23 to 4095. The relationship between the fractional-N divider and the LO frequency is described in the following section.

INT and FRAC Relationship

The integer (INT) and fractional (FRAC) values make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector (PFD) frequency. See the Example—Changing the LO Frequency section for more information.

The LO frequency equation is

$$LO = f_{PFD} \times (INT + (FRAC/2^{25})) \quad (1)$$

where:

LO is the local oscillator frequency.

f_{PFD} is the PFD frequency.

INT is the integer component of the required division factor and is controlled by the CR6 and CR7 registers.

FRAC is the fractional component of the required division factor and is controlled by the CR0 to CR3 registers.

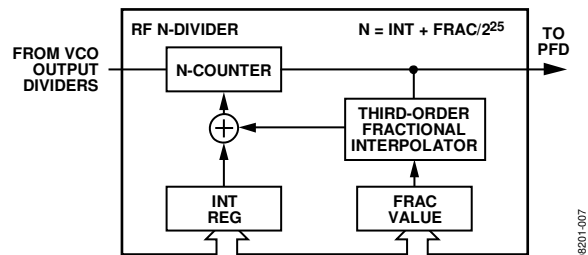


Figure 54. RF Fractional-N Divider

Phase Frequency Detector (PFD) and Charge Pump

The PFD takes inputs from the R-divider and the N-counter and produces an output proportional to the phase and frequency difference between them (see Figure 55 for a simplified schematic). The PFD includes a fixed delay element that sets the width of the antibacklash pulse, ensuring that there is no dead zone in the PFD transfer function.

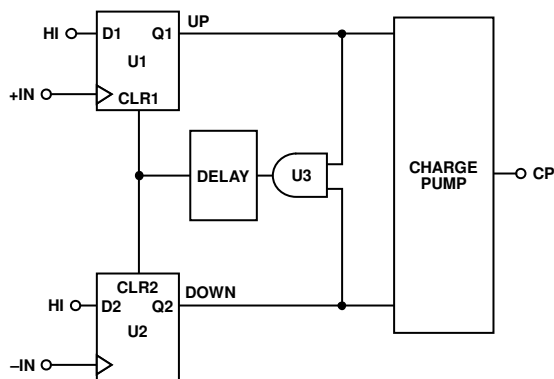


Figure 55. PFD Simplified Schematic

Lock Detect (LDET)

LDET (Pin 44) signals when the PLL has achieved lock to an error frequency of less than 100 Hz. On a write to Register CR0, a new PLL acquisition cycle starts, and the LDET signal goes low. When lock has been achieved, this signal returns high.

Voltage-Controlled Oscillator (VCO)

The VCO core in the ADRF6750 consists of two separate VCOs, each with 16 overlapping bands. Figure 56 shows an acquisition plot demonstrating both the VCO overlap at roughly 1260 MHz and the multiple overlapping bands within each VCO. The choice of two 16-band VCOs allows a wide frequency range to be covered without a large VCO sensitivity (K_{VCO}) and resultant poor phase noise and spurious performance. Note that the VCO range is larger than the $2 \times$ LO frequency range of the part to ensure that the device has enough margin to cover the full frequency range over all conditions.

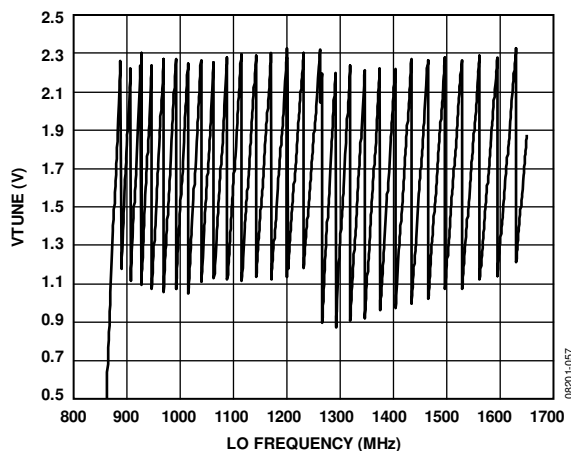


Figure 56. V_{TUNE} vs. LO Frequency

The correct VCO and band are chosen automatically by the VCO and band select circuitry when Register CR0 is updated. This is referred to as autocalibration.

The autocalibration time is set to 50 μ s. During this time, the VCO V_{TUNE} is disconnected from the output of the loop filter and is connected to an internal reference voltage. A typical frequency acquisition is shown in Figure 57.

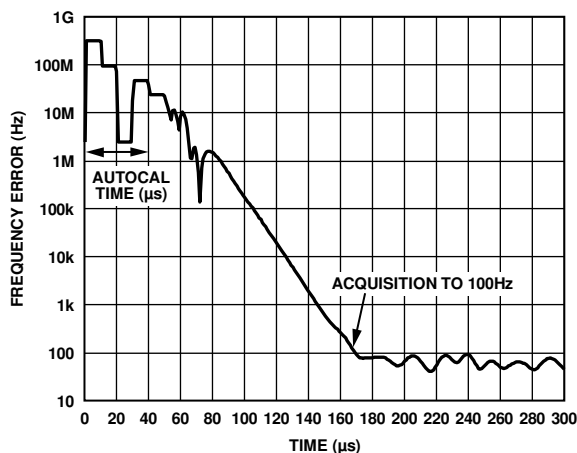


Figure 57. PLL Acquisition

After autocalibration, normal PLL action resumes and the correct frequency is acquired to within a frequency error of 100 Hz in 170 μ s typically.

For a maximum cumulative step of 100 kHz, autocalibration can be turned off by Register CR24, Bit 0. This enables cumulative PLL acquisitions of 100 kHz or less to occur without the autocalibration procedure, which improves acquisition times significantly (see Figure 58).

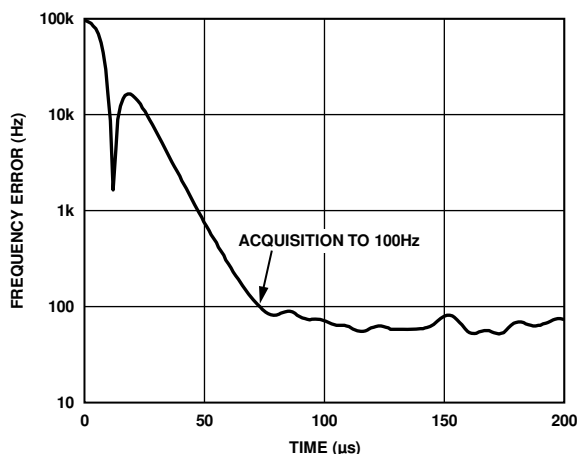


Figure 58. PLL Acquisition Without Autocalibration for 100 kHz Step

The VCO displays a variation of K_{VCO} as V_{TUNE} varies within the band and from band to band. Figure 59 shows how the K_{VCO} varies across the full LO frequency range. Also shown is the average value for each of the frequency bands. Figure 59 is useful when calculating the loop filter bandwidth and individual loop filter components.

ADRF6750

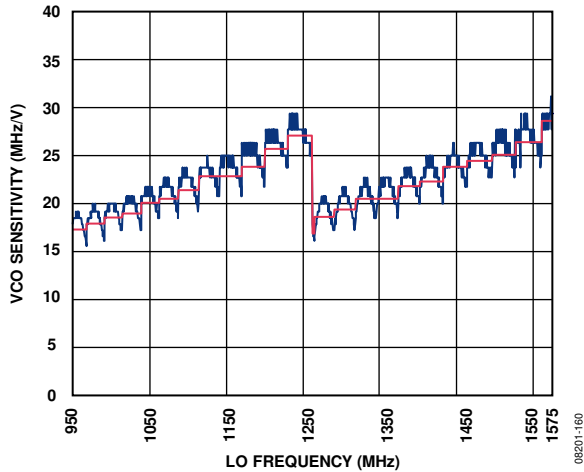


Figure 59. K_{vco} vs. LO Frequency

QUADRATURE MODULATOR

Overview

A basic block diagram of the ADRF6750 quadrature modulator circuit is shown in Figure 60. The VCO generates a signal at the $2 \times$ LO frequency, which is then divided down to give a signal at the LO frequency. This signal is then split into in-phase and quadrature components to provide the LO signals that drive the mixers.

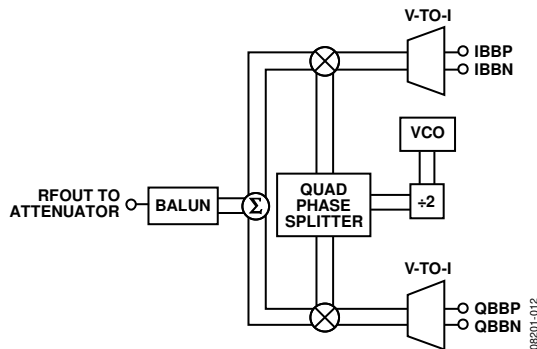


Figure 60. Block Diagram of the Quadrature Modulator

The I and Q baseband input signals are converted to currents by the V-to-I stages, which then drive the two mixers. The outputs of these mixers combine to feed the output balun, which provides a single-ended output. This single-ended output is then fed to the attenuator and, finally, to the external RFOUT signal pin.

Baseband Inputs

The baseband inputs, QBBP, QBBN, IBBP, and IBBN, must be driven from a differential source. The nominal drive level of 0.9 V p-p differential (450 mV p-p on each pin) should be biased to a common-mode level of 500 mV dc.

To set the dc bias level at the baseband inputs, refer to Figure 61. The average output current on each of the AD9779 outputs is 10 mA. A current of 10 mA flowing through each of the 50 Ω resistors to ground produces the desired dc bias of 500 mV at each of the baseband inputs.

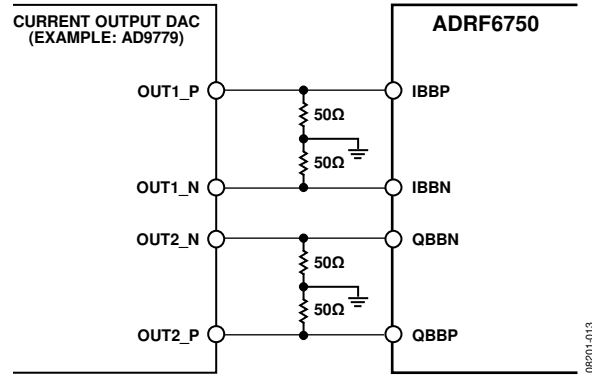


Figure 61. Establishing DC Bias Level on Baseband Inputs

The differential baseband inputs (QBBP, QBBN, IBBN, and IBBP) consist of the bases of PNP transistors, which present a high impedance of about 30 k Ω in parallel with roughly 2 pF of capacitance. The impedance looks like 30 k Ω below 1 MHz and starts to roll off at higher frequency. A 100 Ω differential termination is recommended at the baseband inputs, and this dominates the input impedance as seen by the input baseband signal. This ensures that the input impedance, as seen by the input circuit, remains flat across the baseband bandwidth. See Figure 62 for a typical configuration.

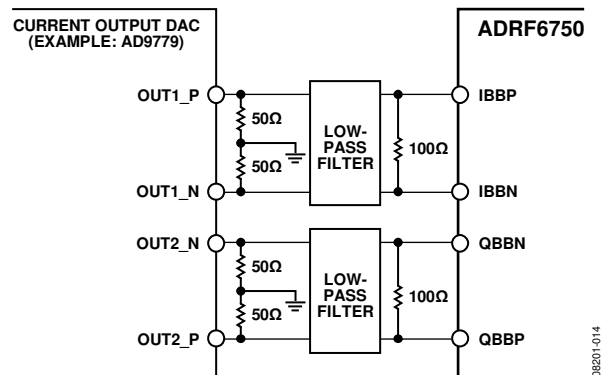


Figure 62. Typical Baseband Input Configuration

The swing of the AD9779 output currents ranges from 0 mA to 20 mA. The ac voltage swing is 1 V p-p single-ended or 2 V p-p differential with the 50 Ω resistors in place. The 100 Ω differential termination resistors at the baseband inputs have the effect of limiting this swing without changing the dc bias condition of 500 mV. The low-pass filter is used to filter the DAC outputs and remove images when driving a modulator.

Another consideration is that the baseband inputs actually source a current of 240 μ A out of each of the four inputs. This current must be taken into account when setting up the dc bias of 500 mV. In the initial example based on Figure 61, an error of 12 mV occurs due to the 240 μ A current flowing through the 50 Ω resistor. Analog Devices, Inc., recommends that the accuracy of the dc bias should be 500 mV \pm 25 mV. It is also important that this 240 μ A current have a dc path to ground.

Optimization

The carrier feedthrough and the sideband suppression performance of the ADRF6750 can be improved over the numbers specified in Table 1 by using the following optimization techniques.

Carrier Feedthrough Nulling

Carrier feedthrough results from dc offsets that occur between the P and N inputs of each of the differential baseband inputs. Normally these inputs are set to a dc bias of approximately 500 mV.

However, if a dc offset is introduced between the P and N inputs of either or both I and Q inputs, the carrier feedthrough is affected in either a positive or a negative fashion. Note that the dc bias level remains at 500 mV (average P and N level). The I channel offset is often held constant while the Q channel offset is varied until a minimum carrier feedthrough level is obtained. Then, while retaining the new Q channel offset, the I channel offset is adjusted until a new minimum is reached. This is usually performed at a single frequency and, thus, is not optimized over the complete frequency range. Multiple optimizations at different frequencies must be performed to ensure optimum carrier feedthrough across the full frequency range.

Sideband Suppression Nulling

Sideband suppression results from relative gain and relative phase offsets between the I channel and Q channel and can be optimized through adjustments to those two parameters. Adjusting only one parameter improves the sideband suppression only to a point. For optimum sideband suppression, an iterative adjustment between phase and amplitude is required.

ATTENUATOR

The digital attenuator consists of six attenuation blocks: 1 dB, 2 dB, 4 dB, 8 dB, and two 16 dB blocks; each is separately controlled. Each attenuation block consists of field effect transistor (FET) switches and resistors that form either a pi-shaped or a T-shaped attenuator. By controlling the states of the FET switches through the control lines, each attenuation block can be set to the pass state (0 dB) or the attenuation state (n dB). The various combinations of the six blocks provide the attenuation states from 0 dB to 47 dB in 1 dB increments.

VOLTAGE REGULATOR

The voltage regulator is powered from a 5 V supply that is provided by VCC1 (Pin 11) and produces a 3.3 V nominal regulated output voltage, REGOUT, on Pin 12. This pin must be connected (external to the IC) to the VREG1 through VREG6 package pins.

The regulator output (REGOUT) should be decoupled by a parallel combination of 10 pF and 220 μ F capacitors. The 220 μ F capacitor, which is recommended for best performance, decouples broadband noise, leading to better phase noise. Each VREGx pin should have the following decoupling capacitors: 100 nF multilayer ceramic with an additional 10 pF in parallel, both placed as close as possible to the DUT power supply pins.

X7R or X5R capacitors are recommended. See the Evaluation Board section for more information.

EXTERNAL VCO OPERATION

The ADRF6750 can be operated with an external VCO. This can be useful if the user wants to improve the phase noise performance or extend the frequency range. Note that the external VCO needs to operate at a frequency of $2 \times \text{LO}$. To operate the ADRF6750 with an external VCO, follow these steps:

1. Connect the charge pump output (Pin 9) to the loop filter and onward to the external VCO input. The K_{VCO} of the external VCO needs to be taken into account when calculating the loop bandwidth and loop filter components. Note that a 50 kHz loop bandwidth is recommended when using the internal VCO. This takes into account the phase noise performance of the internal VCO. It is possible for an external VCO to provide better phase noise performance and a 50 kHz loop bandwidth may not be optimal in that case. When selecting a loop bandwidth, consider rms jitter, phase noise performance, and acquisition time. ADISimPLL™ can be used to optimize the loop bandwidth with a variety of external VCOs.
2. Connect the output of the external VCO to the TESTLO and $\overline{\text{TESTLO}}$ input pins.

It is likely that a low-pass filter will be needed to filter the output of the external VCO. This is very important if the external VCO has poor second harmonic performance. Second harmonic performance directly impacts sideband suppression performance. For example, -30 dBc second harmonic performance leads to -30 dBc sideband suppression. Both TESTLO and $\overline{\text{TESTLO}}$ need to be dc biased. A dc bias of 1.7 V to 3.3 V is recommended. The REGOUT output provides a 3.3 V output voltage.

3. Select external VCO operation by setting the following bits:
 - Set Register CR27[3] = 1. This bit multiplexes the TESTLO and $\overline{\text{TESTLO}}$ through to the quadrature modulator.
 - Set Register CR28[5] = 1. This bit powers down the internal VCO and connects the external VCO to the PLL.
4. Set the correct polarity for the PFD based on the slope of the K_{VCO} . The default is for positive polarity. This bit is accessed by Register CR12[3].

When selecting an external VCO, at times it is difficult to select one with an appropriate frequency range and K_{VCO} . One solution may be the ADF4350, which can function as VCO only with a range of 137.5 MHz to 4.4 GHz. Note that the ADF4350 requires an autocalibration time of 100 μ s which directly impacts acquisition time.

I²C INTERFACE

The ADRF6750 supports a 2-wire, I²C-compatible serial bus that drives multiple peripherals. The serial data (SDA) and serial

ADRF6750

clock (SCL) inputs carry information between any devices that are connected to the bus. Each slave device is recognized by a unique address. The ADRF6750 has two possible 7-bit slave addresses for both read and write operations. The MSB of the 7-bit slave address is set to 1. Bit 5 of the slave address is set by the CS pin (Pin 27). Bits[4:0] of the slave address are set to all 0s. The slave address consists of the seven MSBs of an 8-bit word. The LSB of the word sets either a read or a write operation (see Figure 63). Logic 1 corresponds to a read operation, whereas Logic 0 corresponds to a write operation.

To control the device on the bus, the following protocol must be followed. The master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address and the R/W bit). The bits are transferred from MSB to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices then withdraw from the bus and maintain an idle condition. During the idle condition, the device monitors the SDA and SCL lines waiting for the start condition and the correct transmitted address. The R/W bit determines the direction of the data. Logic 0 on the LSB of the

first byte indicates that the master writes information to the peripheral. Logic 1 on the LSB of the first byte indicates that the master reads information from the peripheral.

The ADRF6750 acts as a standard slave device on the bus. The data on the SDA pin (Pin 29) is eight bits long, supporting the 7-bit addresses plus the R/W bit. The ADRF6750 has 34 subaddresses to enable the user-accessible internal registers. Therefore, it interprets the first byte as the device address and the second byte as the starting subaddress. Autoincrement mode is supported, which allows data to be read from or written to the starting subaddress and each subsequent address without manually addressing the subsequent subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all registers.

Stop and start conditions can be detected at any stage of the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. If an invalid subaddress is issued by the user, the ADRF6750 does not issue an acknowledge and returns to the idle condition. In a no acknowledge condition, the SDA line is not pulled low on the ninth pulse. See Figure 64 and Figure 65 for sample write and read data transfers, Figure 66 for the timing protocol, and Figure 2 for a more detailed timing diagram.

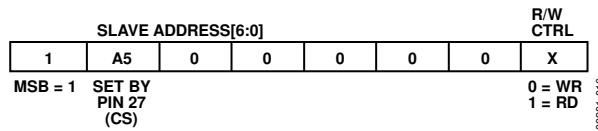


Figure 63. Slave Address Configuration

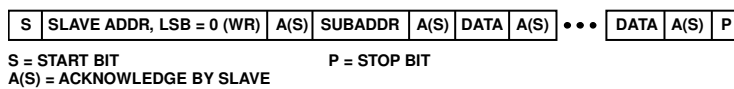


Figure 64. I²C Write Data Transfer

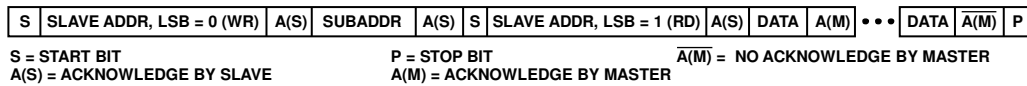


Figure 65. I²C Read Data Transfer

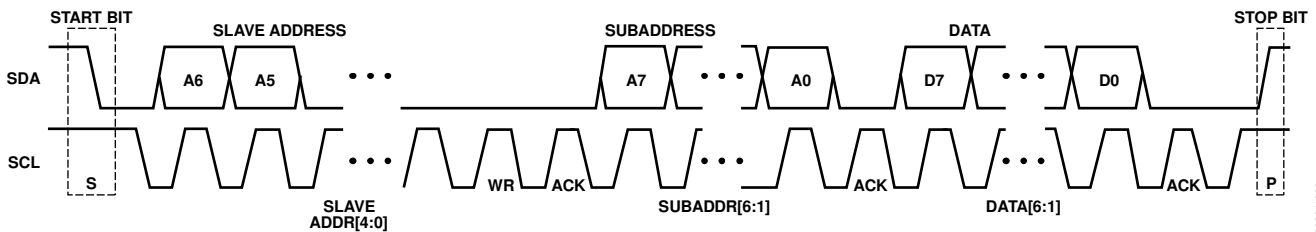


Figure 66. I²C Data Transfer Timing

SPI INTERFACE

The ADRF6750 also supports the SPI protocol. The part powers up in I²C mode but is not locked in this mode. To stay in I²C mode, it is recommended that the user tie the CS line to either 3.3 V or GND, thus disabling SPI mode. It is not possible to lock the I²C mode, but it is possible to select and lock the SPI mode.

To select and lock the SPI mode, three pulses must be sent to the CS pin, as shown in Figure 67. When the SPI protocol is locked in, it cannot be unlocked while the device is still powered up. To reset the serial interface, the part must be powered down and powered up again.

Serial Interface Selection

The CS pin controls selection of the I²C or SPI interface.

Figure 67 shows the selection process that is required to lock the SPI mode. To communicate with the part using the SPI protocol, three pulses must be sent to the CS pin. On the third rising edge, the part selects and locks the SPI protocol. Consistent with most SPI standards, the CS pin must be held low during all SPI communication to the part and held high at all other times.

SPI Serial Interface Functionality

The SPI serial interface of the ADRF6750 consists of the CS, SDI (SDI/SDA), CLK (CLK/SCL), and SDO pins. CS is used to select the device when more than one device is connected to the serial clock and data lines. CLK is used to clock data in and out of the part. The SDI pin is used to write to the registers. The SDO pin is a dedicated output for the read mode. The part operates in slave mode and requires an externally applied serial clock to the CLK pin. The serial interface is designed to allow the part to be interfaced to systems that provide a serial clock that is synchronized to the serial data.

Figure 68 shows an example of a write operation to the ADRF6750. Data is clocked into the registers on the rising edge of CLK using a 24-bit write command. The first eight bits represent the write command 0xD4, the next eight bits are the register address, and the final eight bits are the data to be written to the specific register. Figure 69 shows an example of a read operation. In this example, a shortened 16-bit write command is first used to select the appropriate register for a read operation, the first eight bits representing the write command 0xD4 and the final eight bits representing the specific register. Then the CS line is pulsed low for a second time to retrieve data from the selected register using a 16-bit read command, the first eight bits representing the read command 0xD5 and the final eight bits representing the contents of the register being read. Figure 3 shows the timing for both SPI read and SPI write operations.

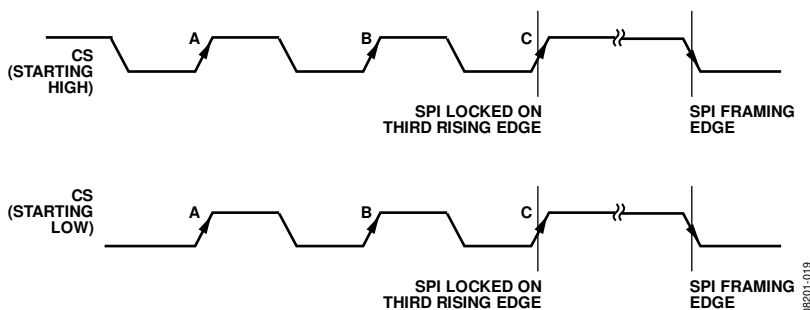


Figure 67. Selecting the SPI Protocol

ADRF6750

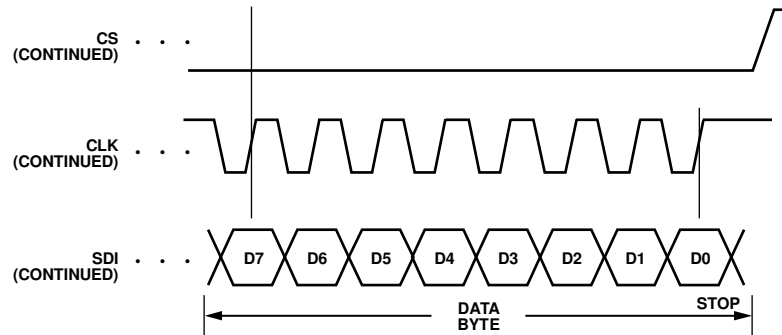
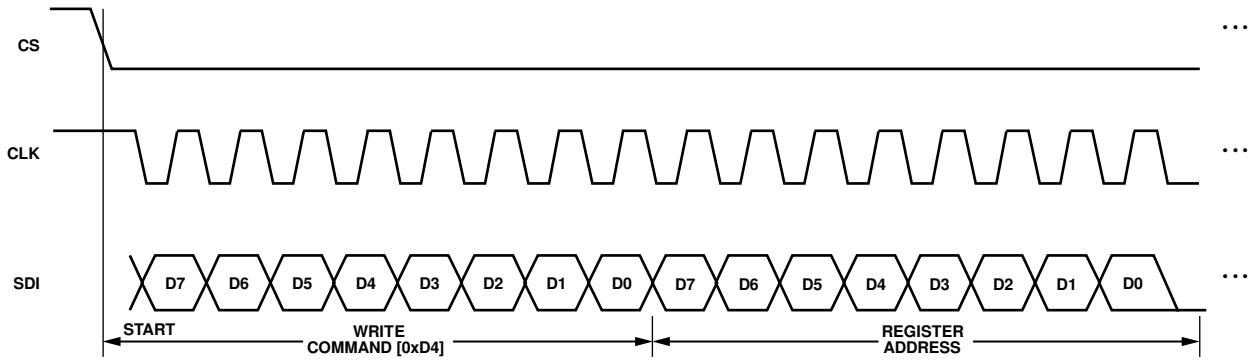


Figure 68. SPI Byte Write Example

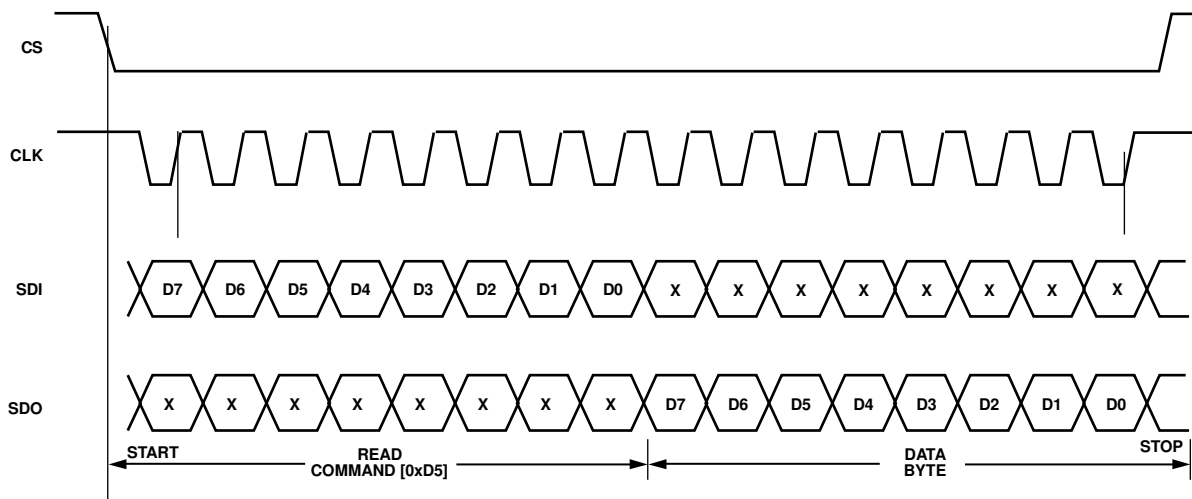
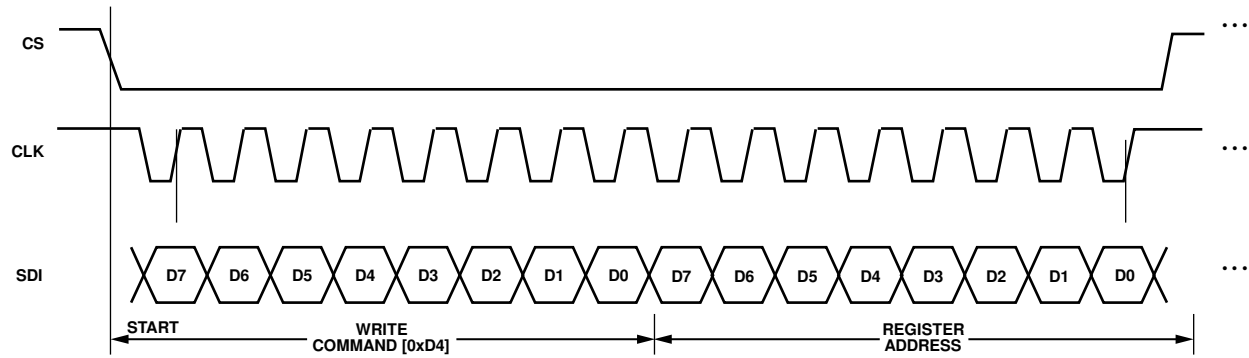


Figure 69. SPI Byte Read Example