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Automotive LPDDR2 SDRAM

EDB1332BD, EDB1316BD, EDB2432B4

Features

- Ultra low-voltage core and I/O power supplies
  - V_{DD2} = 1.14–1.30V
  - V_{DDCA}/V_{DDQ} = 1.14–1.30V
  - V_{DD1} = 1.70–1.95V
- Clock frequency range
  - 533–10 MHz (data rate range: 1066–20 Mb/s/pin)
- Four-bit prefetch DDR architecture
- Eight internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Per-bank refresh for concurrent operation
- On-chip temperature sensor to control self refresh rate (SR not supported >105°C)
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock stop capability
- RoHS-compliant, "green" packaging

Options	Marking
• Density/Page Size	
– 1Gb/2KB - single die	13
– 2Gb/2KB - dual die	24
• Organization	
– x16	16
– x32	32
• V_{DD2}: 1.2V	B
• Revision	
– Single die	D
– Multi-die	4
• FBGA "green" package	
– 134-ball FBGA	BH
– 134-ball multi-die FBGA	MA
• Timing – cycle time	
– 1.875ns @ RL = 8	-1D
• Special options	
– Automotive grade (Package-level burn-in)	A
• Operating temperature range[1]	
– From –40°C to +85°C	IT
– From –40°C to +105°C	AT
– From –40°C to +125°C	UT[2]

Notes:
1. When T_C >105°C, self-refresh mode is not available.
2. UT option use based on automotive usage model. Please contact Micron sales representative with questions.

Table 1: Key Timing Parameters

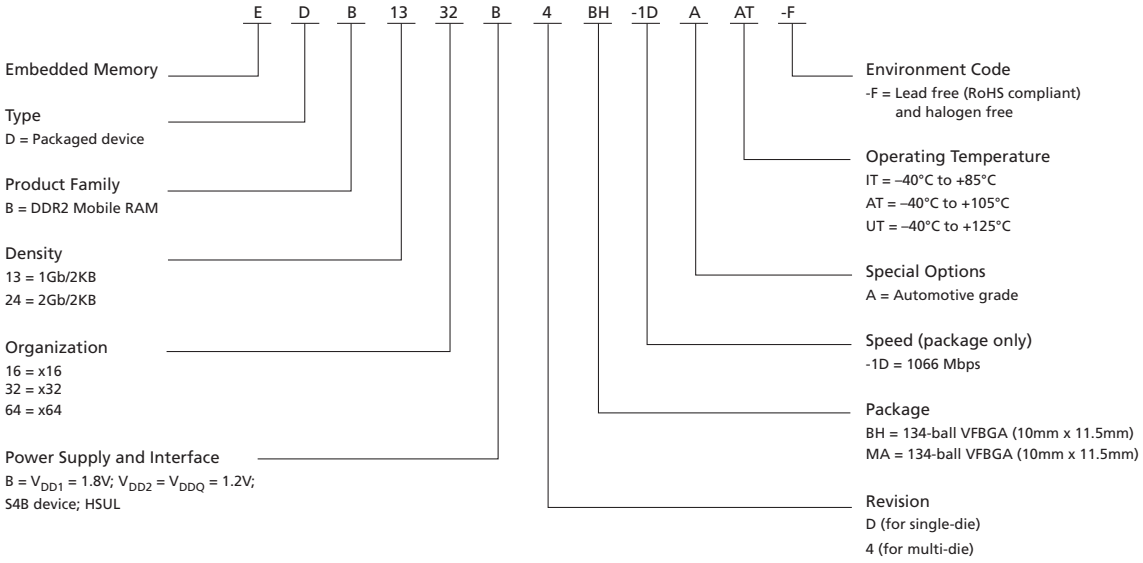
Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL	tRCD/tRP
-1D	533	1066	8	4	Typical

Table 2: S4 Configuration Addressing

Architecture	64 Meg x 16	32 Meg x 32	64 Meg x 32
Die configuration	8 Meg x 16 x 8 banks	4 Meg x 32 x 8 banks	2 x 8 Meg x 16 x 8 banks
Row addressing	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])
Column addressing	1K (A[9:0])	512 (A[8:0])	1K (A[9:0])
Number of die	1	1	2
Die per rank	1	1	2
Ranks per channel [1]	1	1	1

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

Figure 1: LPDDR2 Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Table 3: Package Codes and Descriptions

Package Code	Ball Count	# Ranks	# Channels	Size (mm)	Die per Package	Solder Ball Composition
BH	134	1	1	10 x 11.5 x 1.0, 0.65 pitch	SDP	SAC302
MA	134	1	1	10 x 11.5 x 1.0, 0.65 pitch	DDP	SAC302

Notes: 1. SDP = single-die package; DDP = Dual-die package
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

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General Description

The Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. The LPDDR2-S4 device is internally configured as an eight-bank DRAM. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8192 rows by 512 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

In timing diagrams, "CMD" is used as an indicator only. Actual signals occur on CA[9:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ}.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

I_{DD} Specifications

Table 4: I_{DD} Specifications (32 Meg x 32)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD01}	V_{DD1}	6	mA
I_{DD02}	V_{DD2}	30	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2P1}	V_{DD1}	600	µA
I_{DD2P2}	V_{DD2}	1600	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2PS1}	V_{DD1}	600	µA
I_{DD2PS2}	V_{DD2}	1600	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2N1}	V_{DD1}	0.6	mA
I_{DD2N2}	V_{DD2}	20	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2NS1}	V_{DD1}	0.6	mA
I_{DD2NS2}	V_{DD2}	12	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3P1}	V_{DD1}	1.4	mA
I_{DD3P2}	V_{DD2}	5	
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3PS1}	V_{DD1}	1.4	mA
I_{DD3PS2}	V_{DD2}	5	
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3N1}	V_{DD1}	1.5	mA
I_{DD3N2}	V_{DD2}	22	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3NS1}	V_{DD1}	1.5	mA
I_{DD3NS2}	V_{DD2}	14	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD4R1}	V_{DD1}	2	mA
I_{DD4R2}	V_{DD2}	180	
$I_{DD4R,in}$	V_{DDCA}	2	
I_{DD4W1}	V_{DD1}	2	mA
I_{DD4W2}	V_{DD2}	200	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	1	

Table 4: I_{DD} Specifications (32 Meg x 32) (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD51}	V_{DD1}	20	mA
I_{DD52}	V_{DD2}	70	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5PB1}	V_{DD1}	2	mA
I_{DD5PB2}	V_{DD2}	23	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5AB1}	V_{DD1}	2	mA
I_{DD5AB2}	V_{DD2}	23	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD61}	V_{DD1}	–	Table 6
I_{DD62}	V_{DD2}	–	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	–	
I_{DD81}	V_{DD1}	50	µA
I_{DD82}	V_{DD2}	50	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	20	

Table 5: I_{DD} Specifications (64 Meg x 16)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD01}	V_{DD1}	6	mA
I_{DD02}	V_{DD2}	30	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2P1}	V_{DD1}	600	µA
I_{DD2P2}	V_{DD2}	1600	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2PS1}	V_{DD1}	600	µA
I_{DD2PS2}	V_{DD2}	1600	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2N1}	V_{DD1}	0.6	mA
I_{DD2N2}	V_{DD2}	20	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2NS1}	V_{DD1}	0.6	mA
I_{DD2NS2}	V_{DD2}	12	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	1	

Table 5: I_{DD} Specifications (64 Meg x 16) (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD3P1}	V_{DD1}	1.4	mA
I_{DD3P2}	V_{DD2}	5	
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3PS1}	V_{DD1}	1.4	mA
I_{DD3PS2}	V_{DD2}	5	
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3N1}	V_{DD1}	1.5	mA
I_{DD3N2}	V_{DD2}	22	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3NS1}	V_{DD1}	1.5	mA
I_{DD3NS2}	V_{DD2}	14	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD4R1}	V_{DD1}	2	mA
I_{DD4R2}	V_{DD2}	140	
$I_{DD4R,in}$	V_{DDCA}	2	
I_{DD4W1}	V_{DD1}	2	mA
I_{DD4W2}	V_{DD2}	155	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD51}	V_{DD1}	20	mA
I_{DD52}	V_{DD2}	70	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5PB1}	V_{DD1}	2	mA
I_{DD5PB2}	V_{DD2}	23	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5AB1}	V_{DD1}	2	mA
I_{DD5AB2}	V_{DD2}	23	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD61}	V_{DD1}	–	Table 6
I_{DD62}	V_{DD2}	–	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	–	
I_{DD81}	V_{DD1}	50	µA
I_{DD82}	V_{DD2}	50	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	20	

Table 6: I_{DD6} Partial-Array Self Refresh Current (32 Meg x 32, 64 Meg x 16)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	I_{DD6} Partial-Array Self Refresh Current			Unit
		-40°C to +85°C	+85°C to +105°C	+105°C to +125°C	
Full array	V_{DD1}	230	2100	–	µA
	V_{DD2}	700	4400	–	
	V_{DDi}	20	20	–	
1/2 array	V_{DD1}	200	2000	–	
	V_{DD2}	500	2900	–	
	V_{DDi}	20	20	–	
1/4 array	V_{DD1}	190	1800	–	
	V_{DD2}	400	2000	–	
	V_{DDi}	20	20	–	
1/8 array	V_{DD1}	185	1700	–	
	V_{DD2}	360	1800	–	
	V_{DDi}	20	20	–	

Notes:
1. LPDDR2-S4 SDRAM devices support both bank-masking and segment-masking. I_{DD6} PASR currents are measured using bank-masking only.
2. When T_C >105°C: Self refresh mode is not available.

Table 7: I_{DD} Specifications (64 Meg x 32)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD01}	V_{DD1}	12	mA
I_{DD02}	V_{DD2}	60	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD2P1}	V_{DD1}	1200	µA
I_{DD2P2}	V_{DD2}	3200	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	200	
I_{DD2PS1}	V_{DD1}	1200	µA
I_{DD2PS2}	V_{DD2}	3200	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	200	
I_{DD2N1}	V_{DD1}	1.2	mA
I_{DD2N2}	V_{DD2}	40	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD2NS1}	V_{DD1}	1.2	mA
I_{DD2NS2}	V_{DD2}	24	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	2	

Table 7: I_{DD} Specifications (64 Meg x 32) (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD3P1}	V_{DD1}	2.8	mA
I_{DD3P2}	V_{DD2}	10	
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.2	
I_{DD3PS1}	V_{DD1}	2.8	mA
I_{DD3PS2}	V_{DD2}	10	
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.2	
I_{DD3N1}	V_{DD1}	3	mA
I_{DD3N2}	V_{DD2}	44	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD3NS1}	V_{DD1}	3	mA
I_{DD3NS2}	V_{DD2}	28	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD4R1}	V_{DD1}	4	mA
I_{DD4R2}	V_{DD2}	280	
$I_{DD4R,in}$	V_{DDCA}	4	
I_{DD4W1}	V_{DD1}	4	mA
I_{DD4W2}	V_{DD2}	310	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD51}	V_{DD1}	40	mA
I_{DD52}	V_{DD2}	140	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD5PB1}	V_{DD1}	4	mA
I_{DD5PB2}	V_{DD2}	46	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD5AB1}	V_{DD1}	4	mA
I_{DD5AB2}	V_{DD2}	46	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD61}	V_{DD1}	–	Table 8
I_{DD62}	V_{DD2}	–	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	–	
I_{DD81}	V_{DD1}	100	µA
I_{DD82}	V_{DD2}	100	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	40	

Table 8: I_{DD6} Partial-Array Self Refresh Current (64 Meg x 32)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	I_{DD6} Partial-Array Self Refresh Current			Unit
		-40°C to +85°C	+85°C to +105°C	+105°C to +125°C	
Full array	V_{DD1}	460	4200	–	µA
	V_{DD2}	1400	8800	–	
	V_{DDi}	40	40	–	
1/2 array	V_{DD1}	400	4000	–	
	V_{DD2}	1000	5800	–	
	V_{DDi}	40	40	–	
1/4 array	V_{DD1}	380	3600	–	
	V_{DD2}	800	4000	–	
	V_{DDi}	40	40	–	
1/8 array	V_{DD1}	370	3400	–	
	V_{DD2}	720	3600	–	
	V_{DDi}	40	40	–	

Notes:
1. LPDDR2-S4 SDRAM devices support both bank-masking and segment-masking. I_{DD6} PASR currents are measured using bank-masking only.
2. When T_C >105°C: Self refresh mode is not available.

Figure 2: V_{DD1}Typical Self-Refresh Current vs. Temperature (Per Die)

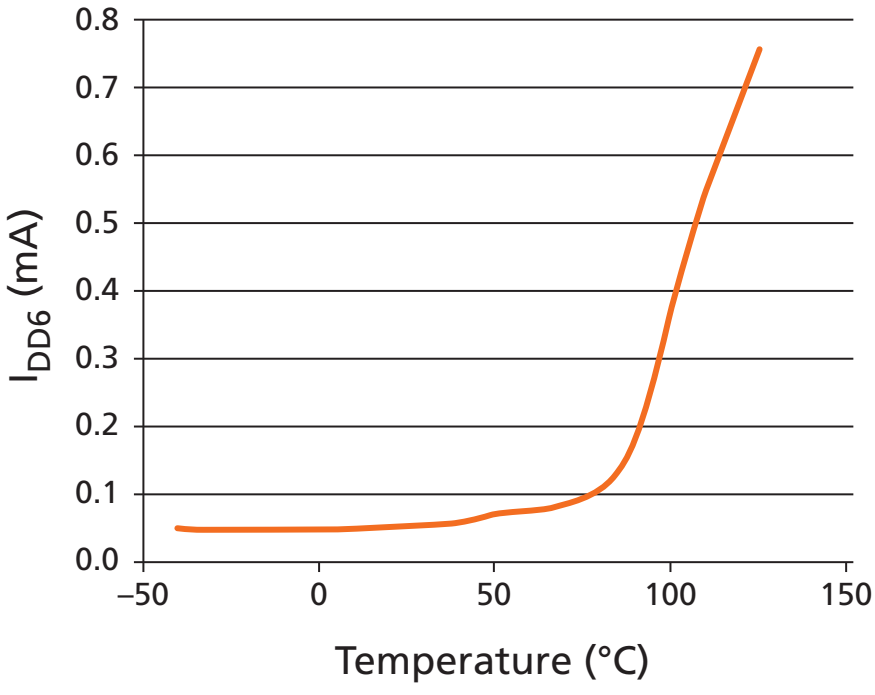
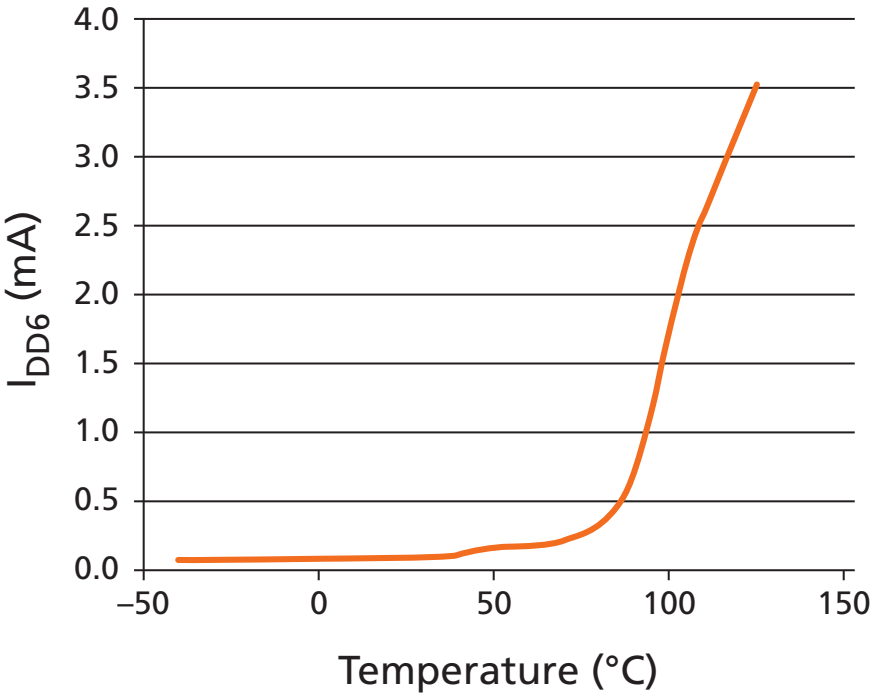


Figure 3: V_{DD2} Typical Self-Refresh Current vs. Temperature (Per Die)



Package Block Diagrams

Figure 4: Single Die Single Rank, Single Channel Package Block Diagram

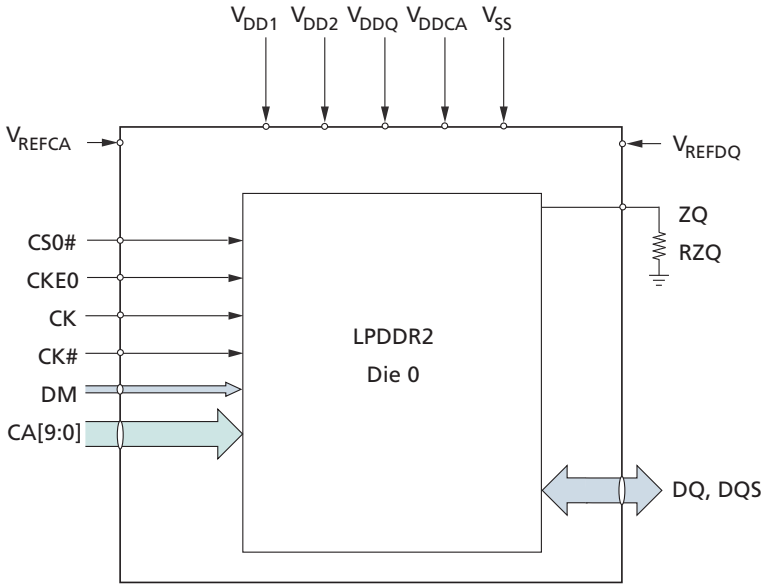
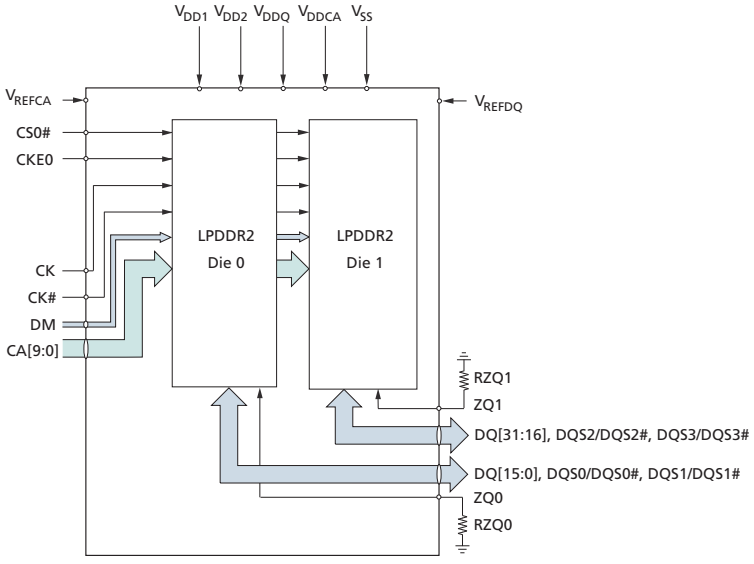
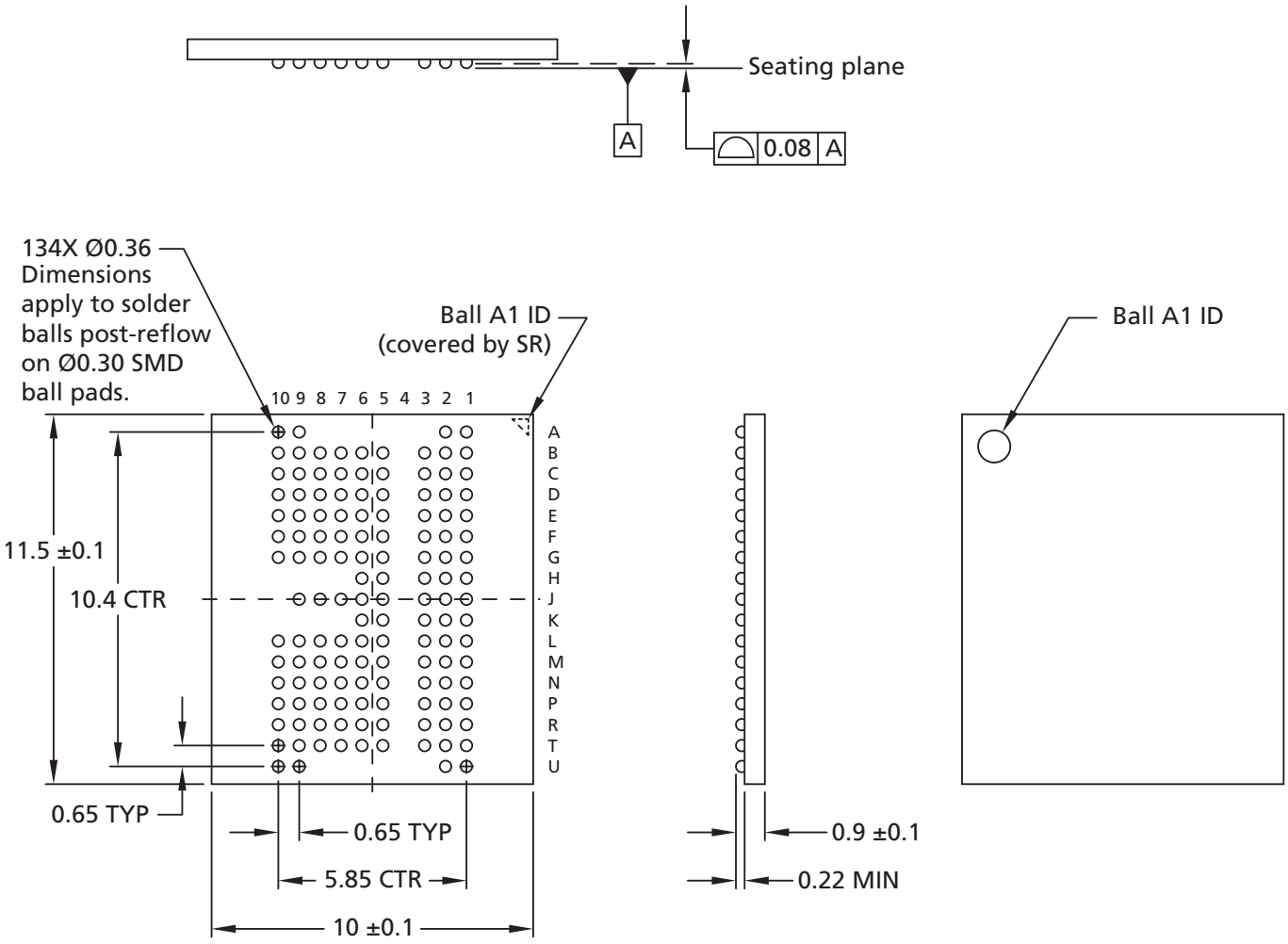


Figure 5: Dual Die Single Rank, Single Channel Package Block Diagram



Package Dimensions

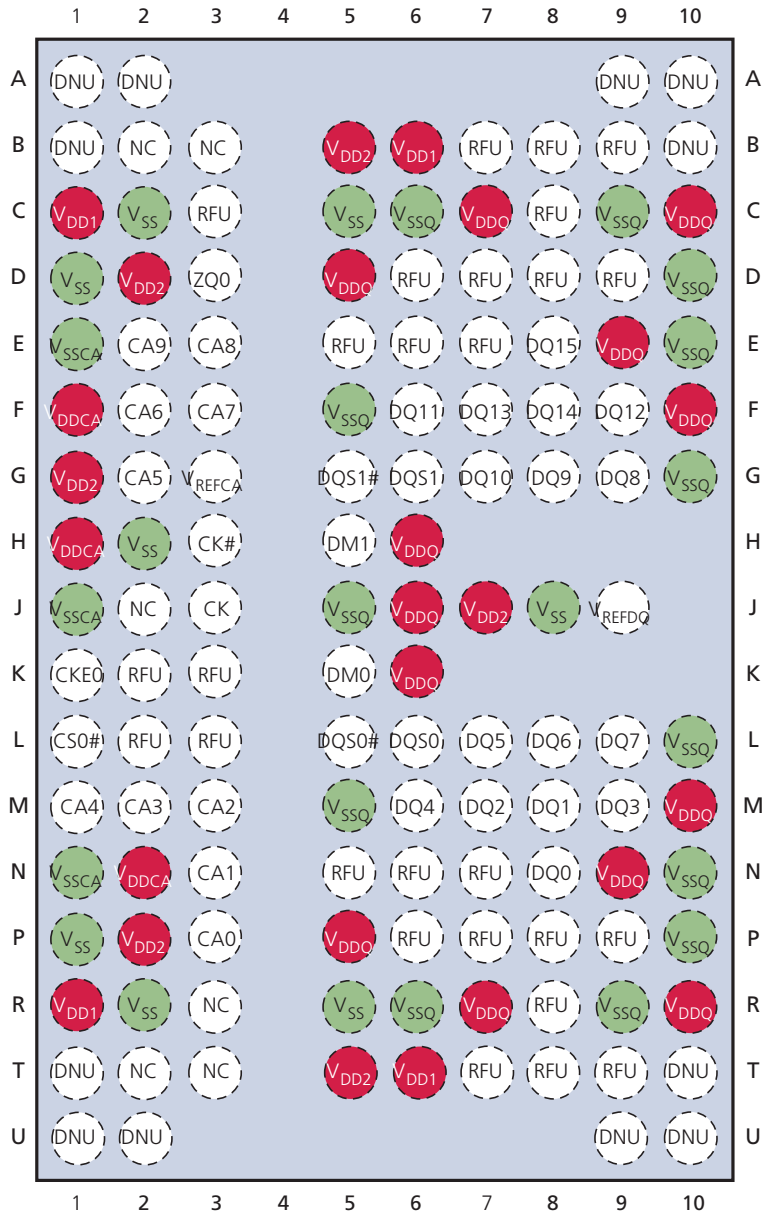
Figure 6: 134-Ball VFBGA – 10mm x 11.5mm (Package Code: BH, MA)



Note: 1. All dimensions are in millimeters.

Ball Assignments

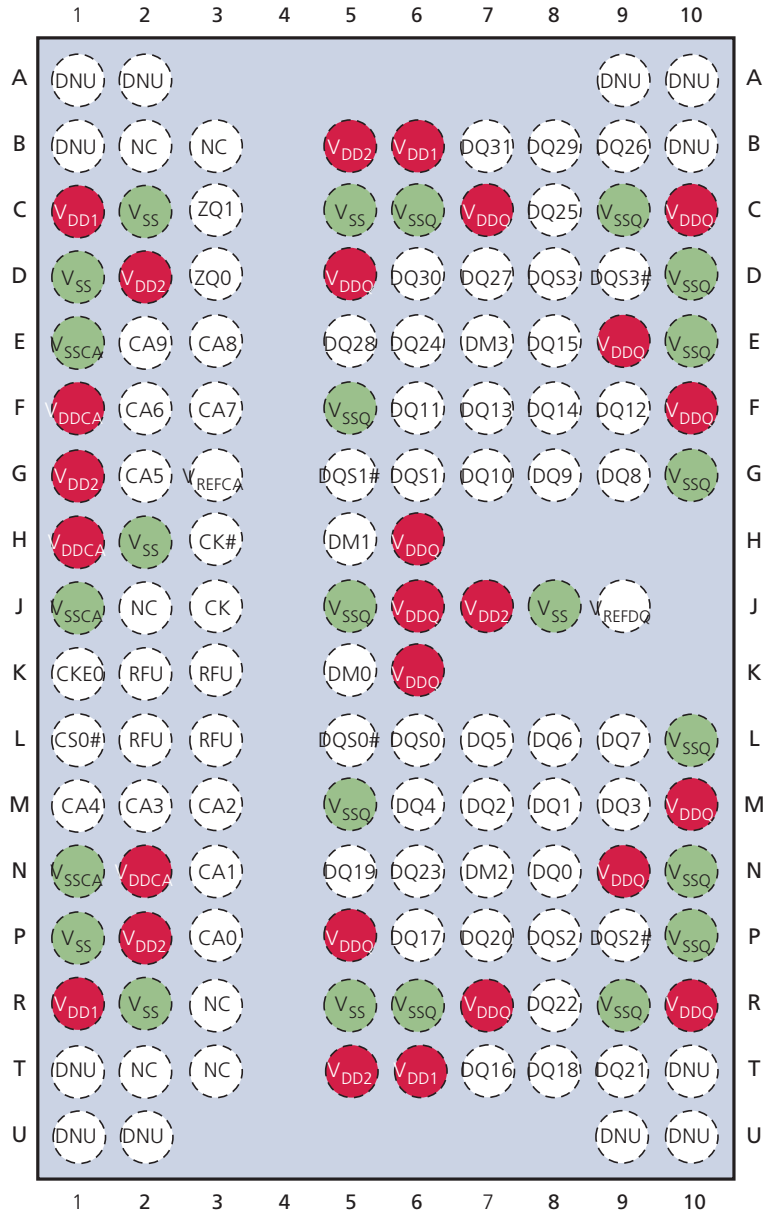
Figure 7: 134-Ball FBGA (64 Meg x16)



Top View (ball down)

Note: 1. V_{DDCA} is unnecessary. F1, H1, N2 pins should be left unconnected.

Figure 8: 134-Ball FBGA (32 Meg x 32, 64 Meg x 32)



Notes:
1. V_{DDCA} is unnecessary. F1, H1, N2 pins should be left unconnected.
2. C3 pin is RFU for 32 Meg x 32, and is ZQ1 for 64 Meg x 32.

Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See Ball Assignments for information specific to this device.

Table 9: Ball/Pad Descriptions

Symbol	Type	Description
CA[9:0]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE[1:0]	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK.
CS[1:0]#	Input	**Chip select:** CS# is considered part of the command code and is sampled at the rising edge of CK.
DM[3:0]	Input	**Input data mask:** DM is an input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[31:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[3:0], DQS[3:0]#	I/O	**Data strobe:** The data strobe is bidirectional (used for read and write data) and complementary (DQS and DQS#). It is edge-aligned output with read data and centered input with write data. DQS[3:0]/DQS[3:0]# is DQS for each of the four data bytes, respectively.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
V_{DDCA}	Supply	**Command/address power supply:** Command/address power supply.
V_{SSCA}	Supply	**Command/address ground:** Isolated on the die for improved noise immunity.
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{SS}	Supply	**Common ground**
V_{REFCA}, V_{REFDQ}	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers.
ZQ	Reference	**External impedance (240 ohm):** This signal is used to calibrate the device output impedance.
RFU	–	**Reserved for future use:** Must be left floating.
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.
(NC)	–	**No connect:** Balls indicated as (NC) are no connects, however, they could be connected together internally.

Functional Description

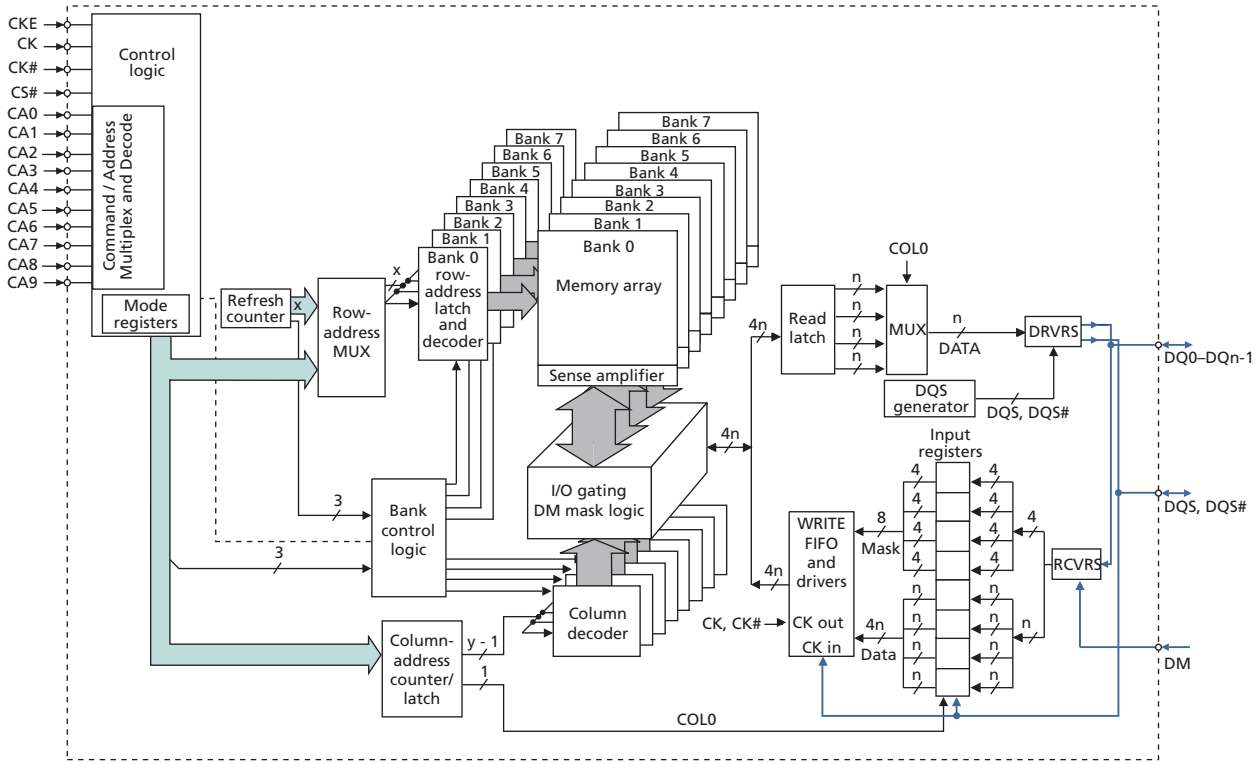
Mobile LPDDR2 is a high-speed SDRAM internally configured as a 4- or 8-bank memory device. LPDDR2 devices use a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

LPDDR2-S4 devices use a double data rate architecture on the DQ pins to achieve high-speed operation. The double data rate architecture is essentially a 4*n* prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command followed by a READ or WRITE command. The address and BA bits registered coincident with the ACTIVATE command are used to select the row and bank to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Figure 9: Functional Block Diagram



Power-Up

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory (see Figure 10 (page 25)). Power-up and initialization by means other than those specified will result in undefined operation.

1. Voltage Ramp

While applying power (after Ta), CKE must be held LOW (≤0.2 × V_{DDCA}), and all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

On or before the completion of the voltage ramp (Tb), CKE must be held LOW. DQ, DM, DQS, and DQS# voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latchup. CK, CK#, CS#, and CA input levels must be between V_{SSCA} and V_{DDCA} during voltage ramp to avoid latchup.

The following conditions apply for voltage ramp:

- Ta is the point when any power supply first reaches 300mV.
- Noted conditions apply between Ta and power-down (controlled or uncontrolled).
- Tb is the point at which all supply and reference voltages are within their defined operating ranges.
- Power ramp duration ^{t}INIT0 (Tb - Ta) must not exceed 20ms.
- For supply and reference voltage operating conditions, see the Recommended DC Operating Conditions table.
- The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins must not exceed 100mV.

Voltage Ramp Completion

After Ta is reached:

- V_{DD1} must be greater than V_{DD2} - 200mV
- V_{DD1} and V_{DD2} must be greater than V_{DDCA} - 200mV
- V_{DD1} and V_{DD2} must be greater than V_{DDQ} - 200mV
- V_{REF} must always be less than all other supply voltages

Beginning at Tb, CKE must remain LOW for at least ^{t}INIT1 = 100ns, after which CKE can be asserted HIGH. The clock must be stable at least ^{t}INIT2 = 5 × ^{t}CK prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS#, and CA inputs must observe setup and hold requirements (^{t}IS, ^{t}IH) with respect to the first rising clock edge (and to subsequent falling and rising edges).

If any MRRs are issued, the clock period must be within the range defined for ^{t}CKb (18ns to 100ns). MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, ^{t}DQSCK) could have relaxed timings (such as ^{t}DQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least ^{t}INIT3 = 200µs (Td).

2. RESET Command

After ^{t}INIT3 is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command.

Wait at least ^{t}INIT4 while keeping CKE asserted and issuing NOP commands.

3. MRRs and Device Auto Initialization (DAI) Polling

After ^{t}INIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications (see Power-Down (page 77)).

The MRR command can be used to poll the DAI bit, which indicates when device auto initialization is complete; otherwise, the controller must wait a minimum of ^{t}INIT5, or until the DAI bit is set, before proceeding.

Because the memory output buffers are not properly configured by Te, some AC parameters must use relaxed timing specifications before the system is appropriately configured.

After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0.

The device sets the DAI bit no later than ^{t}INIT5 after the RESET command. The controller must wait at least ^{t}INIT5 or until the DAI bit is set before proceeding.

4. ZQ Calibration

After ^{t}INIT5 (Tf), the MRW initialization calibration (ZQ calibration) command can be issued to the memory (MR10).

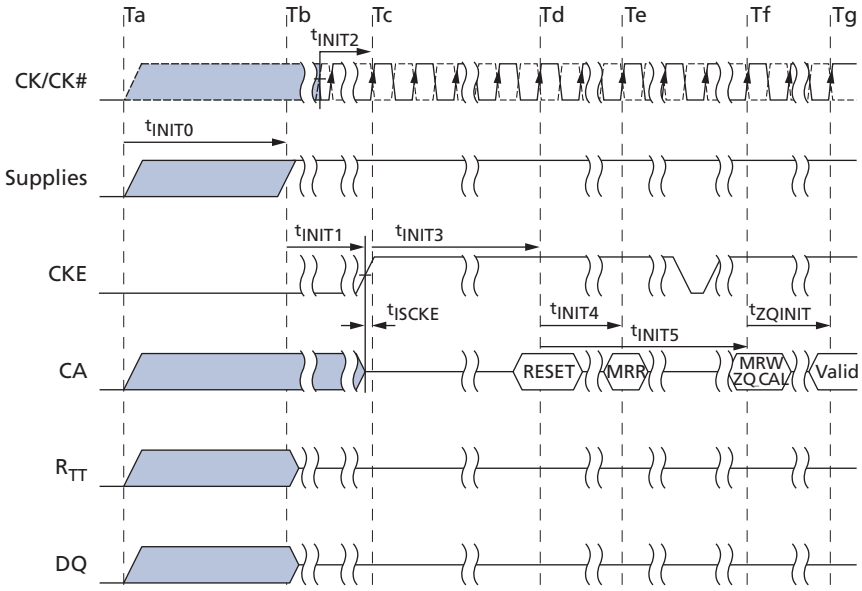
This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one Mobile LPDDR2 device exists on the same bus, the controller must not overlap MRW ZQ calibration commands. The device is ready for normal operation after ^{t}ZQINIT.

5. Normal Operation

After (Tg), MRW commands must be used to properly configure the memory (output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in Input Clock Frequency Changes and Clock Stop with CKE HIGH (page 86).

Figure 10: Voltage Ramp and Initialization Sequence



Note: 1. High-Z on the CA bus indicates valid NOP.

Table 10: Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	–	20	ms	Maximum voltage ramp time
tINIT1	100	–	ns	Minimum CKE LOW time after completion of voltage ramp
tINIT2	5	–	tCK	Minimum stable clock before first CKE HIGH
tINIT3	200	–	µs	Minimum idle time after first CKE assertion
tINIT4	1	–	µs	Minimum idle time after RESET command
tINIT5	–	10	µs	Maximum duration of device auto initialization
tZQINIT	1	–	µs	ZQ initial calibration (S4 devices only)
tCKb	18	100	ns	Clock cycle time during boot

Note: 1. The tINIT0 maximum specification is not a tested limit and should be used as a general guideline. For voltage ramp times exceeding tINIT0 MAX, please contact the factory.

Initialization After RESET (Without Voltage Ramp)

If the RESET command is issued before or after the power-up initialization sequence, the reinitialization procedure must begin at Td.

Power-Off

While powering off, CKE must be held LOW (≤0.2 × V_{DDCA}); all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.