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# Embedded LPDDR2 SDRAM

**EDB1316BD, EDB1332BD, EDB2432B4, EDB4064B4**

## Features

- Ultra low-voltage core and I/O power supplies
  - $V_{DD2} = 1.14\text{--}1.30\text{V}$
  - $V_{DDCA}/V_{DDQ} = 1.14\text{--}1.30\text{V}$
  - $V_{DD1} = 1.70\text{--}1.95\text{V}$
- Clock frequency range
  - 533–10 MHz (data rate range: 1066–20 Mb/s/pin)
- Four-bit prefetch DDR architecture
- Eight internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Per-bank refresh for concurrent operation
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock stop capability
- RoHS-compliant, “green” packaging

## Options

- Density/Page Size
  - 1Gb/2KB - single die 13
  - 2Gb/2KB - dual die 24
  - 4Gb/2KB - quad die 40
- Organization
  - x16 16
  - x32 32
  - x64 64
- $V_{DD2}$ : 1.2V B
- Revision
  - Single die D
  - Multi-die 4
- FBGA “green” package
  - 134-ball FBGA BH
  - 134-ball multi-die FBGA MA
  - 168-ball FBGA PC
  - for PoP
  - 216-ball multi-die FBGA PB
  - for PoP
- Timing – cycle time
  - 1.875ns @ RL = 8 -1D
- Operating temperature range
  - From –30°C to +85°C (Blank)
  - From –40°C to +85°C IT

## Marking

**Table 1: Key Timing Parameters**

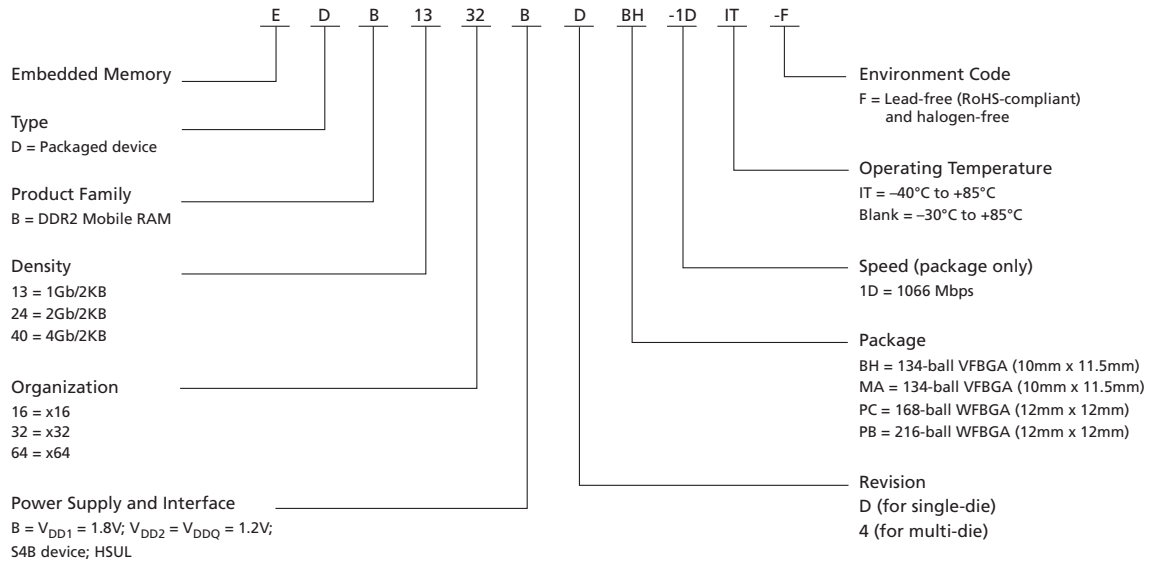
Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL
1D	533	1066	8	4

**Table 2: S4 Configuration Addressing**

Architecture	64 Meg x 16	32 Meg x 32	64 Meg x 32	64 Meg x 64
Die configuration	8 Meg x 16 x 8 banks	4 Meg x 32 x 8 banks	2 x 8 Meg x 16 x 8 banks	4 x 8 Meg x 16 x 8 banks
Row addressing	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])
Column addressing	1K (A[9:0])	512 (A[8:0])	1K (A[9:0])	1K (A[9:0])
Number of die	1	1	2	4
Die per rank	1	1	2	2
Ranks per channel <sup>1</sup>	1	1	1	2

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

**Figure 1: LPDDR2 Part Numbering**



## FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at [www.micron.com/decoder](http://www.micron.com/decoder).

**Table 3: Package Codes and Descriptions**

Package Code	Ball Count	# Ranks	# Channels	Size (mm)	Die per Package	Solder Ball Composition
BH	134	1	1	10 x 11.5 x 1.0, 0.65 pitch	SDP	SAC302
MA	134	1	1	10 x 11.5 x 1.0, 0.65 pitch	DDP	SAC302
PC	168	1	1	12 x 12 x 0.8, 0.5 pitch	SDP	SAC302
PB	216	2	2	12 x 12 x 0.8, 0.4 pitch	QDP	SAC302

- Notes: 1. SDP = single-die package; DDP = Dual-die package; QDP = Quad-die package;  
 2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).



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## General Description

The Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. The LPDDR2-S4 device is internally configured as an eight-bank DRAM. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8192 rows by 512 columns by 32 bits.

## General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

In timing diagrams, "CMD" is used as an indicator only. Actual signals occur on CA[9:0].

$V_{REF}$  indicates  $V_{REFCA}$  and  $V_{REFDQ}$ .

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

## I<sub>DD</sub> Specifications

**Table 4: I<sub>DD</sub> Specifications (32 Meg x 32)**
 $V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

Parameter	Supply	Speed Grade	Unit
		-1D	
I <sub>DD01</sub>	V <sub>DD1</sub>	6	mA
I <sub>DD02</sub>	V <sub>DD2</sub>	30	
I <sub>DD0,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD2P1</sub>	V <sub>DD1</sub>	600	μA
I <sub>DD2P2</sub>	V <sub>DD2</sub>	1600	
I <sub>DD2P,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	100	
I <sub>DD2PS1</sub>	V <sub>DD1</sub>	600	μA
I <sub>DD2PS2</sub>	V <sub>DD2</sub>	1600	
I <sub>DD2PS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	100	
I <sub>DD2N1</sub>	V <sub>DD1</sub>	0.6	mA
I <sub>DD2N2</sub>	V <sub>DD2</sub>	20	
I <sub>DD2N,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD2NS1</sub>	V <sub>DD1</sub>	0.6	mA
I <sub>DD2NS2</sub>	V <sub>DD2</sub>	12	
I <sub>DD2NS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD3P1</sub>	V <sub>DD1</sub>	1.4	mA
I <sub>DD3P2</sub>	V <sub>DD2</sub>	5	
I <sub>DD3P,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.1	
I <sub>DD3PS1</sub>	V <sub>DD1</sub>	1.4	mA
I <sub>DD3PS2</sub>	V <sub>DD2</sub>	5	
I <sub>DD3PS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.1	
I <sub>DD3N1</sub>	V <sub>DD1</sub>	1.5	mA
I <sub>DD3N2</sub>	V <sub>DD2</sub>	22	
I <sub>DD3N,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD3NS1</sub>	V <sub>DD1</sub>	1.5	mA
I <sub>DD3NS2</sub>	V <sub>DD2</sub>	14	
I <sub>DD3NS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD4R1</sub>	V <sub>DD1</sub>	2	mA
I <sub>DD4R2</sub>	V <sub>DD2</sub>	180	
I <sub>DD4R,in</sub>	V <sub>DDCA</sub>	2	
I <sub>DD4W1</sub>	V <sub>DD1</sub>	2	mA
I <sub>DD4W2</sub>	V <sub>DD2</sub>	200	
I <sub>DD4W,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	

**Table 4: I<sub>DD</sub> Specifications (32 Meg x 32) (Continued)**
 $V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

Parameter	Supply	Speed Grade	Unit
		-1D	
I <sub>DD51</sub>	V <sub>DD1</sub>	20	mA
I <sub>DD52</sub>	V <sub>DD2</sub>	70	
I <sub>DD5,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD5PB1</sub>	V <sub>DD1</sub>	2	mA
I <sub>DD5PB2</sub>	V <sub>DD2</sub>	23	
I <sub>DD5PB,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD5AB1</sub>	V <sub>DD1</sub>	2	mA
I <sub>DD5AB2</sub>	V <sub>DD2</sub>	23	
I <sub>DD5AB,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD81</sub>	V <sub>DD1</sub>	50	μA
I <sub>DD82</sub>	V <sub>DD2</sub>	50	
I <sub>DD8,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	20	

**Table 5: I<sub>DD</sub> Specifications (64 Meg x 16)**
 $V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

Parameter	Supply	Speed Grade	Unit
		-1D	
I <sub>DD01</sub>	V <sub>DD1</sub>	6	mA
I <sub>DD02</sub>	V <sub>DD2</sub>	30	
I <sub>DD0,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD2P1</sub>	V <sub>DD1</sub>	600	μA
I <sub>DD2P2</sub>	V <sub>DD2</sub>	1600	
I <sub>DD2P,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	100	
I <sub>DD2PS1</sub>	V <sub>DD1</sub>	600	μA
I <sub>DD2PS2</sub>	V <sub>DD2</sub>	1600	
I <sub>DD2PS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	100	
I <sub>DD2N1</sub>	V <sub>DD1</sub>	0.6	mA
I <sub>DD2N2</sub>	V <sub>DD2</sub>	20	
I <sub>DD2N,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD2NS1</sub>	V <sub>DD1</sub>	0.6	mA
I <sub>DD2NS2</sub>	V <sub>DD2</sub>	12	
I <sub>DD2NS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD3P1</sub>	V <sub>DD1</sub>	1.4	mA
I <sub>DD3P2</sub>	V <sub>DD2</sub>	5	
I <sub>DD3P,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.1	



**Table 5: I<sub>DD</sub> Specifications (64 Meg x 16) (Continued)**
 $V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

Parameter	Supply	Speed Grade	Unit
		-1D	
I <sub>DD3PS1</sub>	V <sub>DD1</sub>	1.4	mA
I <sub>DD3PS2</sub>	V <sub>DD2</sub>	5	
I <sub>DD3PS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.1	
I <sub>DD3N1</sub>	V <sub>DD1</sub>	1.5	mA
I <sub>DD3N2</sub>	V <sub>DD2</sub>	22	
I <sub>DD3N,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD3NS1</sub>	V <sub>DD1</sub>	1.5	mA
I <sub>DD3NS2</sub>	V <sub>DD2</sub>	14	
I <sub>DD3NS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD4R1</sub>	V <sub>DD1</sub>	2	mA
I <sub>DD4R2</sub>	V <sub>DD2</sub>	140	
I <sub>DD4R,in</sub>	V <sub>DDCA</sub>	2	
I <sub>DD4W1</sub>	V <sub>DD1</sub>	2	mA
I <sub>DD4W2</sub>	V <sub>DD2</sub>	155	
I <sub>DD4W,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD51</sub>	V <sub>DD1</sub>	20	mA
I <sub>DD52</sub>	V <sub>DD2</sub>	70	
I <sub>DD5,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD5PB1</sub>	V <sub>DD1</sub>	2	mA
I <sub>DD5PB2</sub>	V <sub>DD2</sub>	23	
I <sub>DD5PB,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD5AB1</sub>	V <sub>DD1</sub>	2	mA
I <sub>DD5AB2</sub>	V <sub>DD2</sub>	23	
I <sub>DD5AB,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	1	
I <sub>DD81</sub>	V <sub>DD1</sub>	50	μA
I <sub>DD82</sub>	V <sub>DD2</sub>	50	
I <sub>DD8,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	20	

**Table 6: I<sub>DD</sub> Specifications (64 Meg x 32, 64 Meg x 64<sup>1</sup>)**
 $V_{DD}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

Parameter	Supply	Speed Grade	Unit
		-1D	
I <sub>DD01</sub>	V <sub>DD1</sub>	12	mA
I <sub>DD02</sub>	V <sub>DD2</sub>	60	
I <sub>DD0,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	2	

**Table 6: I<sub>DD</sub> Specifications (64 Meg x 32, 64 Meg x 64<sup>1</sup>) (Continued)**
 $V_{DD}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

Parameter	Supply	Speed Grade	Unit
		-1D	
I <sub>DD2P1</sub>	V <sub>DD1</sub>	1200	μA
I <sub>DD2P2</sub>	V <sub>DD2</sub>	3200	
I <sub>DD2P,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	200	
I <sub>DD2PS1</sub>	V <sub>DD1</sub>	1200	μA
I <sub>DD2PS2</sub>	V <sub>DD2</sub>	3200	
I <sub>DD2PS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	200	
I <sub>DD2N1</sub>	V <sub>DD1</sub>	1.2	mA
I <sub>DD2N2</sub>	V <sub>DD2</sub>	40	
I <sub>DD2N,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	2	
I <sub>DD2NS1</sub>	V <sub>DD1</sub>	1.2	mA
I <sub>DD2NS2</sub>	V <sub>DD2</sub>	24	
I <sub>DD2NS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	2	
I <sub>DD3P1</sub>	V <sub>DD1</sub>	2.8	mA
I <sub>DD3P2</sub>	V <sub>DD2</sub>	10	
I <sub>DD3P,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.2	
I <sub>DD3PS1</sub>	V <sub>DD1</sub>	2.8	mA
I <sub>DD3PS2</sub>	V <sub>DD2</sub>	10	
I <sub>DD3PS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.2	
I <sub>DD3N1</sub>	V <sub>DD1</sub>	3	mA
I <sub>DD3N2</sub>	V <sub>DD2</sub>	44	
I <sub>DD3N,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	2	
I <sub>DD3NS1</sub>	V <sub>DD1</sub>	3	mA
I <sub>DD3NS2</sub>	V <sub>DD2</sub>	28	
I <sub>DD3NS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	2	
I <sub>DD4R1</sub>	V <sub>DD1</sub>	4	mA
I <sub>DD4R2</sub>	V <sub>DD2</sub>	280	
I <sub>DD4R,in</sub>	V <sub>DDCA</sub>	4	
I <sub>DD4W1</sub>	V <sub>DD1</sub>	4	mA
I <sub>DD4W2</sub>	V <sub>DD2</sub>	310	
I <sub>DD4W,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	2	
I <sub>DD51</sub>	V <sub>DD1</sub>	40	mA
I <sub>DD52</sub>	V <sub>DD2</sub>	140	
I <sub>DD5,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	2	
I <sub>DD5PB1</sub>	V <sub>DD1</sub>	4	mA
I <sub>DD5PB2</sub>	V <sub>DD2</sub>	46	
I <sub>DD5PB,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	2	

**Table 6: I<sub>DD</sub> Specifications (64 Meg x 32, 64 Meg x 64<sup>1</sup>) (Continued)**

V<sub>DD</sub>, V<sub>DDQ</sub>, V<sub>DDCA</sub> = 1.14–1.30V; V<sub>DD1</sub> = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I <sub>DD5AB1</sub>	V <sub>DD1</sub>	4	mA
I <sub>DD5AB2</sub>	V <sub>DD2</sub>	46	
I <sub>DD5AB,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	2	
I <sub>DD81</sub>	V <sub>DD1</sub>	100	μA
I <sub>DD82</sub>	V <sub>DD2</sub>	100	
I <sub>DD8,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	40	

Note: 1. Actual I<sub>DD</sub> for the 64M x 64 QDP device is dependant on the specific states in which the memory controller operates each of the two ranks. Consult Micron's Power Calculator for LPDDR2.

**Table 7: I<sub>DD6</sub> Partial-Array Self Refresh Current**

V<sub>DD2</sub>, V<sub>DDQ</sub>, V<sub>DDCA</sub> = 1.14–1.30V; V<sub>DD1</sub> = 1.70–1.95V

PASR	Supply	I <sub>DD6</sub> Partial-Array Self Refresh Current			Unit
		32 Meg x 32 64 Meg x 16	64 Meg x 32	64 Meg x 64	
Full array	V <sub>DD1</sub>	230	460	920	μA
	V <sub>DD2</sub>	700	1400	2800	
	V <sub>DDi</sub>	20	40	80	
1/2 array	V <sub>DD1</sub>	200	400	800	
	V <sub>DD2</sub>	500	1000	2000	
	V <sub>DDi</sub>	20	40	80	
1/4 array	V <sub>DD1</sub>	190	380	760	
	V <sub>DD2</sub>	400	800	1600	
	V <sub>DDi</sub>	20	40	80	
1/8 array	V <sub>DD1</sub>	185	370	740	
	V <sub>DD2</sub>	360	720	1440	
	V <sub>DDi</sub>	20	40	80	

Note: 1. LPDDR2-S4 SDRAM devices support both bank-masking and segment-masking. I<sub>DD6</sub> PASR currents are measured using bank-masking only.

Figure 2: V<sub>DD1</sub> Typical Self-Refresh Current vs. Temperature (Per Die)

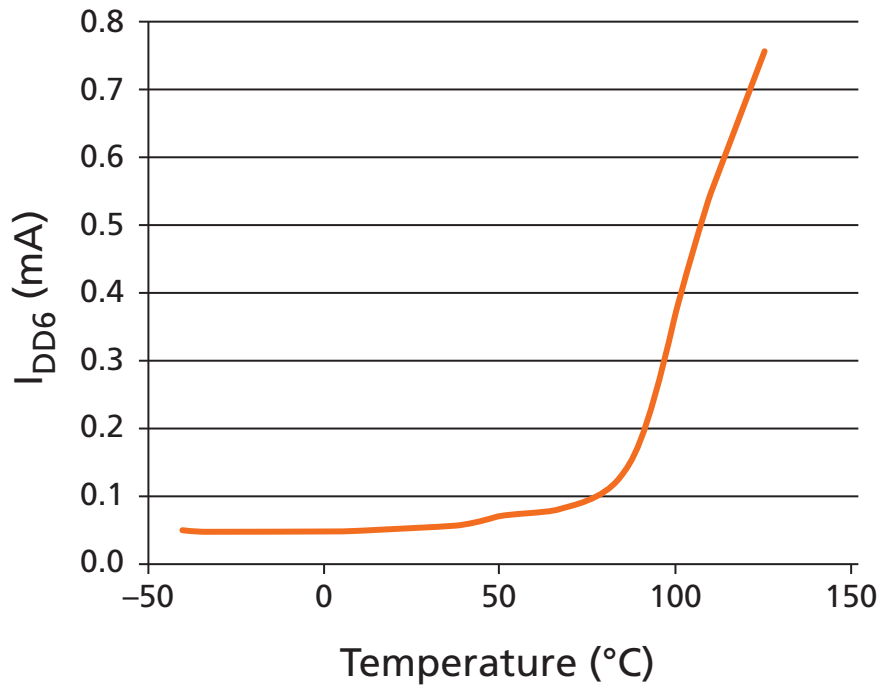
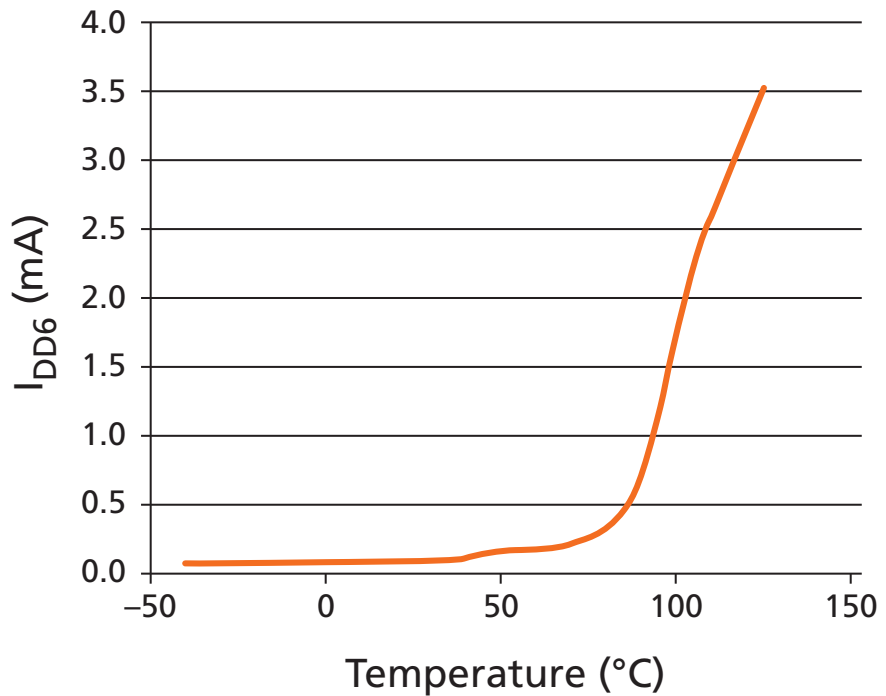


Figure 3: V<sub>DD2</sub> Typical Self-Refresh Current vs. Temperature (Per Die)





## Package Block Diagrams

Figure 4: Single Die Single Rank, Single Channel Package Block Diagram

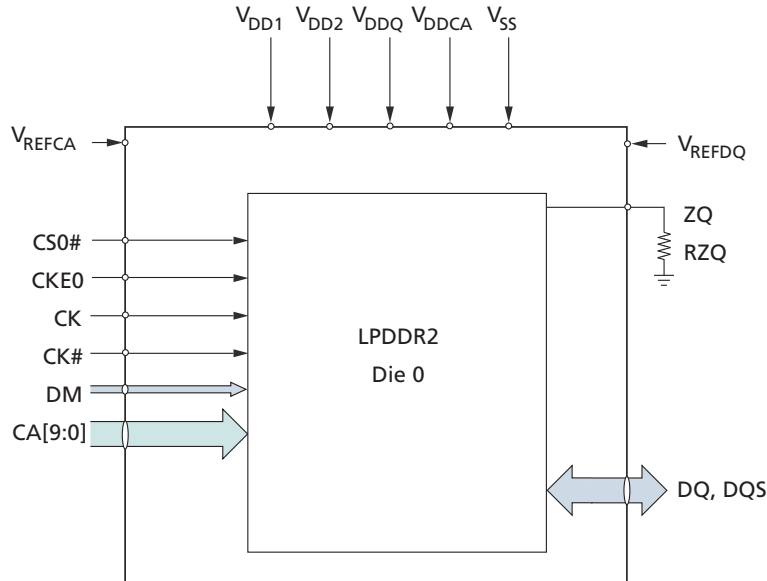
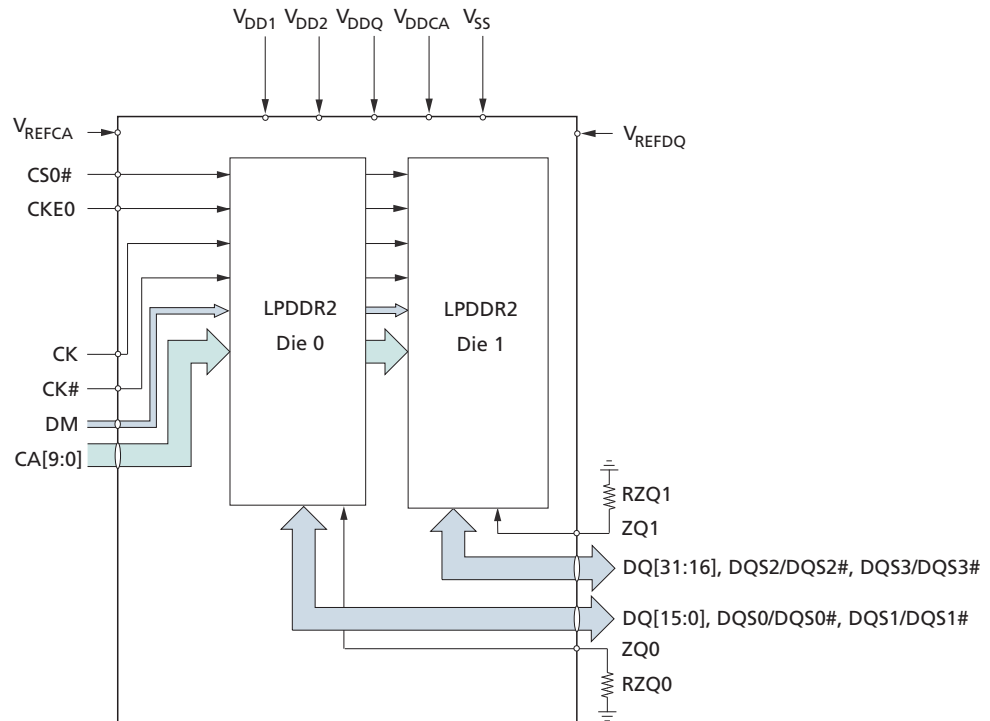
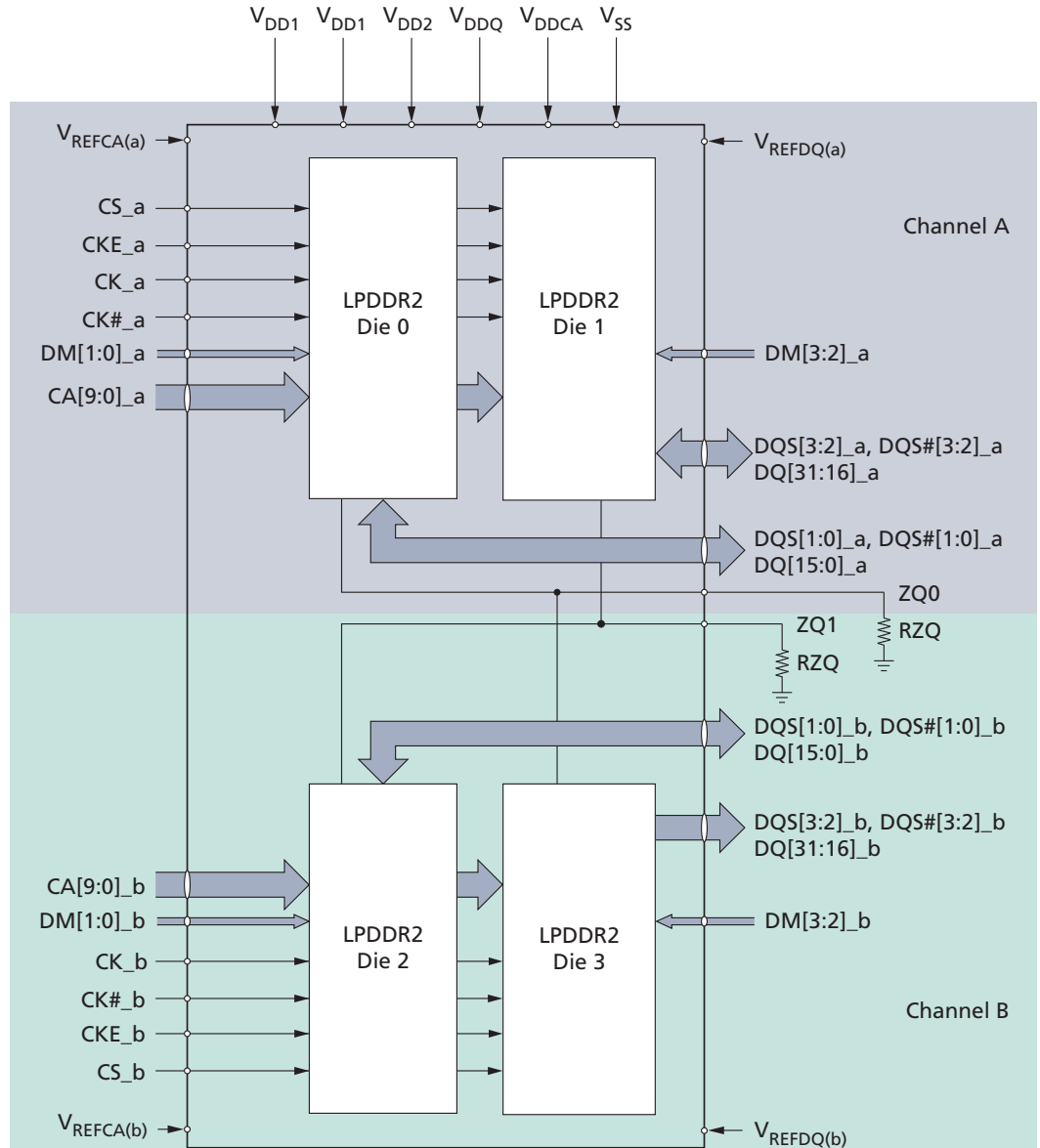


Figure 5: Dual Die Single Rank, Single Channel Package Block Diagram

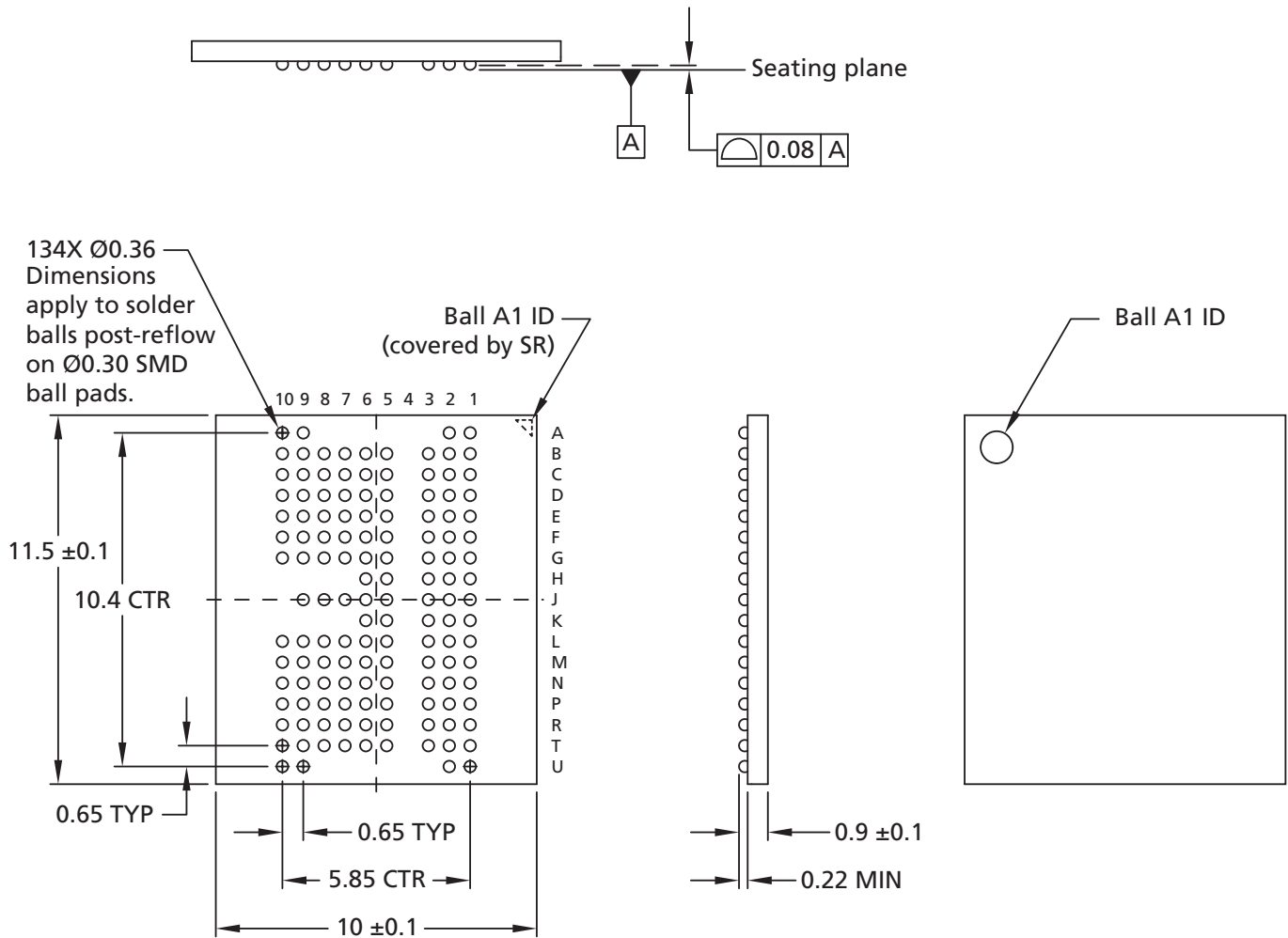


**Figure 6: Quad Die Dual Rank, Dual Channel Package Block Diagram**



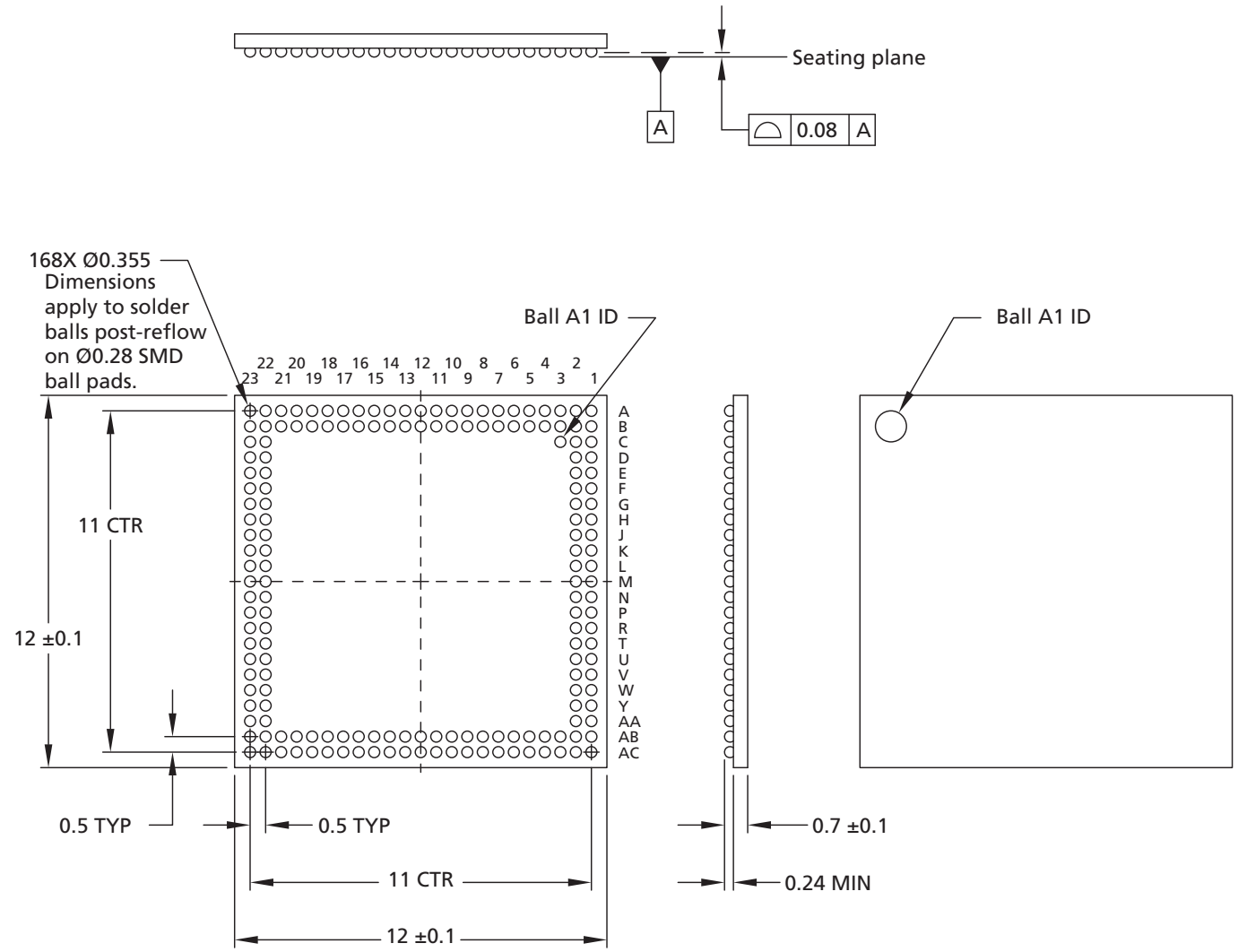
## Package Dimensions

Figure 7: 134-Ball VFBGA – 10mm x 11.5mm (Package Code: BH, MA)



Note: 1. All dimensions are in millimeters.

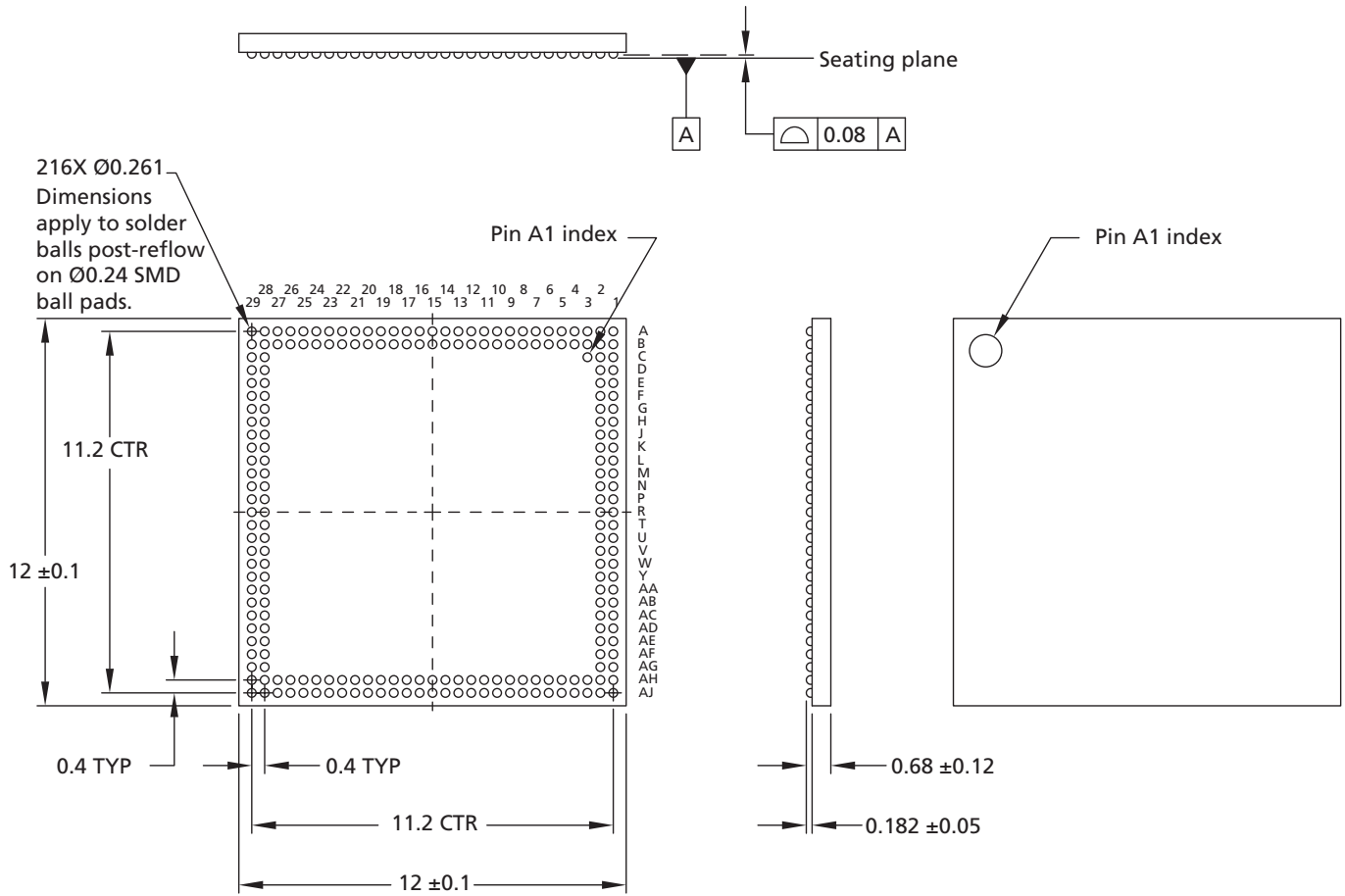
**Figure 8: 168-Ball WFBGA – 12mm x 12mm (Package Code: PC)**



Note: 1. All dimensions are in millimeters.



**Figure 9: 216-Ball WFBGA – 12mm x 12mm (Package Code: PB)**



Note: 1. All dimensions are in millimeters.

## Ball Assignments

Figure 10: 134-Ball FBGA (x16)

	1	2	3	4	5	6	7	8	9	10	
A	DNU	DNU							DNU	DNU	A
B	DNU	NC	NC		V <sub>DD2</sub>	V <sub>DD1</sub>	RFU	RFU	RFU	DNU	B
C	V <sub>DD1</sub>	V <sub>SS</sub>	RFU		V <sub>SS</sub>	V <sub>SSQ</sub>	V <sub>DDQ</sub>	RFU	V <sub>SSQ</sub>	V <sub>DDQ</sub>	C
D	V <sub>SS</sub>	V <sub>DD2</sub>	ZQ0		V <sub>DDQ</sub>	RFU	RFU	RFU	RFU	V <sub>SSQ</sub>	D
E	V <sub>SSCA</sub>	CA9	CA8		RFU	RFU	RFU	DQ15	V <sub>DDQ</sub>	V <sub>SSQ</sub>	E
F	V <sub>DDCA</sub>	CA6	CA7		V <sub>SSQ</sub>	DQ11	DQ13	DQ14	DQ12	V <sub>DDQ</sub>	F
G	V <sub>DD2</sub>	CA5	V <sub>REFCA</sub>		DQS1#	DQS1	DQ10	DQ9	DQ8	V <sub>SSQ</sub>	G
H	V <sub>DDCA</sub>	V <sub>SS</sub>	CK#		DM1	V <sub>DDQ</sub>					H
J	V <sub>SSCA</sub>	NC	CK		V <sub>SSQ</sub>	V <sub>DDQ</sub>	V <sub>DD2</sub>	V <sub>SS</sub>	V <sub>REFDQ</sub>		J
K	CKE0	RFU	RFU		DM0	V <sub>DDQ</sub>					K
L	CS0#	RFU	RFU		DQS0#	DQS0	DQ5	DQ6	DQ7	V <sub>SSQ</sub>	L
M	CA4	CA3	CA2		V <sub>SSQ</sub>	DQ4	DQ2	DQ1	DQ3	V <sub>DDQ</sub>	M
N	V <sub>SSCA</sub>	V <sub>DDCA</sub>	CA1		RFU	RFU	RFU	DQ0	V <sub>DDQ</sub>	V <sub>SSQ</sub>	N
P	V <sub>SS</sub>	V <sub>DD2</sub>	CA0		V <sub>DDQ</sub>	RFU	RFU	RFU	RFU	V <sub>SSQ</sub>	P
R	V <sub>DD1</sub>	V <sub>SS</sub>	NC		V <sub>SS</sub>	V <sub>SSQ</sub>	V <sub>DDQ</sub>	RFU	V <sub>SSQ</sub>	V <sub>DDQ</sub>	R
T	DNU	NC	NC		V <sub>DD2</sub>	V <sub>DD1</sub>	RFU	RFU	RFU	DNU	T
U	DNU	DNU							DNU	DNU	U

Top View (ball down)

Note: 1. V<sub>DDCA</sub> is unnecessary. F1, H1, and N2 pins should be left unconnected.

**Figure 11: 134-Ball FBGA (x32)**

	1	2	3	4	5	6	7	8	9	10	
A	DNU	DNU							DNU	DNU	A
B	DNU	NC	NC		V <sub>DD2</sub>	V <sub>DD1</sub>	DQ31	DQ29	DQ26	DNU	B
C	V <sub>DD1</sub>	V <sub>SS</sub>	ZQ1		V <sub>SS</sub>	V <sub>SSQ</sub>	V <sub>DDQ</sub>	DQ25	V <sub>SSQ</sub>	V <sub>DDQ</sub>	C
D	V <sub>SS</sub>	V <sub>DD2</sub>	ZQ0		V <sub>DDQ</sub>	DQ30	DQ27	DQ53	DQ53#	V <sub>SSQ</sub>	D
E	V <sub>SSCA</sub>	CA9	CA8		DQ28	DQ24	DM3	DQ15	V <sub>DDQ</sub>	V <sub>SSQ</sub>	E
F	V <sub>DDCA</sub>	CA6	CA7		V <sub>SSQ</sub>	DQ11	DQ13	DQ14	DQ12	V <sub>DDQ</sub>	F
G	V <sub>DD2</sub>	CA5	V <sub>REFCA</sub>		DQS1#	DQ51	DQ10	DQ9	DQ8	V <sub>SSQ</sub>	G
H	V <sub>DDCA</sub>	V <sub>SS</sub>	CK#		DM1	V <sub>DDQ</sub>					H
J	V <sub>SSCA</sub>	NC	CK		V <sub>SSQ</sub>	V <sub>DDQ</sub>	V <sub>DD2</sub>	V <sub>SS</sub>	V <sub>REFDQ</sub>		J
K	CKE0	RFU	RFU		DM0	V <sub>DDQ</sub>					K
L	CS0#	RFU	RFU		DQS0#	DQS0	DQ5	DQ6	DQ7	V <sub>SSQ</sub>	L
M	CA4	CA3	CA2		V <sub>SSQ</sub>	DQ4	DQ2	DQ1	DQ3	V <sub>DDQ</sub>	M
N	V <sub>SSCA</sub>	V <sub>DDCA</sub>	CA1		DQ19	DQ23	DM2	DQ0	V <sub>DDQ</sub>	V <sub>SSQ</sub>	N
P	V <sub>SS</sub>	V <sub>DD2</sub>	CA0		V <sub>DDQ</sub>	DQ17	DQ20	DQ52	DQ52#	V <sub>SSQ</sub>	P
R	V <sub>DD1</sub>	V <sub>SS</sub>	NC		V <sub>SS</sub>	V <sub>SSQ</sub>	V <sub>DDQ</sub>	DQ22	V <sub>SSQ</sub>	V <sub>DDQ</sub>	R
T	DNU	NC	NC		V <sub>DD2</sub>	V <sub>DD1</sub>	DQ16	DQ18	DQ21	DNU	T
U	DNU	DNU							DNU	DNU	U

Top View (ball down)

- Notes:
1. V<sub>DDCA</sub> is unnecessary. F1, H1, and N2 pins should be left unconnected.
  2. C3 pin is RFU for 32 Meg x 32 and ZQ1 for 64 Meg x 32.

**Figure 12: 168-Ball FBGA**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	118	19	20	21	22	23	
A	DNU	DNU	NC	NC	NC	(NC) <sup>2</sup>	NC	NC	(NC) <sup>2</sup>	NC	V <sub>DD1</sub>	V <sub>SSQ</sub>	DQ30	DQ29	V <sub>SSQ</sub>	DQ26	DQ25	V <sub>SSQ</sub>	DQS#3	V <sub>DD1</sub>	V <sub>SS</sub>	DNU	DNU	A
B	DNU	DNU	V <sub>DD1</sub>	NC	NC	NC	NC	NC	NC	V <sub>SS</sub>	V <sub>DD2</sub>	DQ31	V <sub>DDQ</sub>	DQ28	DQ27	V <sub>DDQ</sub>	DQ24	DQS3	V <sub>DDQ</sub>	DM3	V <sub>DD2</sub>	DNU	DNU	B
C	V <sub>SS</sub>	V <sub>DD2</sub>																				DQ15	V <sub>SSQ</sub>	C
D	NC	NC																				V <sub>DDQ</sub>	DQ14	D
E	NC	NC																				DQ12	DQ13	E
F	(NC) <sup>2</sup>	NC																				DQ11	V <sub>SSQ</sub>	F
G	NC	NC																				V <sub>DDQ</sub>	DQ10	G
H	NC	NC																				DQ8	DQ9	H
J	(NC) <sup>2</sup>	NC																				DQS1	V <sub>SSQ</sub>	J
K	NC	NC																				V <sub>DDQ</sub>	DQS#1	K
L	NC	NC																				V <sub>DD2</sub>	DM1	L
M	NC	V <sub>SS</sub>																				V <sub>REFDQ</sub>	V <sub>SS</sub>	M
N	NC	V <sub>DD1</sub>																				V <sub>DD1</sub>	DM0	N
P	ZQ	V <sub>REFCA</sub>																				DQS#0	V <sub>SSQ</sub>	P
R	V <sub>SS</sub>	V <sub>DD2</sub>																				V <sub>DDQ</sub>	DQ50	R
T	CA9	CA8																				DQ6	DQ7	T
U	CA7	V <sub>DDCA</sub>																				DQ5	V <sub>SSQ</sub>	U
V	V <sub>SSCA</sub>	CA6																				V <sub>DDQ</sub>	DQ4	V
W	CA5	V <sub>DDCA</sub>																				DQ2	DQ3	W
Y	CK#	CK																				DQ1	V <sub>SSQ</sub>	Y
AA	V <sub>SS</sub>	V <sub>DD2</sub>																				V <sub>DDQ</sub>	DQ0	AA
AB	DNU	DNU	CS0#	RFU	V <sub>DD1</sub>	CA1	V <sub>SSCA</sub>	CA3	CA4	V <sub>DD2</sub>	V <sub>SS</sub>	DQ16	V <sub>DDQ</sub>	DQ18	DQ20	V <sub>DDQ</sub>	DQ22	DQS2	V <sub>DDQ</sub>	DM2	V <sub>DD2</sub>	DNU	DNU	AB
AC	DNU	DNU	CKE0	RFU	V <sub>SS</sub>	CA0	CA2	V <sub>DDCA</sub>	V <sub>SS</sub> <sup>1</sup>	(NC) <sup>2</sup>	NC	V <sub>SSQ</sub>	DQ17	DQ19	V <sub>SSQ</sub>	DQ21	DQ23	V <sub>SSQ</sub>	DQS#2	V <sub>DD1</sub>	V <sub>SS</sub>	DNU	DNU	AC

Top View (ball down)

LPDDR2    
  Supply    
  Ground

- Notes:
- Ball AC9 may be V<sub>SS</sub> or left unconnected.
  - Balls labeled "(NC)" = no connect; however, they can be connected together internally.
  - V<sub>DDCA</sub> is unnecessary. U2, W2, and AC8 pins should be left unconnected.



**Figure 13: 216-Ball FBGA**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	DNU	V <sub>SS</sub>	V <sub>DD2</sub>	DQ30	DQ29	V <sub>SSQ</sub>	DQ26	DQ25	V <sub>SSQ</sub>	DQ5#3	V <sub>SSQ</sub>	DQ14	DQ13	V <sub>SS</sub>	V <sub>DD1</sub>	V <sub>DD2</sub>	DQ11	DQ10	DQ9	DQ51	DM1	V <sub>DDQ</sub>	DQ50	DQ7	DQ6	DQ4	DQ3	V <sub>SS</sub>	DNU	A
B	V <sub>SSQ</sub>	NC	DQ31	V <sub>DDQ</sub>	DQ28	DQ27	V <sub>DDQ</sub>	DQ24	V <sub>DDQ</sub>	DQ53	DM3	DQ15	V <sub>DDQ</sub>	V <sub>SSQ</sub>	V <sub>REFDQ</sub>	V <sub>DD2</sub>	DQ12	V <sub>DDQ</sub>	DQ8	DQ5#1	V <sub>SSQ</sub>	DM0	DQ5#0	V <sub>SSQ</sub>	V <sub>DDQ</sub>	DQ5	DQ2	NC	V <sub>SSQ</sub>	B
C	V <sub>DD1</sub>	DQ16																										V <sub>DD1</sub>	V <sub>DD2</sub>	C
D	DQ17	V <sub>DDQ</sub>																										DQ1	V <sub>DDQ</sub>	D
E	DQ18	DQ19																										V <sub>SSQ</sub>	DQ0	E
F	V <sub>SSQ</sub>	DQ20																										DM2	V <sub>DDQ</sub>	F
G	DQ21	V <sub>DDQ</sub>																										DQ52	DQ5#2	G
H	DQ22	DQ23																										V <sub>SSQ</sub>	DQ23	H
J	V <sub>SSQ</sub>	V <sub>DDQ</sub>																										V <sub>DDQ</sub>	DQ22	J
K	DQ5#2	DQ52																										DQ20	DQ21	K
L	DM2	DQ0																										DQ19	V <sub>SSQ</sub>	L
M	DQ1	V <sub>SSQ</sub>																										V <sub>DDQ</sub>	DQ18	M
N	DQ2	V <sub>DD1</sub>																										DQ16	DQ17	N
P	V <sub>SS</sub>	V <sub>SS</sub>																										V <sub>DD2</sub>	V <sub>DD1</sub>	P
R	V <sub>DD1</sub>	V <sub>REFDQ</sub>																										V <sub>SS</sub>	CA0	R
T	V <sub>DD2</sub>	V <sub>DD2</sub>																										V <sub>DDCA</sub>	CA1	T
U	V <sub>DDQ</sub>	DQ3																										V <sub>REFCA</sub>	CA2	U
V	DQ4	V <sub>SSQ</sub>																										V <sub>SSCA</sub>	CA3	V
W	DQ6	DQ5																										CA4	NC	W
Y	V <sub>DDQ</sub>	DQ7																										CS0#	NC	Y
AA	DQ50	DQ5#0																										V <sub>SSCA</sub>	CKE0	AA
AB	DM0	V <sub>SSQ</sub>																										CK	CK#	AB
AC	V <sub>DDQ</sub>	DM1																										V <sub>DDCA</sub>	CA5	AC
AD	DQ5#1	DQ51																										CA7	CA6	AD
AE	DQ8	V <sub>SSQ</sub>																										CA8	V <sub>DDCA</sub>	AE
AF	DQ9	V <sub>DDQ</sub>																										V <sub>SSCA</sub>	CA9	AF
AG	DQ10	DQ11																										V <sub>DD2</sub>	ZQ	AG
AH	V <sub>SSQ</sub>	V <sub>DD1</sub>	V <sub>DD2</sub>	DQ13	V <sub>SSQ</sub>	DQ15	DM3	DQ53	V <sub>DDQ</sub>	DQ26	DQ27	V <sub>DDQ</sub>	DQ30	V <sub>SSQ</sub>	V <sub>DD2</sub>	V <sub>REFCA</sub>	CA9	V <sub>SSCA</sub>	CA7	CA6	CK#	V <sub>DDCA</sub>	CKE0	CS0#	CA3	CA2	CA1	V <sub>DD1</sub>	V <sub>SSCA</sub>	AH
AJ	DNU	V <sub>SS</sub>	DQ12	V <sub>DDQ</sub>	DQ14	V <sub>DDQ</sub>	V <sub>SSQ</sub>	DQ5#3	DQ24	DQ25	V <sub>SSQ</sub>	DQ28	DQ29	DQ31	V <sub>DD1</sub>	V <sub>SS</sub>	ZQ	CAB	V <sub>DDCA</sub>	CA5	CK	V <sub>SSCA</sub>	NC	NC	CA4	V <sub>DDCA</sub>	CA0	V <sub>SS</sub>	DNU	AJ

Top View (ball down)

Channel A
  Channel B
  Supply
  Ground

Note: 1. V<sub>DDCA</sub> is unnecessary. T28, AC28, AE29, AH22, AJ19, and AJ26 pins should be left unconnected.

## Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See Ball Assignments for information specific to this device.

**Table 8: Ball/Pad Descriptions**

Symbol	Type	Description
CA[9:0]	Input	<b>Command/address inputs:</b> Provide the command and address inputs according to the command truth table.
CK, CK#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE[1:0]	Input	<b>Clock enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK.
CS[1:0]#	Input	<b>Chip select:</b> CS# is considered part of the command code and is sampled at the rising edge of CK.
DM[3:0]	Input	<b>Input data mask:</b> DM is an input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[31:0]	I/O	<b>Data input/output:</b> Bidirectional data bus.
DQS[3:0], DQS[3:0]#	I/O	<b>Data strobe:</b> The data strobe is bidirectional (used for read and write data) and complementary (DQS and DQS#). It is edge-aligned output with read data and centered input with write data. DQS[3:0]/DQS[3:0]# is DQS for each of the four data bytes, respectively.
V <sub>DDQ</sub>	Supply	<b>DQ power supply:</b> Isolated on the die for improved noise immunity.
V <sub>SSQ</sub>	Supply	<b>DQ ground:</b> Isolated on the die for improved noise immunity.
V <sub>DDCA</sub>	Supply	<b>Command/address power supply:</b> Command/address power supply.
V <sub>SSCA</sub>	Supply	<b>Command/address ground:</b> Isolated on the die for improved noise immunity.
V <sub>DD1</sub>	Supply	<b>Core power:</b> Supply 1.
V <sub>DD2</sub>	Supply	<b>Core power:</b> Supply 2.
V <sub>SS</sub>	Supply	<b>Common ground</b>
V <sub>REFCA</sub> , V <sub>REFDQ</sub>	Supply	<b>Reference voltage:</b> V <sub>REFCA</sub> is reference for command/address input buffers, V <sub>REFDQ</sub> is reference for DQ input buffers.
ZQ	Reference	<b>External impedance (240 ohm):</b> This signal is used to calibrate the device output impedance.
RFU	–	<b>Reserved for future use:</b> Must be left floating.
DNU	–	<b>Do not use:</b> Must be grounded or left floating.
NC	–	<b>No connect:</b> Not internally connected.
(NC)	–	<b>No connect:</b> Balls indicated as (NC) are no connects, however, they could be connected together internally.