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Embedded LPDDR2 SDRAM

EDB1316BD, EDB1332BD, EDB2432B4, EDB4064B4

Features

- Ultra low-voltage core and I/O power supplies
  - V_{DD2} = 1.14–1.30V
  - V_{DDCA}/V_{DDQ} = 1.14–1.30V
  - V_{DD1} = 1.70–1.95V
- Clock frequency range
  - 533–10 MHz (data rate range: 1066–20 Mb/s/pin)
- Four-bit prefetch DDR architecture
- Eight internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Per-bank refresh for concurrent operation
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock stop capability
- RoHS-compliant, “green” packaging

Options / Marking

Options	Marking
• Density/Page Size	
– 1Gb/2KB - single die	13
– 2Gb/2KB - dual die	24
– 4Gb/2KB - quad die	40
• Organization	
– x16	16
– x32	32
– x64	64
• V_{DD2}: 1.2V	B
• Revision	
– Single die	D
– Multi-die	4
• FBGA “green” package	
– 134-ball FBGA	BH
– 134-ball multi-die FBGA	MA
– 168-ball FBGA for PoP	PC
– 216-ball multi-die FBGA for PoP	PB
• Timing – cycle time	
– 1.875ns @ RL = 8	-1D
• Operating temperature range	
– From –30°C to +85°C	(Blank)
– From –40°C to +85°C	IT

Table 1: Key Timing Parameters

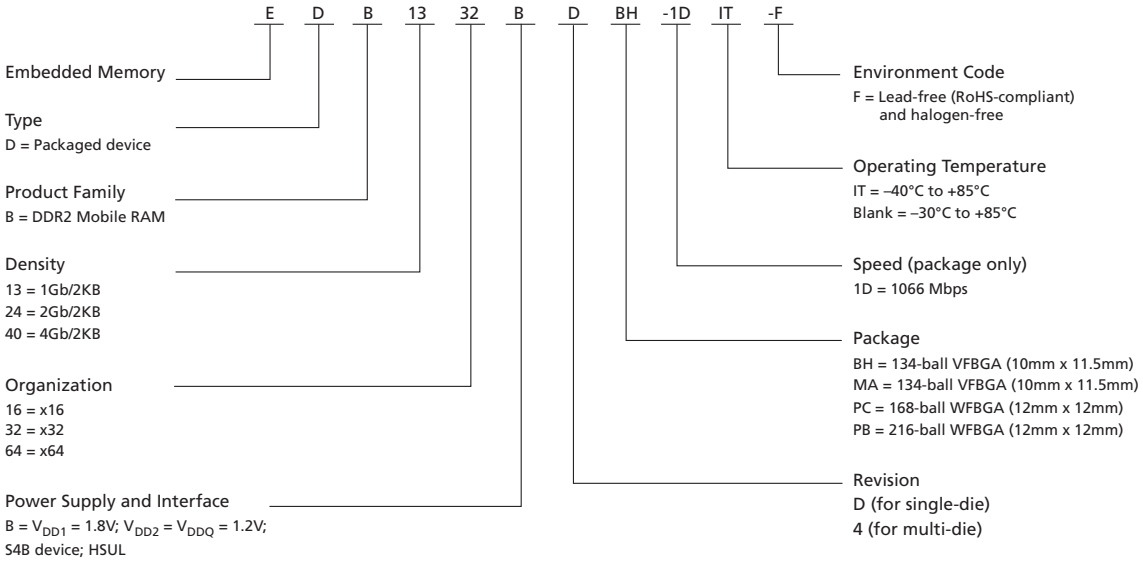
Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL
1D	533	1066	8	4

Table 2: S4 Configuration Addressing

Architecture	64 Meg x 16	32 Meg x 32	64 Meg x 32	64 Meg x 64
Die configuration	8 Meg x 16 x 8 banks	4 Meg x 32 x 8 banks	2 x 8 Meg x 16 x 8 banks	4 x 8 Meg x 16 x 8 banks
Row addressing	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])
Column addressing	1K (A[9:0])	512 (A[8:0])	1K (A[9:0])	1K (A[9:0])
Number of die	1	1	2	4
Die per rank	1	1	2	2
Ranks per channel[1]	1	1	1	2

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

Figure 1: LPDDR2 Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Table 3: Package Codes and Descriptions

Package Code	Ball Count	# Ranks	# Channels	Size (mm)	Die per Package	Solder Ball Composition
BH	134	1	1	10 x 11.5 x 1.0, 0.65 pitch	SDP	SAC302
MA	134	1	1	10 x 11.5 x 1.0, 0.65 pitch	DDP	SAC302
PC	168	1	1	12 x 12 x 0.8, 0.5 pitch	SDP	SAC302
PB	216	2	2	12 x 12 x 0.8, 0.4 pitch	QDP	SAC302

Notes: 1. SDP = single-die package; DDP = Dual-die package; QDP = Quad-die package;.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

Contents

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List of Tables

General Description

The Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. The LPDDR2-S4 device is internally configured as an eight-bank DRAM. Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1024 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8192 rows by 512 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

In timing diagrams, "CMD" is used as an indicator only. Actual signals occur on CA[9:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ}.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

I_{DD} Specifications

Table 4: I_{DD} Specifications (32 Meg x 32)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD01}	V_{DD1}	6	mA
I_{DD02}	V_{DD2}	30	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2P1}	V_{DD1}	600	µA
I_{DD2P2}	V_{DD2}	1600	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2PS1}	V_{DD1}	600	µA
I_{DD2PS2}	V_{DD2}	1600	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2N1}	V_{DD1}	0.6	mA
I_{DD2N2}	V_{DD2}	20	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2NS1}	V_{DD1}	0.6	mA
I_{DD2NS2}	V_{DD2}	12	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3P1}	V_{DD1}	1.4	mA
I_{DD3P2}	V_{DD2}	5	
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3PS1}	V_{DD1}	1.4	mA
I_{DD3PS2}	V_{DD2}	5	
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3N1}	V_{DD1}	1.5	mA
I_{DD3N2}	V_{DD2}	22	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3NS1}	V_{DD1}	1.5	mA
I_{DD3NS2}	V_{DD2}	14	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD4R1}	V_{DD1}	2	mA
I_{DD4R2}	V_{DD2}	180	
$I_{DD4R,in}$	V_{DDCA}	2	
I_{DD4W1}	V_{DD1}	2	mA
I_{DD4W2}	V_{DD2}	200	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	1	

Table 4: I_{DD} Specifications (32 Meg x 32) (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD51}	V_{DD1}	20	mA
I_{DD52}	V_{DD2}	70	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5PB1}	V_{DD1}	2	mA
I_{DD5PB2}	V_{DD2}	23	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5AB1}	V_{DD1}	2	mA
I_{DD5AB2}	V_{DD2}	23	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD81}	V_{DD1}	50	µA
I_{DD82}	V_{DD2}	50	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	20	

Table 5: I_{DD} Specifications (64 Meg x 16)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD01}	V_{DD1}	6	mA
I_{DD02}	V_{DD2}	30	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2P1}	V_{DD1}	600	µA
I_{DD2P2}	V_{DD2}	1600	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2PS1}	V_{DD1}	600	µA
I_{DD2PS2}	V_{DD2}	1600	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	100	
I_{DD2N1}	V_{DD1}	0.6	mA
I_{DD2N2}	V_{DD2}	20	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2NS1}	V_{DD1}	0.6	mA
I_{DD2NS2}	V_{DD2}	12	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3P1}	V_{DD1}	1.4	mA
I_{DD3P2}	V_{DD2}	5	
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.1	

Table 5: I_{DD} Specifications (64 Meg x 16) (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD3PS1}	V_{DD1}	1.4	mA
I_{DD3PS2}	V_{DD2}	5	
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3N1}	V_{DD1}	1.5	mA
I_{DD3N2}	V_{DD2}	22	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3NS1}	V_{DD1}	1.5	mA
I_{DD3NS2}	V_{DD2}	14	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD4R1}	V_{DD1}	2	mA
I_{DD4R2}	V_{DD2}	140	
$I_{DD4R,in}$	V_{DDCA}	2	
I_{DD4W1}	V_{DD1}	2	mA
I_{DD4W2}	V_{DD2}	155	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD51}	V_{DD1}	20	mA
I_{DD52}	V_{DD2}	70	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5PB1}	V_{DD1}	2	mA
I_{DD5PB2}	V_{DD2}	23	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5AB1}	V_{DD1}	2	mA
I_{DD5AB2}	V_{DD2}	23	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD81}	V_{DD1}	50	µA
I_{DD82}	V_{DD2}	50	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	20	

Table 6: I_{DD} Specifications (64 Meg x 32, 64 Meg x 64[1])

V_{DD}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD01}	V_{DD1}	12	mA
I_{DD02}	V_{DD2}	60	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	2	

Table 6: I_{DD} Specifications (64 Meg x 32, 64 Meg x 64[1]) (Continued)

V_{DD}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD2P1}	V_{DD1}	1200	µA
I_{DD2P2}	V_{DD2}	3200	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	200	
I_{DD2PS1}	V_{DD1}	1200	µA
I_{DD2PS2}	V_{DD2}	3200	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	200	
I_{DD2N1}	V_{DD1}	1.2	mA
I_{DD2N2}	V_{DD2}	40	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD2NS1}	V_{DD1}	1.2	mA
I_{DD2NS2}	V_{DD2}	24	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD3P1}	V_{DD1}	2.8	mA
I_{DD3P2}	V_{DD2}	10	
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.2	
I_{DD3PS1}	V_{DD1}	2.8	mA
I_{DD3PS2}	V_{DD2}	10	
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.2	
I_{DD3N1}	V_{DD1}	3	mA
I_{DD3N2}	V_{DD2}	44	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD3NS1}	V_{DD1}	3	mA
I_{DD3NS2}	V_{DD2}	28	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD4R1}	V_{DD1}	4	mA
I_{DD4R2}	V_{DD2}	280	
$I_{DD4R,in}$	V_{DDCA}	4	
I_{DD4W1}	V_{DD1}	4	mA
I_{DD4W2}	V_{DD2}	310	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD51}	V_{DD1}	40	mA
I_{DD52}	V_{DD2}	140	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD5PB1}	V_{DD1}	4	mA
I_{DD5PB2}	V_{DD2}	46	
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	2	

Table 6: I_{DD} Specifications (64 Meg x 32, 64 Meg x 64[1]) (Continued)

V_{DD}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD5AB1}	V_{DD1}	4	mA
I_{DD5AB2}	V_{DD2}	46	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	2	
I_{DD81}	V_{DD1}	100	µA
I_{DD82}	V_{DD2}	100	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	40	

Note: 1. Actual I_{DD} for the 64M x 64 QDP device is dependant on the specific states in which the memory controller operates each of the two ranks. Consult Micron's Power Calculator for LPDDR2.

Table 7: I_{DD6} Partial-Array Self Refresh Current

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	I_{DD6} Partial-Array Self Refresh Current			Unit
		32 Meg x 32 64 Meg x 16	64 Meg x 32	64 Meg x 64	
Full array	V_{DD1}	230	460	920	µA
	V_{DD2}	700	1400	2800	
	V_{DDi}	20	40	80	
1/2 array	V_{DD1}	200	400	800	
	V_{DD2}	500	1000	2000	
	V_{DDi}	20	40	80	
1/4 array	V_{DD1}	190	380	760	
	V_{DD2}	400	800	1600	
	V_{DDi}	20	40	80	
1/8 array	V_{DD1}	185	370	740	
	V_{DD2}	360	720	1440	
	V_{DDi}	20	40	80	

Note: 1. LPDDR2-S4 SDRAM devices support both bank-masking and segment-masking. I_{DD6} PASR currents are measured using bank-masking only.

Figure 2: V_{DD1}Typical Self-Refresh Current vs. Temperature (Per Die)

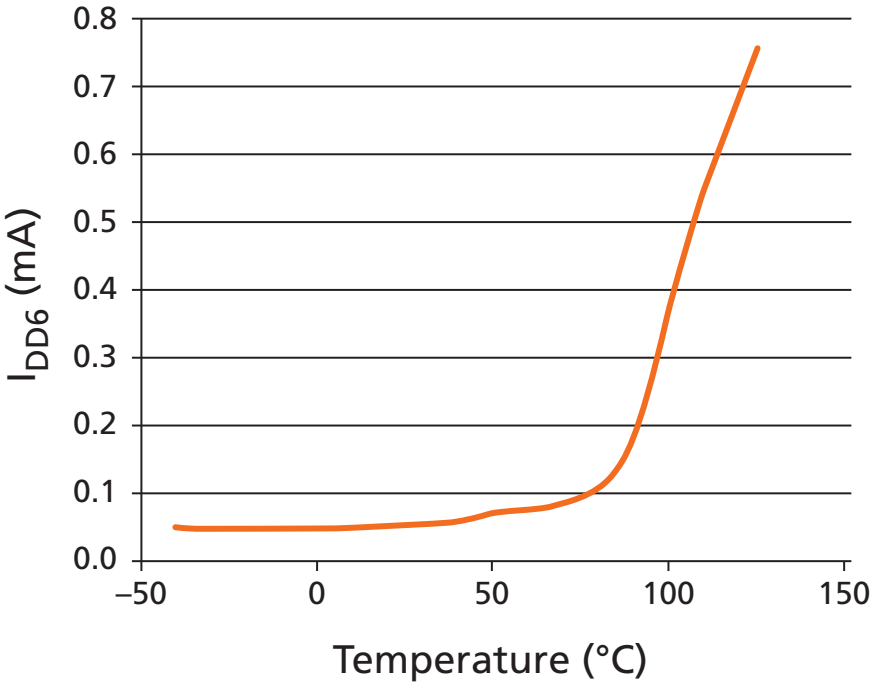
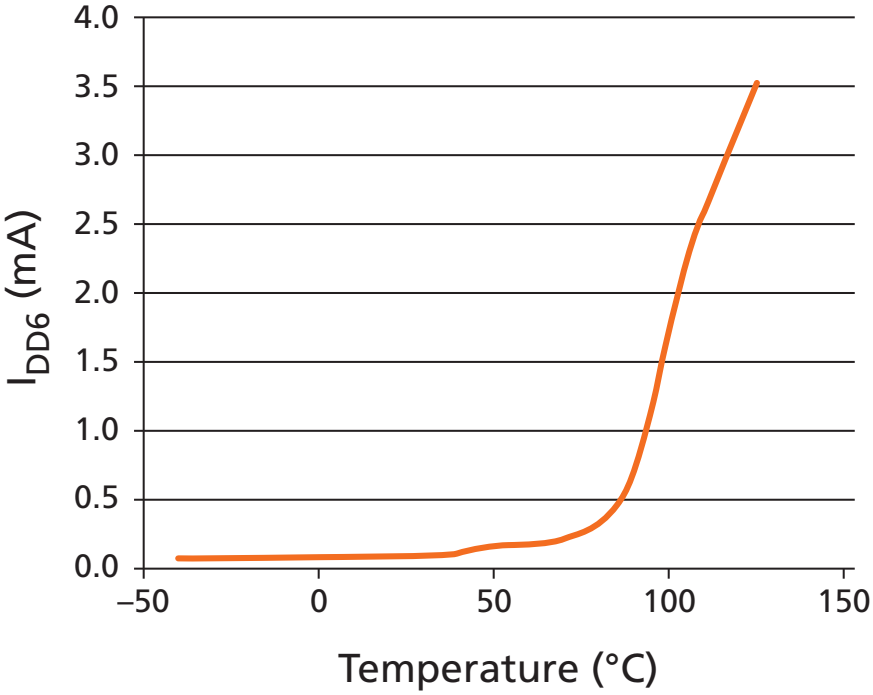


Figure 3: V_{DD2} Typical Self-Refresh Current vs. Temperature (Per Die)



Package Block Diagrams

Figure 4: Single Die Single Rank, Single Channel Package Block Diagram

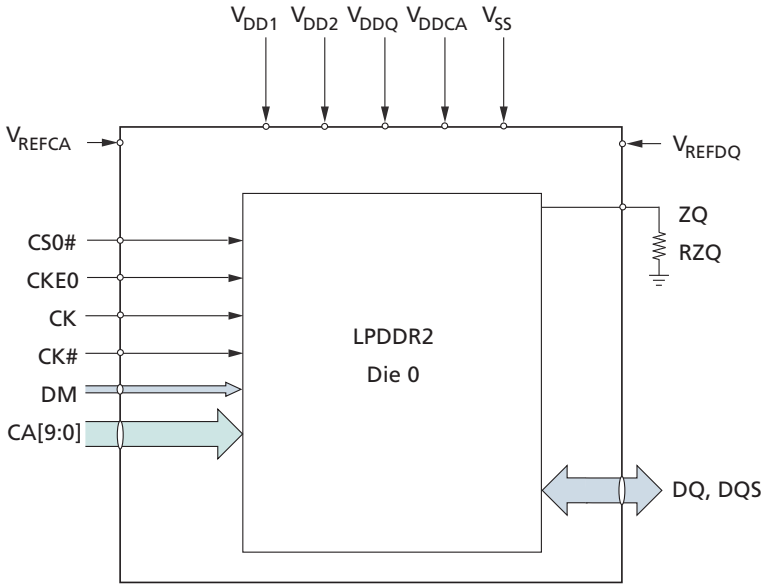


Figure 5: Dual Die Single Rank, Single Channel Package Block Diagram

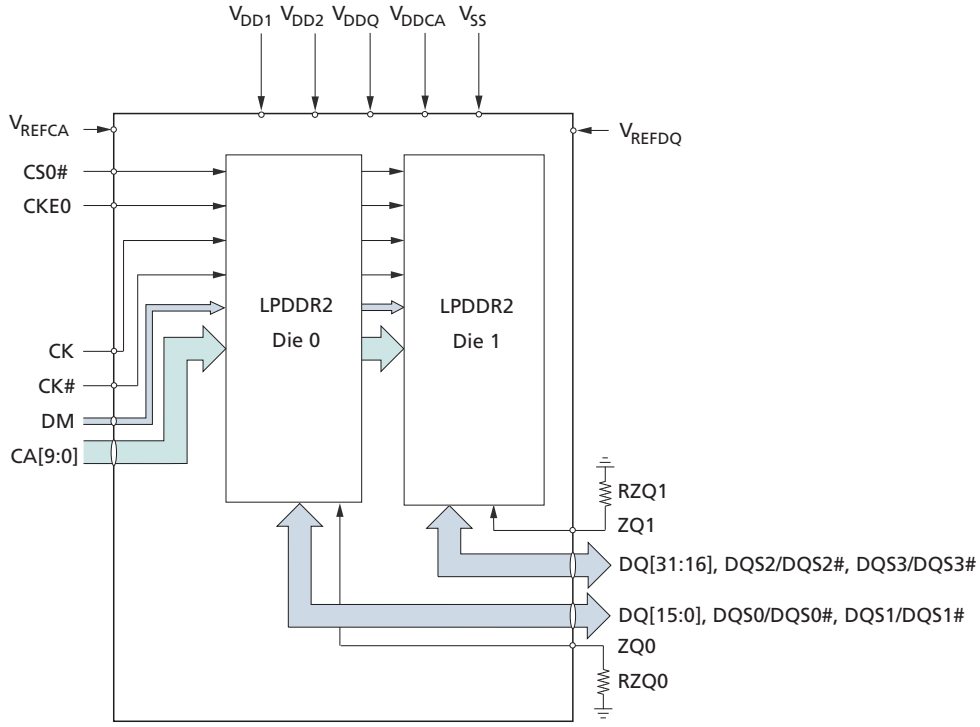
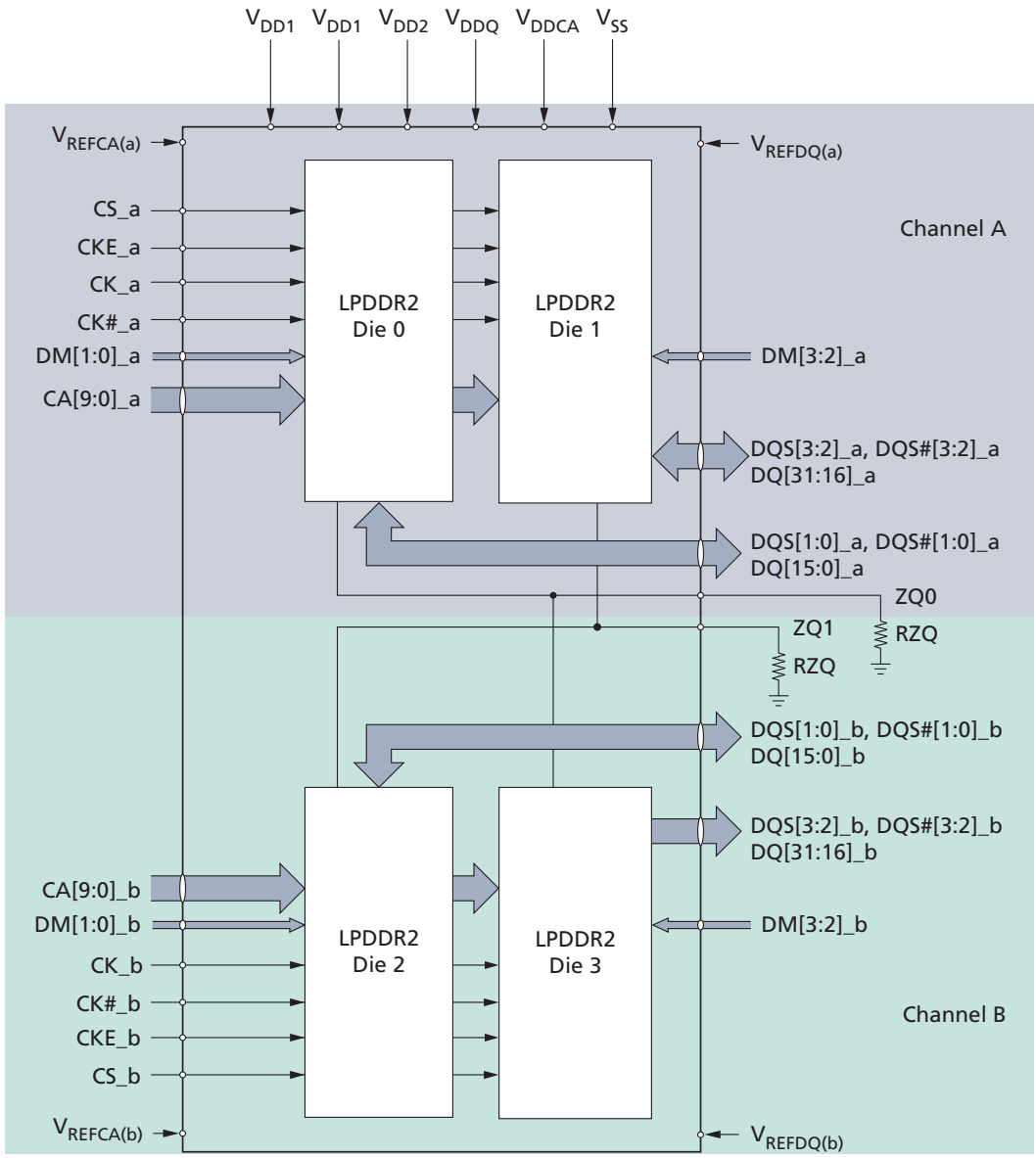
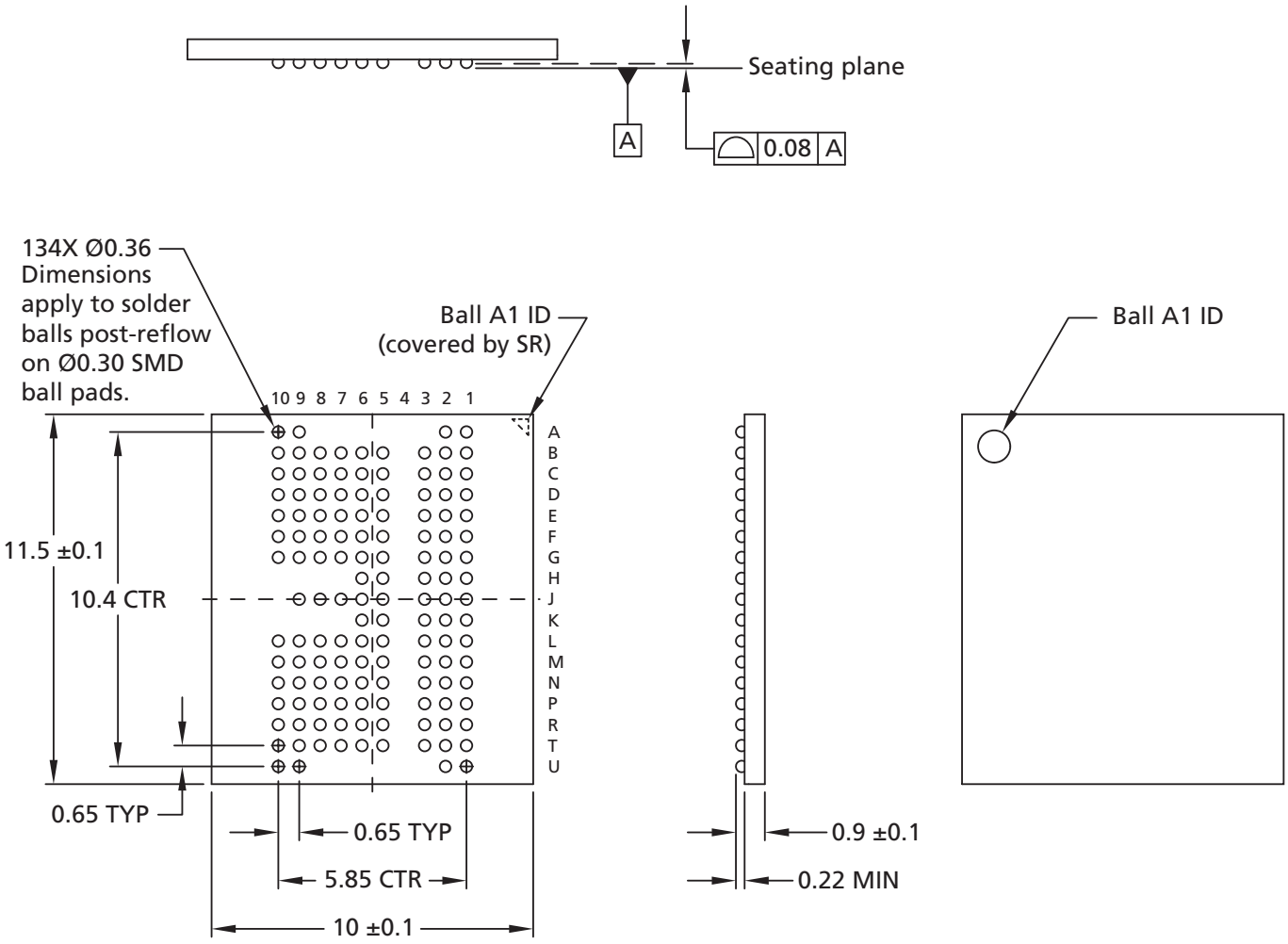


Figure 6: Quad Die Dual Rank, Dual Channel Package Block Diagram



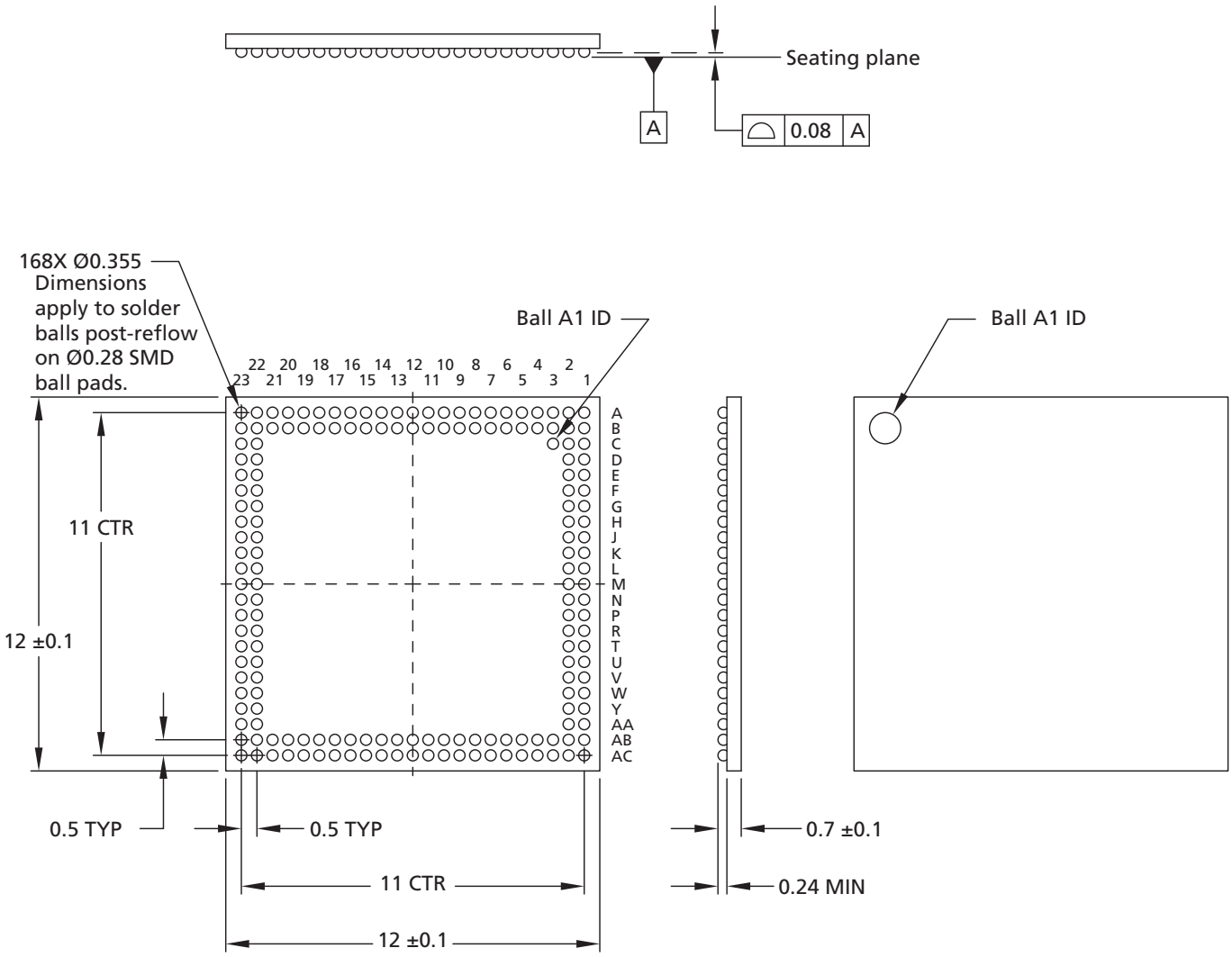
Package Dimensions

Figure 7: 134-Ball VFBGA – 10mm x 11.5mm (Package Code: BH, MA)



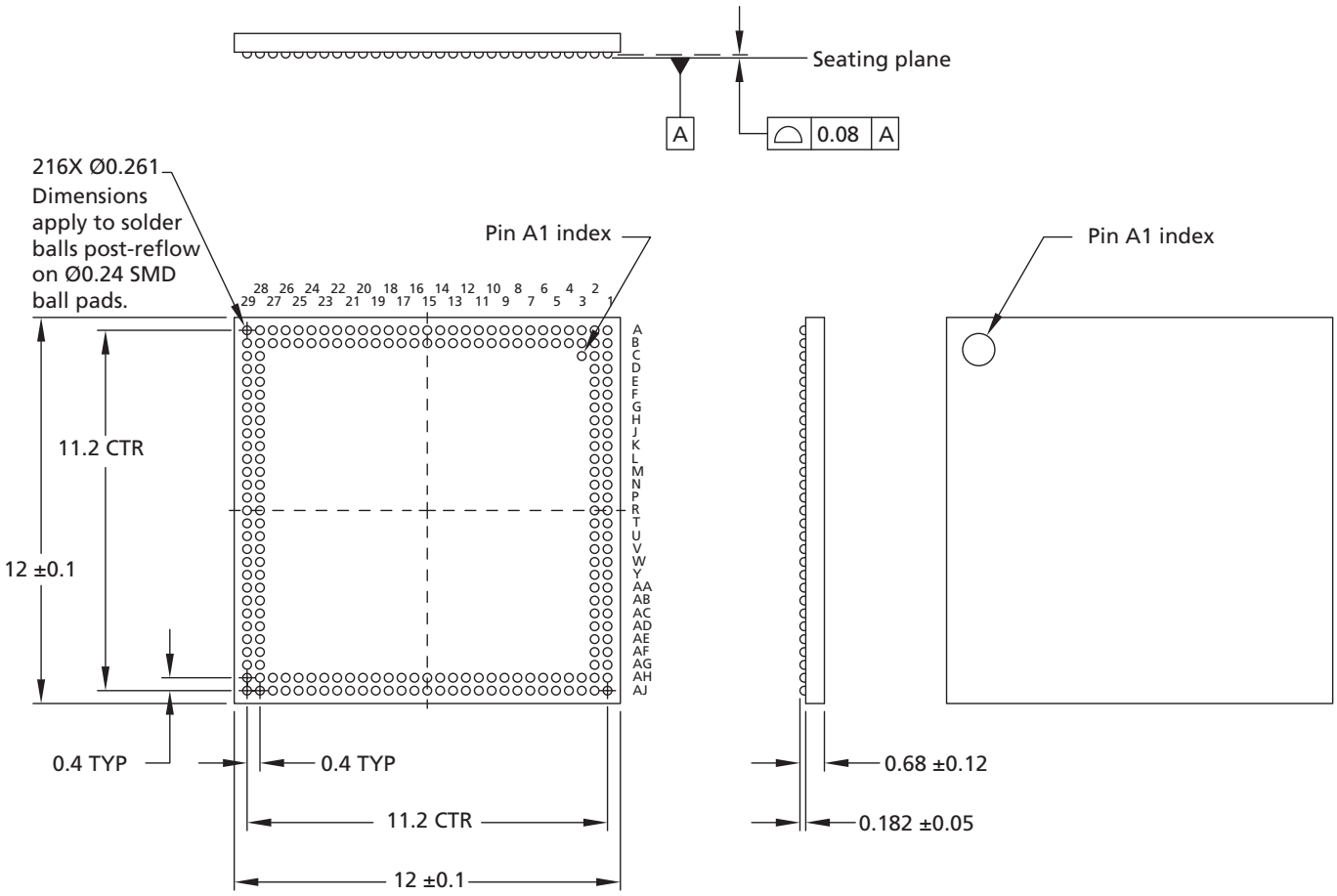
Note: 1. All dimensions are in millimeters.

Figure 8: 168-Ball WFBGA – 12mm x 12mm (Package Code: PC)



Note: 1. All dimensions are in millimeters.

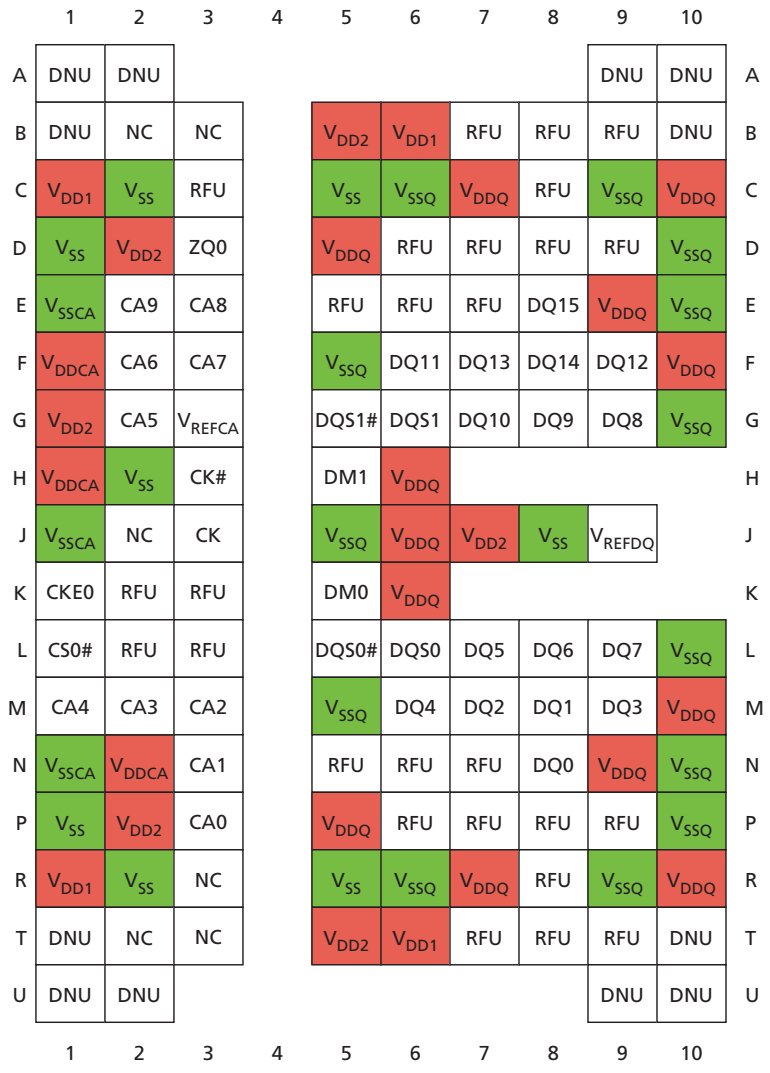
Figure 9: 216-Ball WFBGA – 12mm x 12mm (Package Code: PB)



Note: 1. All dimensions are in millimeters.

Ball Assignments

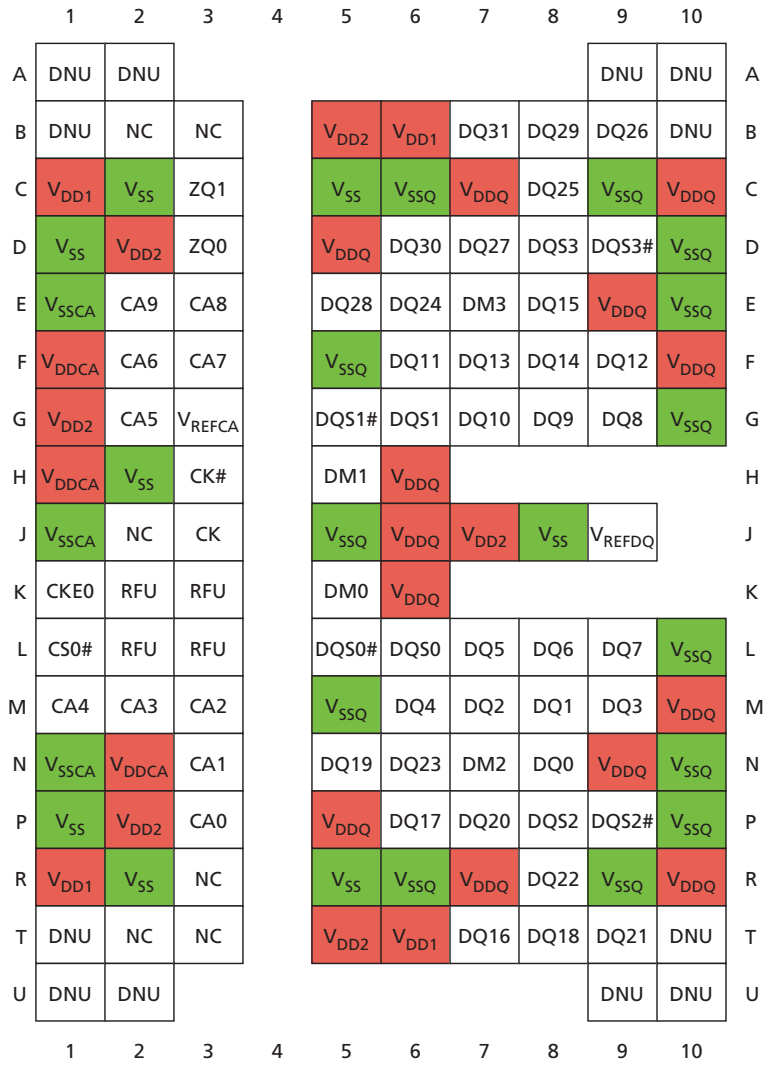
Figure 10: 134-Ball FBGA (x16)



Top View (ball down)

Note: 1. V_{DDCA} is unnecessary. F1, H1, and N2 pins should be left unconnected.

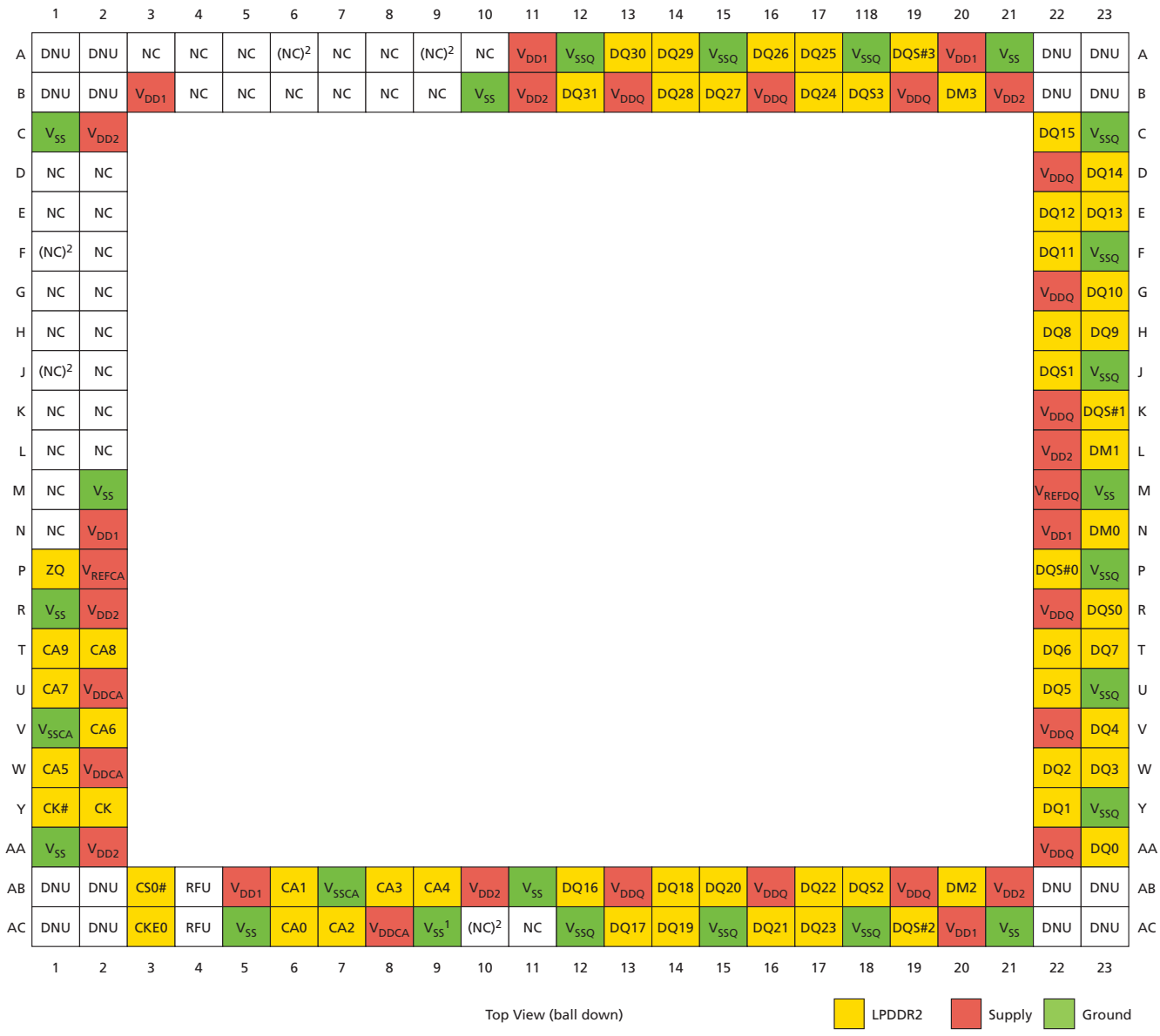
Figure 11: 134-Ball FBGA (x32)



Top View (ball down)

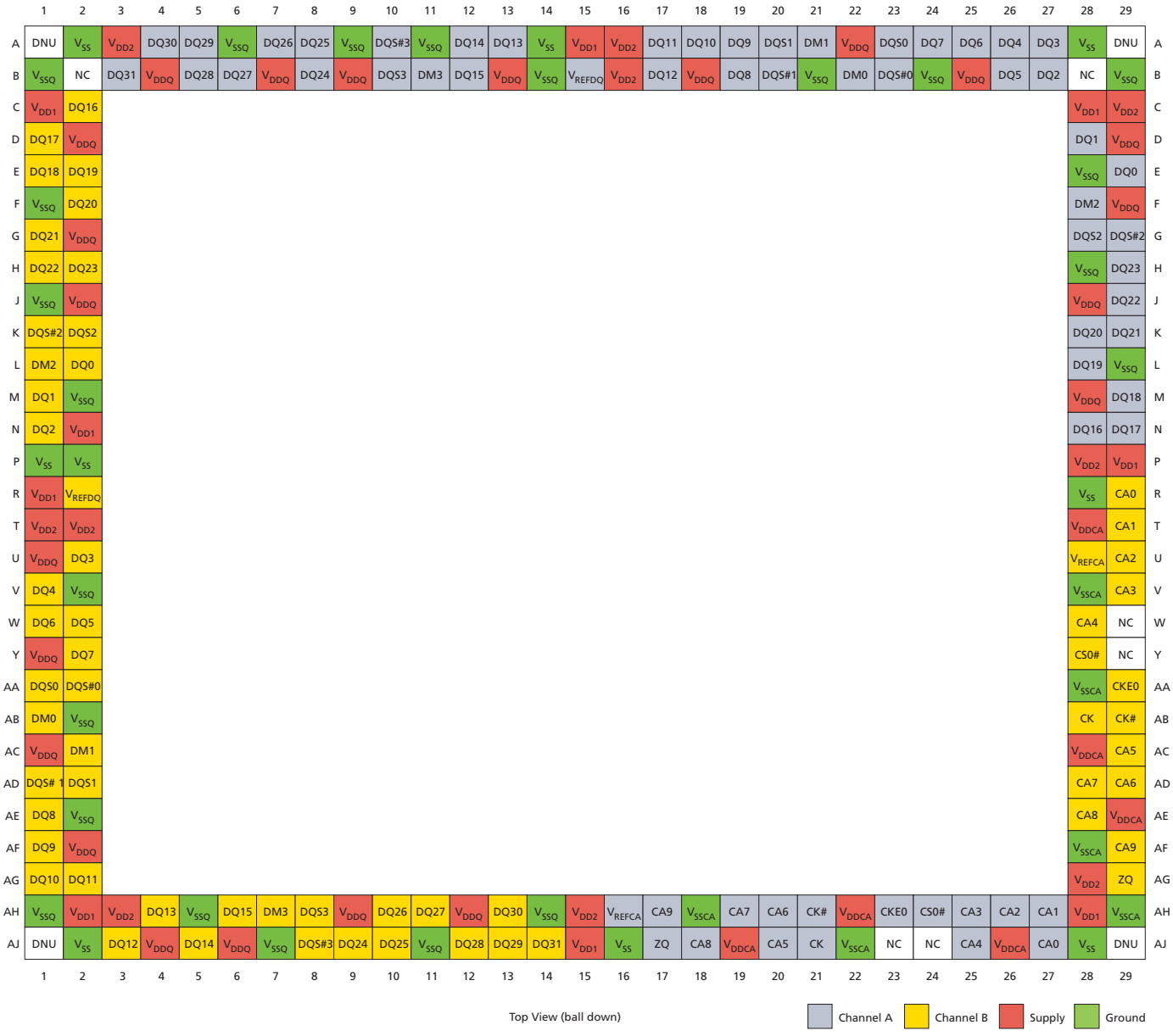
Notes: 1. V_{DDCA} is unnecessary. F1, H1, and N2 pins should be left unconnected.
2. C3 pin is RFU for 32 Meg x 32 and ZQ1 for 64 Meg x 32.

Figure 12: 168-Ball FBGA



Notes:
1. Ball AC9 may be V_{SS} or left unconnected.
2. Balls labeled "(NC)" = no connect; however, they can be connected together internally.
3. V_{DDCA} is unnecessary. U2, W2, and AC8 pins should be left unconnected.

Figure 13: 216-Ball FBGA



Note: 1. V_{DDCA} is unnecessary. T28, AC28, AE29, AH22, AJ19, and AJ26 pins should be left unconnected.

Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See Ball Assignments for information specific to this device.

Table 8: Ball/Pad Descriptions

Symbol	Type	Description
CA[9:0]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE[1:0]	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK.
CS[1:0]#	Input	**Chip select:** CS# is considered part of the command code and is sampled at the rising edge of CK.
DM[3:0]	Input	**Input data mask:** DM is an input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[31:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[3:0], DQS[3:0]#	I/O	**Data strobe:** The data strobe is bidirectional (used for read and write data) and complementary (DQS and DQS#). It is edge-aligned output with read data and centered input with write data. DQS[3:0]/DQS[3:0]# is DQS for each of the four data bytes, respectively.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
V_{DDCA}	Supply	**Command/address power supply:** Command/address power supply.
V_{SSCA}	Supply	**Command/address ground:** Isolated on the die for improved noise immunity.
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{SS}	Supply	**Common ground**
V_{REFCA}, V_{REFDQ}	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers.
ZQ	Reference	**External impedance (240 ohm):** This signal is used to calibrate the device output impedance.
RFU	–	**Reserved for future use:** Must be left floating.
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.
(NC)	–	**No connect:** Balls indicated as (NC) are no connects, however, they could be connected together internally.