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Automotive Mobile LPDDR2 SDRAM

EDB5432BEBH, EDB5432BEPA

Features[1]

- Ultra low-voltage core and I/O power supplies
  - V_{DD2} = 1.14–1.30V
  - V_{DDCA}/V_{DDQ} = 1.14–1.30V
  - V_{DD1} = 1.70–1.95V
- Clock frequency range
  - 533–10 MHz (data rate range: 1066–20 Mb/s/pin)
- Four-bit prefetch DDR architecture
- Four internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on every CK edge
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)[2]
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock stop capability
- RoHS-compliant, "green" packaging

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL	^{t}RCD/^{t}RP
-1D	533	1066	8	4	Typical

Options — Marking

- V_{DD2}: 1.2V — B
- Density/Page Size
  - 512Mb/2KB - single die — 54
- Organization
  - x32 — 32
- FBGA "green" package
  - 134-ball VFBGA (10mm x 11.5mm) — BH
  - 168-ball WFBGA (12mm x 12mm) — PA
- Timing – cycle time
  - 1.875ns @ RL = 8 — -1D
- Special options
  - Standard — None
  - Automotive certified (Package-level burn-in) — A
- Operating temperature range
  - From –40°C to +85°C — IT
  - From –40°C to +105°C — AT
  - From –40°C to +125°C[3] — UT
- Revision — :E

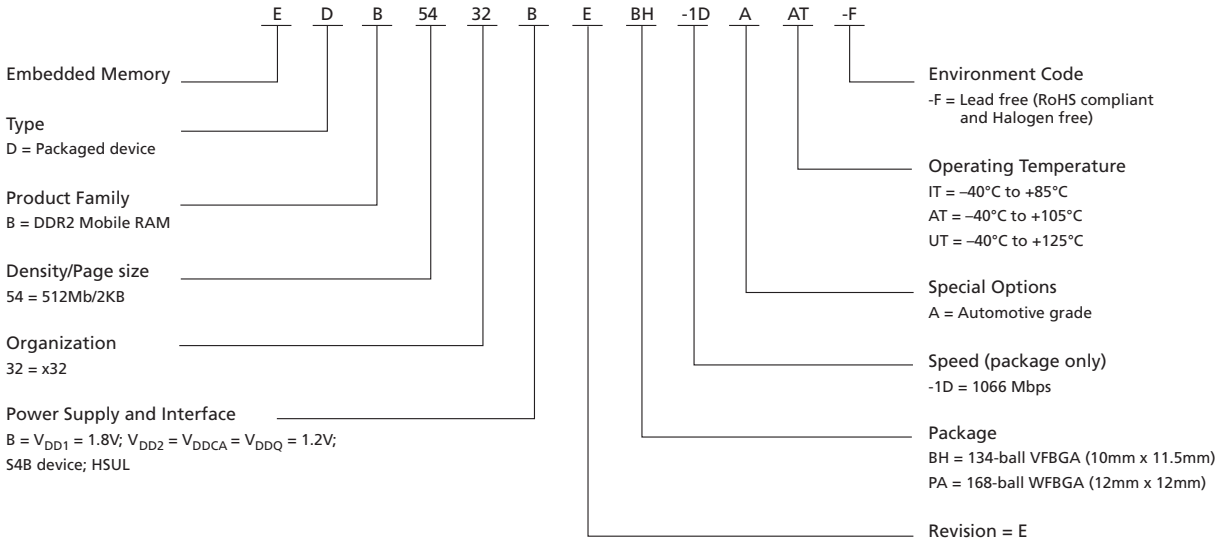
Notes:
1. All items related to 8-bank in this data sheet are not available. For example per-bank refresh option is not supported.
2. When T_C > 105°C, self-refresh mode is not available.
3. UT option use based on automotive usage model. Please contact Micron sales representative if you have questions.

Table 2: Single Channel S4 Configuration Addressing

Architecture	16 Meg x 32
Die configuration	4 Meg x 32 x 4 banks
Row addressing	8K (A[12:0])
Column addressing	512 (A[8:0])
Number of die	1
Die per rank	1
Ranks per channel[1]	1

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

Figure 1: 512Mb LPDDR2 Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Table 3: Package Codes and Descriptions

Package Code	Ball Count	# Ranks	# Channels	Size (mm)	Die per Package	Solder Ball Composition
BH	134	1	1	10 x 11.5 x 1.0, 0.65 pitch	SDP	SAC302
PA	168	1	1	12 x 12 x 0.8, 0.5 pitch	SDP	SAC302

Notes: 1. SDP = Single-die package.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

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General Description

The 512Mb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. The LPDDR2-S4 device is internally configured as an four-bank DRAM. Each of the x32's 134,217,728-bit banks is organized as 8192 rows by 512 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS, DQS# and CK, CK# respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

In timing diagrams, "CMD" is used as an indicator only. Actual signals occur on CA[9:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ}.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

I_{DD} Specifications

Table 4: 16 Meg x 32 I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD01}	V_{DD1}	6	mA
I_{DD02}	V_{DD2}	30	
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2P1}	V_{DD1}	0.6	mA
I_{DD2P2}	V_{DD2}	1.6	
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD2PS1}	V_{DD1}	0.6	mA
I_{DD2PS2}	V_{DD2}	1.6	
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD2N1}	V_{DD1}	0.6	mA
I_{DD2N2}	V_{DD2}	20	
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD2NS1}	V_{DD1}	0.6	mA
I_{DD2NS2}	V_{DD2}	12	
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3P1}	V_{DD1}	1.4	mA
I_{DD3P2}	V_{DD2}	5	
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3PS1}	V_{DD1}	1.4	mA
I_{DD3PS2}	V_{DD2}	5	
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.1	
I_{DD3N1}	V_{DD1}	1.5	mA
I_{DD3N2}	V_{DD2}	22	
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD3NS1}	V_{DD1}	1.5	mA
I_{DD3NS2}	V_{DD2}	14	
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD4R1}	V_{DD1}	2	mA
I_{DD4R2}	V_{DD2}	180	
$I_{DD4R,in}$	V_{DDCA}	2	
I_{DD4W1}	V_{DD1}	2	mA
I_{DD4W2}	V_{DD2}	200	
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	1	

Table 4: 16 Meg x 32 I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

Parameter	Supply	Speed Grade	Unit
		-1D	
I_{DD51}	V_{DD1}	20	mA
I_{DD52}	V_{DD2}	70	
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD5AB1}	V_{DD1}	2	mA
I_{DD5AB2}	V_{DD2}	23	
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	1	
I_{DD61}	V_{DD1}	–	See Table 5
I_{DD62}	V_{DD2}	–	
$I_{DD6,in}$	V_{DDCA} + V_{DDQ}	–	
I_{DD81}	V_{DD1}	0.05	mA
I_{DD82}	V_{DD2}	0.05	
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	0.02	

Table 5: I_{DD6} Partial-Array Self Refresh Current

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value (-40˚C to +85˚C)	Value (+85˚C to +105˚C)	Value (+105˚C to +125˚C)	Unit
Full array	V_{DD1}	230	2100	–	µA
	V_{DD2}	700	4400	–	
	V_{DDi}	20	20	–	
1/2 array	V_{DD1}	200	2000	–	
	V_{DD2}	500	2900	–	
	V_{DDi}	20	20	–	
1/4 array	V_{DD1}	190	1800	–	
	V_{DD2}	400	2000	–	
	V_{DDi}	20	20	–	
1/8 array	V_{DD1}	185	1700	–	
	V_{DD2}	360	1800	–	
	V_{DDi}	20	20	–	

Notes:
1. LPDDR2-S4 SDRAM devices support both bank-masking and segment-masking. I_{DD6} PASR currents are measured using bank-masking only.
2. When T_C > 105°C: self-refresh mode is not available.

Figure 2: V_{DD1}Typical Self-Refresh Current vs. Temperature

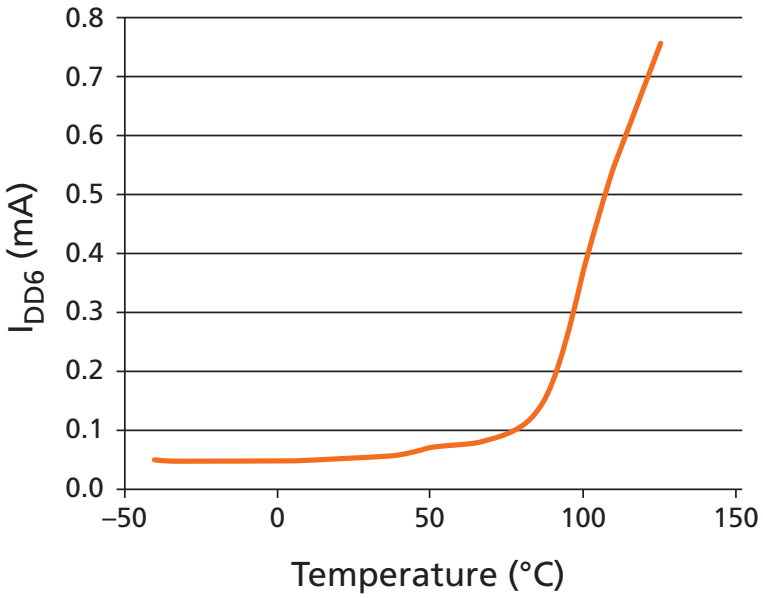
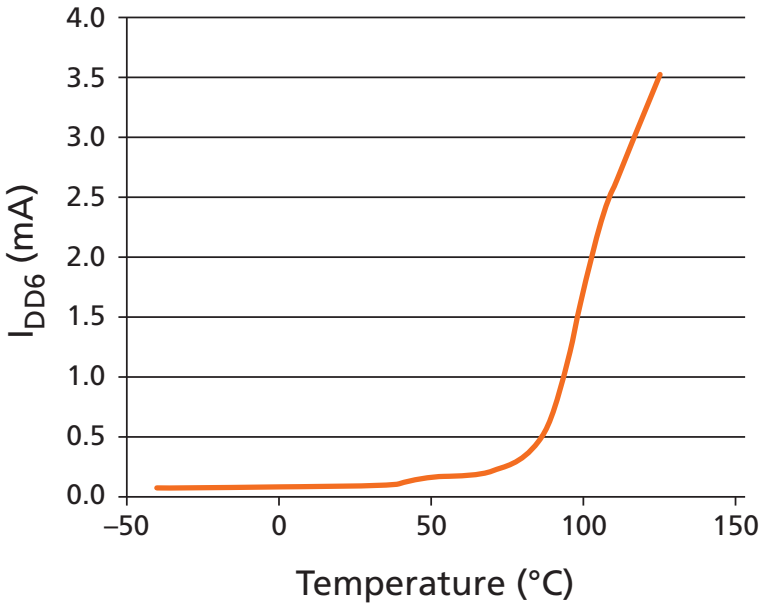
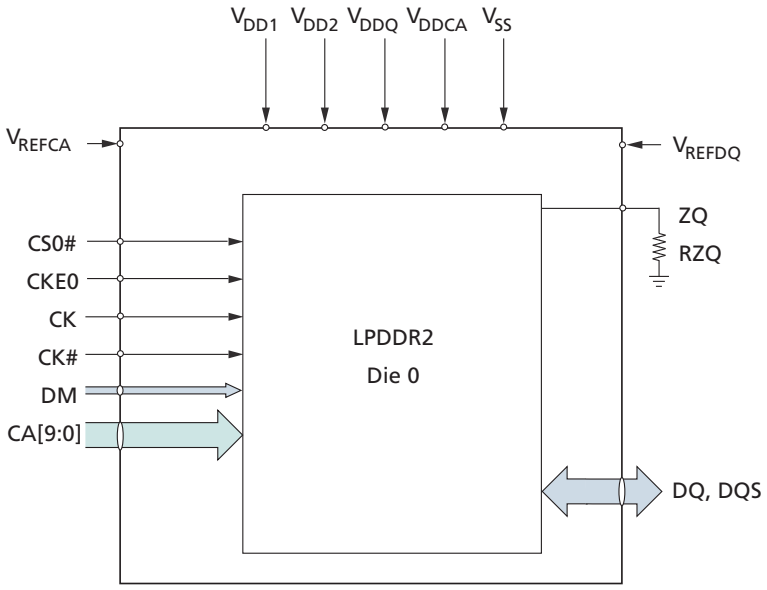


Figure 3: V_{DD2} Typical Self-Refresh Current vs. Temperature



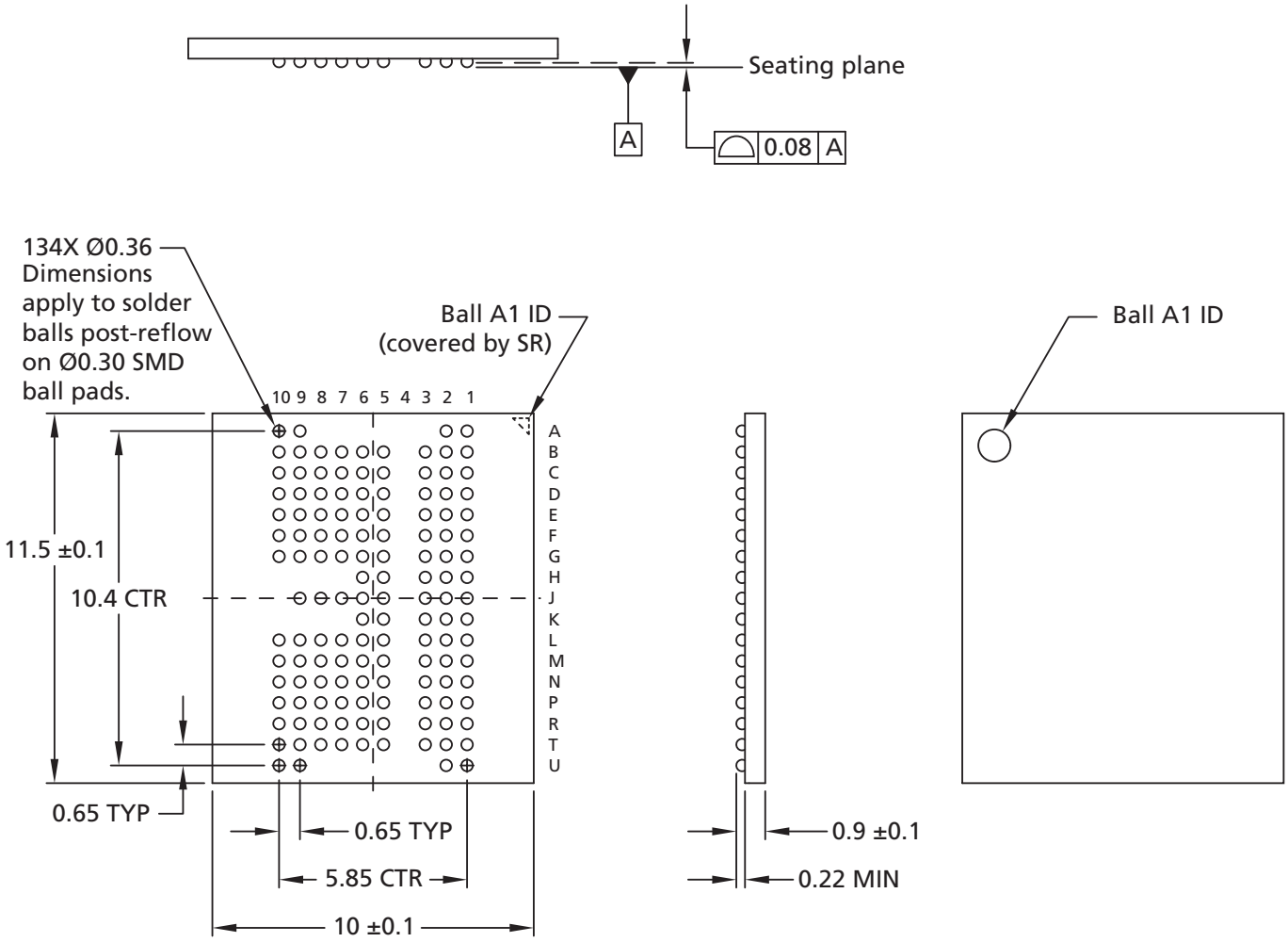
Package Block Diagrams

Figure 4: Single Rank, Single Channel Package Block Diagram



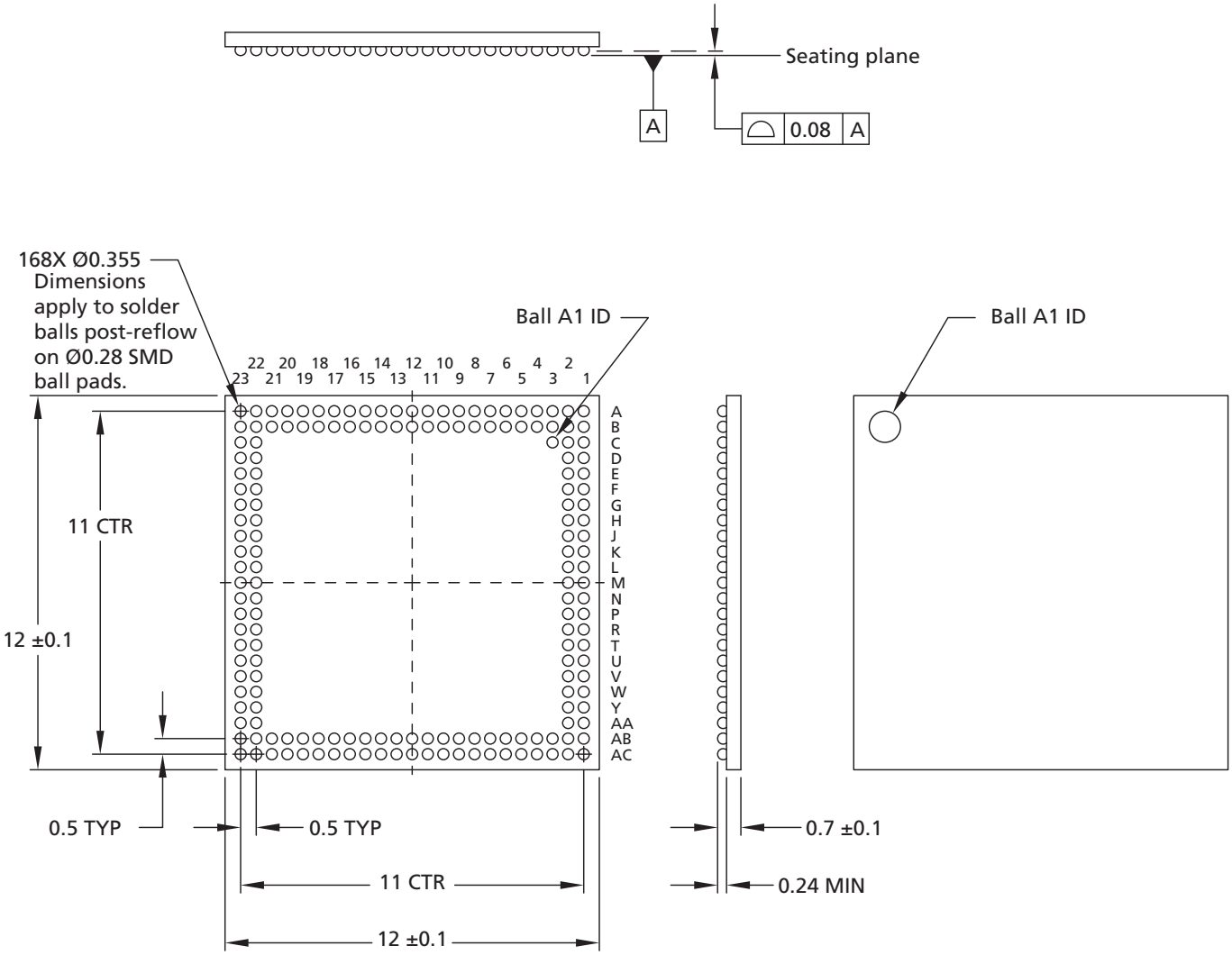
Package Dimensions

Figure 5: 134-Ball VFBGA – 10mm x 11.5mm (Package Code: BH)



Note: 1. All dimensions are in millimeters.

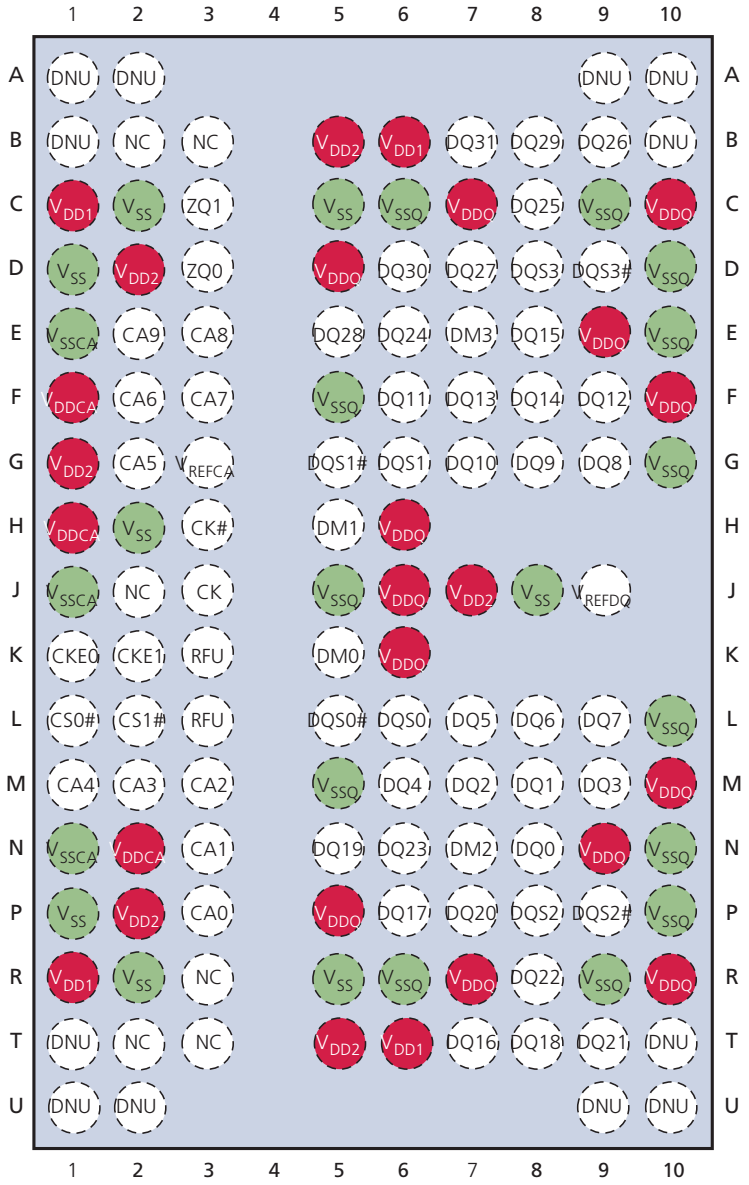
Figure 6: 168-Ball WFBGA – 12mm x 12mm (Package Code: PA)



Note: 1. All dimensions are in millimeters.

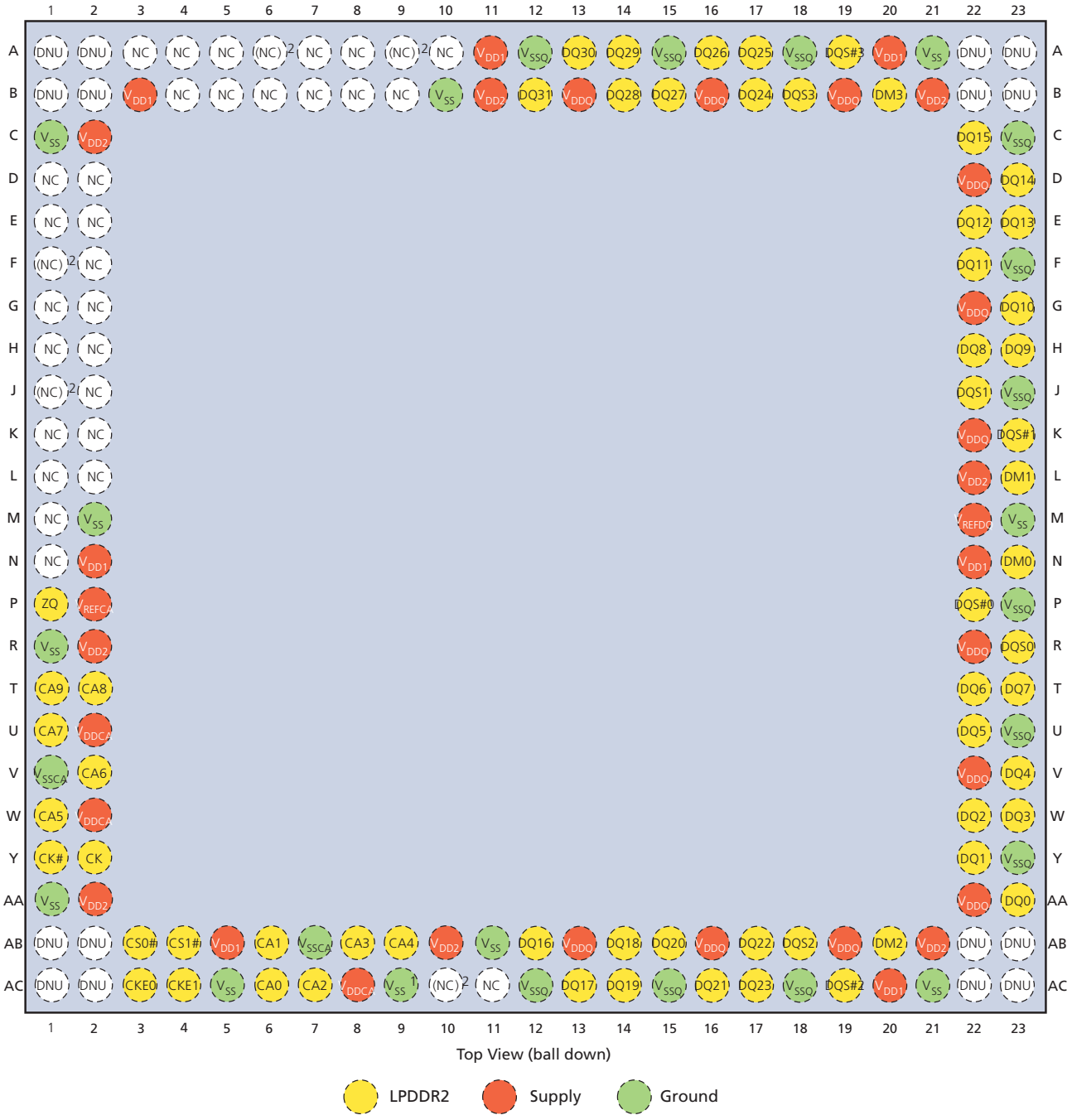
Ball Assignments and Descriptions

Figure 7: 134-Ball VFBGA (x32)



Notes:
1. CS1#, CKE1, and ZQ1 are reserved for the second rank use.
2. V_{DDCA} is unnecessary. F1, H1, and N2 pins are no care of the external connection.

Figure 8: 168-Ball WFBGA – 12mm x 12mm



Notes:
1. Ball AC9 may be V_{SS} or left unconnected.
2. Balls labeled NC = no connect; however, they can be connected together internally.
3. CS1# and CKE1 are reserved for the second rank use.
4. V_{DDCA} is unnecessary. U2, W2, and CA8 pins are no care of the external connection.

Table 6: Ball/Pad Descriptions

Symbol	Type	Description
CA[9:0]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE[1:0]	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK.
CS[1:0]#	Input	**Chip select:** CS# is considered part of the command code and is sampled at the rising edge of CK.
DM[3:0]	Input	**Input data mask:** DM is an input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[31:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[3:0], DQS[3:0]#	I/O	**Data strobe:** The data strobe is bidirectional (used for read and write data) and complementary (DQS and DQS#). It is edge-aligned output with read data and centered input with write data. DQS[3:0]/DQS[3:0]# is DQS for each of the four data bytes, respectively.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
V_{DDCA}	Supply	**Command/address power supply:** Command/address power supply.
V_{SSCA}	Supply	**Command/address ground:** Isolated on the die for improved noise immunity.
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{SS}	Supply	**Common ground**
V_{REFCA}, V_{REFDQ}	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers.
ZQ	Reference	**External impedance (240 ohm):** This signal is used to calibrate the device output impedance.
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.
(NC)	–	**No connect:** Balls indicated as (NC) are no connects, however, they could be connected together internally.

Note: 1. CS1# and CKE1 are reserved for the second rank use.

Functional Description

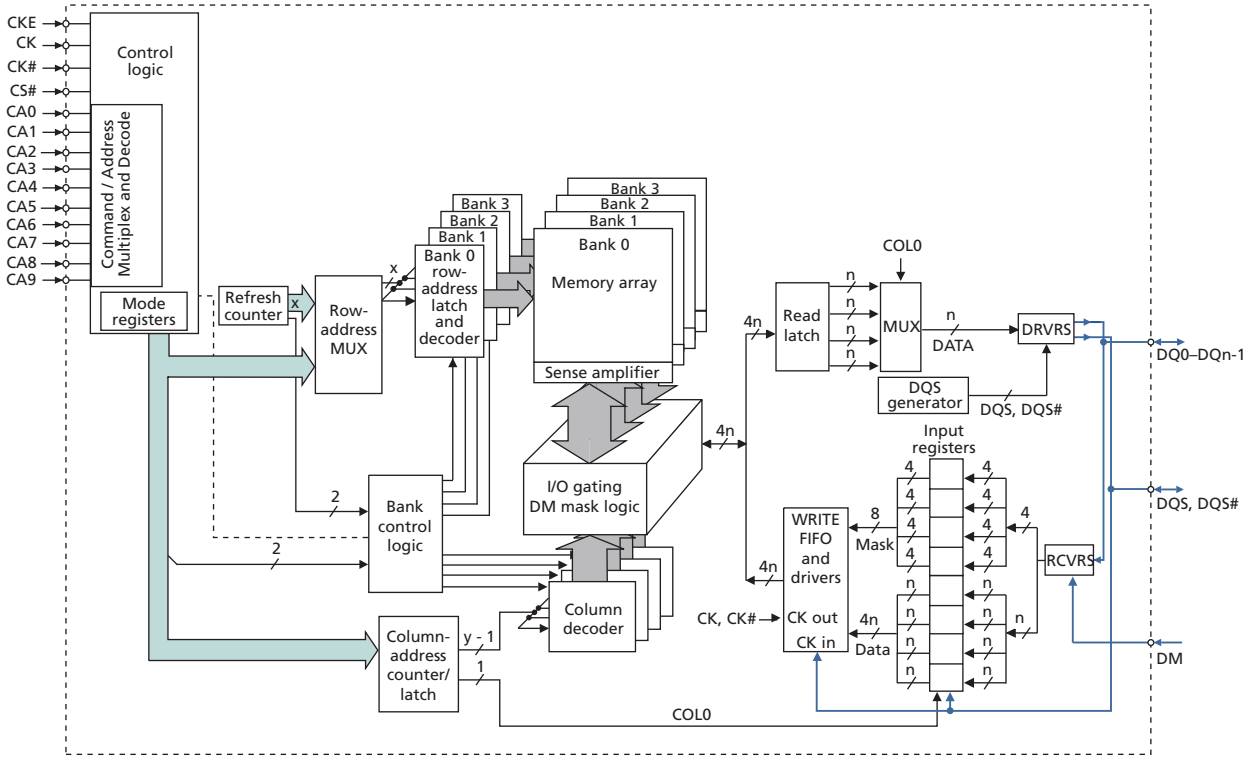
Mobile LPDDR2 is a high-speed SDRAM internally configured as a 4-bank memory device. LPDDR2 devices use a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

LPDDR2-S4 devices use a double data rate architecture on the DQ pins to achieve high-speed operation. The double data rate architecture is essentially a 4*n* prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command followed by a READ or WRITE command. The address and BA bits registered coincident with the ACTIVATE command are used to select the row and bank to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

Figure 9: Functional Block Diagram



Power-Up

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory (see Figure 10 (page 23)). Power-up and initialization by means other than those specified will result in undefined operation.

1. Voltage Ramp

While applying power (after Ta), CKE must be held LOW ($\leq 0.2 \times V_{DDCA}$), and all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

On or before the completion of the voltage ramp (Tb), CKE must be held LOW. DQ, DM, DQS, and DQS# voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latchup. CK, CK#, CS#, and CA input levels must be between V_{SSCA} and V_{DDCA} during voltage ramp to avoid latchup.

The following conditions apply for voltage ramp:

- Ta is the point when any power supply first reaches 300mV.
- Noted conditions apply between Ta and power-down (controlled or uncontrolled).
- Tb is the point at which all supply and reference voltages are within their defined operating ranges.
- Power ramp duration ^{t}INIT0 (Tb - Ta) must not exceed 20ms.
- For supply and reference voltage operating conditions, see the Recommended DC Operating Conditions table.
- The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins must not exceed 100mV.

Voltage Ramp Completion

After Ta is reached:

- V_{DD1} must be greater than V_{DD2} - 200mV
- V_{DD1} and V_{DD2} must be greater than V_{DDCA} - 200mV
- V_{DD1} and V_{DD2} must be greater than V_{DDQ} - 200mV
- V_{REF} must always be less than all other supply voltages

Beginning at Tb, CKE must remain LOW for at least ^{t}INIT1 = 100ns, after which CKE can be asserted HIGH. The clock must be stable at least ^{t}INIT2 = 5 × ^{t}CK prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS#, and CA inputs must observe setup and hold requirements (^{t}IS, ^{t}IH) with respect to the first rising clock edge (and to subsequent falling and rising edges).

If any MRRs are issued, the clock period must be within the range defined for ^{t}CKb (18ns to 100ns). MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, ^{t}DQSCK) could have relaxed timings (such as ^{t}DQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least ^{t}INIT3 = 200µs (Td).

2. RESET Command

After ^{t}INIT3 is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command.

Wait at least ^{t}INIT4 while keeping CKE asserted and issuing NOP commands.

3. MRRs and Device Auto Initialization (DAI) Polling

After ^{t}INIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications (see Power-Down).

The MRR command can be used to poll the DAI bit, which indicates when device auto initialization is complete; otherwise, the controller must wait a minimum of ^{t}INIT5, or until the DAI bit is set, before proceeding.

Because the memory output buffers are not properly configured by Te, some AC parameters must use relaxed timing specifications before the system is appropriately configured.

After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0.

The device sets the DAI bit no later than ^{t}INIT5 after the RESET command. The controller must wait at least ^{t}INIT5 or until the DAI bit is set before proceeding.

4. ZQ Calibration

After ^{t}INIT5 (Tf), the MRW initialization calibration (ZQ calibration) command can be issued to the memory (MR10).

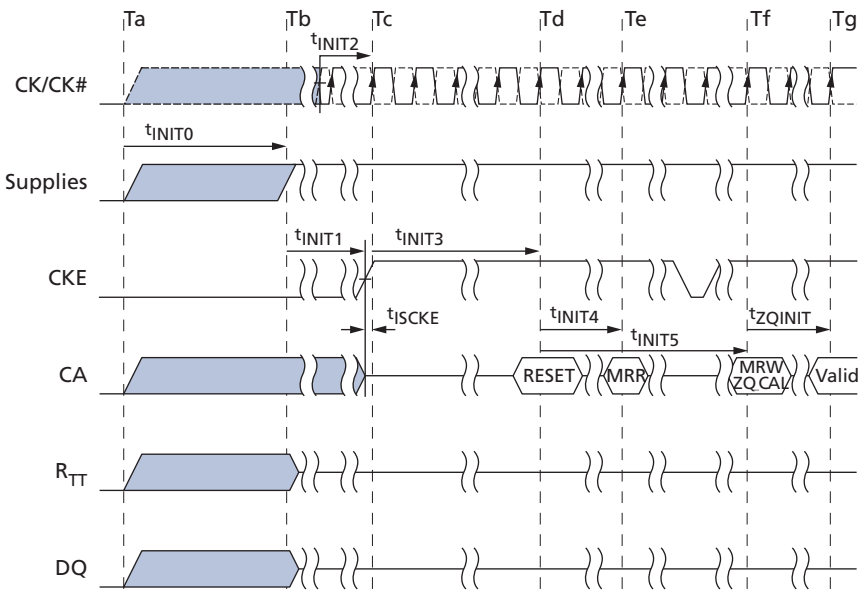
This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one Mobile LPDDR2 device exists on the same bus, the controller must not overlap MRW ZQ calibration commands. The device is ready for normal operation after ^{t}ZQINIT.

5. Normal Operation

After (Tg), MRW commands must be used to properly configure the memory (output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in Input Clock Frequency Changes and Clock Stop with CKE HIGH (page 75).

Figure 10: Voltage Ramp and Initialization Sequence



Note: 1. High-Z on the CA bus indicates valid NOP.

Table 7: Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	–	20	ms	Maximum voltage ramp time
tINIT1	100	–	ns	Minimum CKE LOW time after completion of voltage ramp
tINIT2	5	–	tCK	Minimum stable clock before first CKE HIGH
tINIT3	200	–	µs	Minimum idle time after first CKE assertion
tINIT4	1	–	µs	Minimum idle time after RESET command
tINIT5	–	10	µs	Maximum duration of device auto initialization
tZQINIT	1	–	µs	ZQ initial calibration (S4 devices only)
tCKb	18	100	ns	Clock cycle time during boot

Note: 1. The tINIT0 maximum specification is not a tested limit and should be used as a general guideline. For voltage ramp times exceeding tINIT0 MAX, please contact the factory.

Initialization After RESET (Without Voltage Ramp)

If the RESET command is issued before or after the power-up initialization sequence, the reinitialization procedure must begin at Td.

Power-Off

While powering off, CKE must be held LOW ($\leq 0.2 \times V_{DDCA}$); all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS, and DQS# voltage levels must be between V_{SSQ} and V_{DDQ} during the power-off sequence to avoid latchup. CK, CK#, CS#, and CA input levels must be between V_{SSCA} and V_{DDCA} during the power-off sequence to avoid latchup.

Tx is the point where any power supply drops below the minimum value specified in the Recommended DC Operating Conditions table.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Required Power Supply Conditions Between Tx and Tz:

- V_{DD1} must be greater than V_{DD2} - 200mV
- V_{DD1} must be greater than V_{DDCA} - 200mV
- V_{DD1} must be greater than V_{DDQ} - 200mV
- V_{REF} must always be less than all other supply voltages

The voltage difference between V_{SS}, V_{SSQ}, and V_{SSCA} must not exceed 100mV.

For supply and reference voltage operating conditions, see Recommended DC Operating Conditions table.

Uncontrolled Power-Off

When an uncontrolled power-off occurs, the following conditions must be met:

- At Tx, when the power supply drops below the minimum values specified in the Recommended DC Operating Conditions table, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.
- After Tz (the point at which all power supplies first reach 300mV), the device must power off. The time between Tx and Tz must not exceed ^{t}POFF. During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 8: Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Maximum power-off ramp time	^{t}POFF	–	2	sec

Mode Register Definition

LPDDR2 devices contain a set of mode registers used for programming device operating parameters, reading device information and status, and for initiating special operations such as DQ calibration, ZQ calibration, and device reset.

Mode Register Assignments and Definitions

The MRR command is used to read from a register. The MRW command is used to write to a register. An "R" in the access column of the mode register assignment table indicates read-only; a "W" indicates write-only; "R/W" indicates read or write capable or enabled.

Table 9: Mode Register Assignments

Notes 1–5 apply to all parameters and conditions

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00h	Device info	R	RFU			RZQI		DNVI	DI	DAI	go to MR0
1	01h	Device feature 1	W	*n*WR (for AP)			WC	BT	BL			go to MR1
2	02h	Device feature 2	W	RFU				RL and WL				go to MR2
3	03h	I/O config-1	W	RFU				DS				go to MR3
4	04h	SDRAM refresh rate	R	TUF	RFU				Refresh rate			go to MR4
5	05h	Basic config-1	R	LPDDR2 Manufacturer ID								go to MR5
6	06h	Basic config-2	R	Revision ID1								go to MR6
7	07h	Basic config-3	R	Revision ID2								go to MR7
8	08h	Basic config-4	R	I/O width		Density				Type		go to MR8
9	09h	Test mode	W	Vendor-specific test mode								go to MR9
10	0Ah	I/O calibration	W	Calibration code								go to MR10
11–15	0Bh ≈ 0Fh	Reserved	–	RFU								go to MR11
16	10h	PASR_Bank	W	Bank mask								go to MR16
17	11h	PASR_Seg	W	Segment mask								go to MR17
18–19	12h–13h	Reserved	–	RFU								go to MR18
20–31	14h–1Fh	Reserved for NVM										MR20–MR30
32	20h	DQ calibration pattern A	R	See Table 42 (page 62).								go to MR32
33–39	21h–27h	Do not use										go to MR33
40	28h	DQ calibration pattern B	R	See Table 42 (page 62).								go to MR40
41–47	29h–2Fh	Do not use										go to MR41
48–62	30h–3Eh	Reserved	–	RFU								go to MR48
63	3Fh	RESET	W	X								go to MR63
64–126	40h–7Eh	Reserved	–	RFU								go to MR64
127	7Fh	Do not use										go to MR127
128–190	80h–BEh	Reserved for vendor use		RVU								go to MR128
191	BFh	Do not use										go to MR191
192–254	C0h–FEh	Reserved for vendor use		RVU								go to MR192
255	FFh	Do not use										go to MR255

Notes:
1. RFU bits must be set to 0 during MRW.
2. RFU bits must be read as 0 during MRR.
3. For READs to a write-only or RFU register, DQS will be toggled and undefined data is returned.
4. RFU mode registers must not be written.
5. WRITEs to read-only registers must have no impact on the functionality of the device.