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LPDDR2 SDRAM

EDB8164B4PR, EDB8164B4PK, EDB8164B4PT, ED8A164B2PR

Features

- Ultra-low-voltage core and I/O power supplies
- Frequency range
 - 533 MHz (data rate: 1066 Mb/s/pin)
- 4n prefetch DDR architecture
- 8 internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on each CK_t/CK_c edge
- Bidirectional/differential data strobe per byte of data (DQS_t/DQS_c)
- Programmable READ and WRITE latencies (RL/WL)
- Burst length: 4, 8, and 16
- Per-bank refresh for concurrent operation
- Auto temperature-compensated self refresh (ATCSR) by built-in temperature sensor
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock-stop capability
- Lead-free (RoHS-compliant) and halogen-free packaging

Options

- Density/Page Size
 - 8Gb/2-CS – dual die
 - 16Gb/4-CS – quad die
- Organization
 - x64
- V_{DD1}/V_{DD2}/V_{DDQ}: 1.8V/1.2V/1.2V
- Revision
 - Dual die
 - Quad die
- FBGA “green” package
 - 12mm x 12mm x 0.8mm, 216-ball PoP FBGA package, dual die
 - 12mm x 12mm x 0.8mm, 216-ball PoP FBGA package, dual die
 - 12mm x 12mm x 1.0mm, 216-ball PoP FBGA package, quad die
 - 14mm x 14mm x 0.7mm, 220-ball PoP FBGA package, dual die
- Timing – cycle time
 - 1.875ns @ RL = 8
- Special options
 - Non-Automotive
- Operating temperature range
 - From –30°C to +85°C
 - From –40°C to +85°C
 - From –40°C to +105°C

Marking

- 81
- A1
- 64
- B
- 4
- 2
- PR
- PT
- PR
- PK
- 1D
- blank
- blank
- IT
- AT

Table 1: Key Timing Parameters

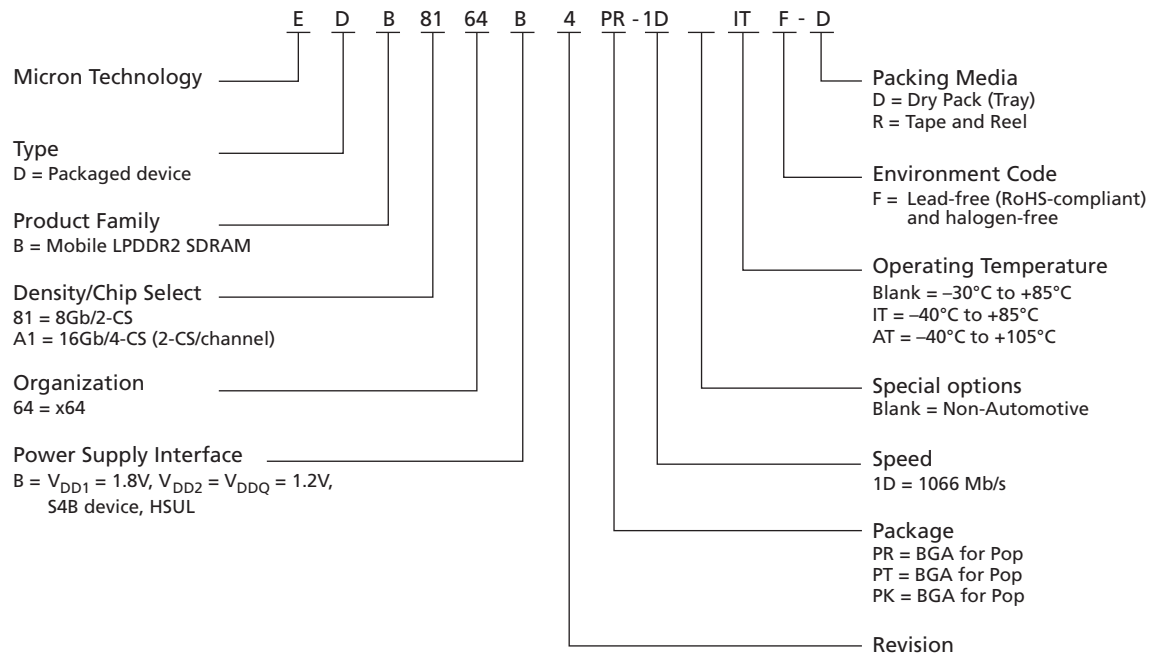
Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL
1D	533	1066	8	4

Table 2: S4 Configuration Addressing

Architecture	128 Meg x 64	256 Meg x 64
Die configuration	16 Meg x 32 x 8 banks x 2 channel	32 Meg x 32 x 8 banks x 2 channel
Row addressing	16K A[13:0]	16K A[13:0]
Column addressing	1K A[9:0]	1K A[9:0]
Number of die	2	4
Die per rank	1	2
Ranks per channel	1	2

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

Figure 1: LPDDR2 Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Table 3: Package Codes and Descriptions

Package Code	Ball Count	# Ranks	# Channels	Size (mm)	Die per Package	Solder Ball Composition
PR	216	1	2	12mm x 12mm x 0.80mm, 0.40 pitch	DDP	SAC302
PT	216	1	2	12mm x 12mm x 0.80mm, 0.40 pitch	DDP	SAC302
PR	216	2	2	12mm x 12mm x 1.00mm, 0.40 pitch	QDP	SAC302
PK	220	1	2	14mm x 14mm x 0.70mm, 0.50 pitch	DDP	SAC302

- Notes:
- DDP = dual-die package, QDP = quad-die package
 - Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

Contents

LPDDR2 Array Configuration	9
General Notes	9
I _{DD} Specifications	10
Package Block Diagrams	16
Package Dimensions	18
Ball Assignments	21
Ball Descriptions	24
Functional Description	25
Simplified State Diagram	26
Power-Up and Initialization	28
Voltage Ramp and Device Initialization	28
Initialization After RESET (Without Voltage Ramp)	30
Power-Off Sequence	30
Uncontrolled Power-Off Sequence	31
Mode Register Definition	31
Mode Register Assignments and Definitions	31
Commands and Timing	42
ACTIVATE Command	43
8-Bank Device Operation	44
Read and Write Access Modes	45
Burst READ Command	45
READs Interrupted by a READ	52
Burst WRITE Command	52
WRITEs Interrupted by a WRITE	55
BURST TERMINATE Command	55
Write Data Mask	57
PRECHARGE Command	58
READ Burst Followed by PRECHARGE	59
WRITE Burst Followed by PRECHARGE	60
Auto Precharge operation	61
READ Burst with Auto Precharge	61
WRITE Burst with Auto Precharge	62
REFRESH Command	64
REFRESH Requirements	66
SELF REFRESH Operation	73
Partial-Array Self Refresh – Bank Masking	75
Partial-Array Self Refresh – Segment Masking	75
MODE REGISTER READ	76
Temperature Sensor	78
DQ Calibration	80
MODE REGISTER WRITE Command	82
MRW RESET Command	82
MRW ZQ Calibration Commands	83
ZQ External Resistor Value, Tolerance, and Capacitive Loading	85
Power-Down	85
Deep Power-Down	92
Input Clock Frequency Changes and Stop Events	93
Input Clock Frequency Changes and Clock Stop with CKE LOW	93
Input Clock Frequency Changes and Clock Stop with CKE HIGH	94
NO OPERATION Command	94



Truth Tables	94
Absolute Maximum Ratings	102
Input/Output Capacitance	102
Electrical Specifications – I _{DD} Specifications and Conditions	103
AC and DC Operating Conditions	106
AC and DC Logic Input Measurement Levels for Single-Ended Signals	107
V _{REF} Tolerances	108
Input Signal	110
AC and DC Logic Input Measurement Levels for Differential Signals	112
Single-Ended Requirements for Differential Signals	113
Differential Input Crosspoint Voltage	115
Input Slew Rate	116
Output Characteristics and Operating Conditions	116
Single-Ended Output Slew Rate	117
Differential Output Slew Rate	118
HSUL ₁₂ Driver Output Timing Reference Load	120
Output Driver Impedance	121
Output Driver Impedance Characteristics with ZQ Calibration	122
Output Driver Temperature and Voltage Sensitivity	123
Output Impedance Characteristics Without ZQ Calibration	123
Clock Specification	126
^t CK(abs), ^t CH(abs), and ^t CL(abs)	128
Clock Period Jitter	128
Clock Period Jitter Effects on Core Timing Parameters	128
Cycle Time Derating for Core Timing Parameters	129
Clock Cycle Derating for Core Timing Parameters	129
Clock Jitter Effects on Command/Address Timing Parameters	129
Clock Jitter Effects on READ Timing Parameters	129
Clock Jitter Effects on WRITE Timing Parameters	130
Refresh Requirements Parameters	131
AC Timing	131
CA and CS _n Setup, Hold, and Derating	137
Data Setup, Hold, and Slew Rate Derating	145
Revision History	152
Rev. F – 08/16	152
Rev. E – 05/16	152
Rev. D – 03/16	152
Rev. C – 02/16	152
Rev. B – 01/15	152
Rev. A – 09/14	152

List of Figures

Figure 1: LPDDR2 Part Numbering	2
Figure 2: Dual Die Single Rank, Dual Channel Package Block Diagram	16
Figure 3: Quad Die Dual Rank, Dual Channel Package Block Diagram	17
Figure 4: 216-Ball FBGA (12mm x 12mm x 0.8mm) – EDB8164B4PR, EDB8164B4PT	18
Figure 5: 216-Ball FBGA (12mm x 12mm x 1.0mm) – ED8164B2PR	19
Figure 6: 220-Ball FBGA (14mm x 14mm x 0.7mm) – EDB8164B4PK	20
Figure 7: 216-Ball Dual-Channel FBGA – 2 x 4Gb Die	21
Figure 8: 220-Ball Dual-Channel FBGA – 2 x 4Gb Die	22
Figure 9: 216-Ball Dual-Channel FBGA – 4 x 4Gb Die	23
Figure 10: Functional Block Diagram	26
Figure 11: Simplified State Diagram	27
Figure 12: Voltage Ramp and Initialization Sequence	30
Figure 13: Command and Input Setup and Hold	43
Figure 14: CKE Input Setup and Hold	43
Figure 15: ACTIVATE Command	44
Figure 16: ^t FAW Timing (8-Bank Devices)	45
Figure 17: READ Output Timing – ^t DQSCK (MAX)	46
Figure 18: READ Output Timing – ^t DQSCK (MIN)	46
Figure 19: Burst READ – RL = 5, BL = 4, ^t DQSCK > ^t CK	47
Figure 20: Burst READ – RL = 3, BL = 8, ^t DQSCK < ^t CK	47
Figure 21: ^t DQSCKDL Timing	48
Figure 22: ^t DQSCKDM Timing	49
Figure 23: ^t DQSCKDS Timing	50
Figure 24: Burst READ Followed by Burst WRITE – RL = 3, WL = 1, BL = 4	51
Figure 25: Seamless Burst READ – RL = 3, BL = 4, ^t CCD = 2	51
Figure 26: READ Burst Interrupt Example – RL = 3, BL = 8, ^t CCD = 2	52
Figure 27: Data Input (WRITE) Timing	53
Figure 28: Burst WRITE – WL = 1, BL = 4	53
Figure 29: Burst WRITE Followed by Burst READ – RL = 3, WL = 1, BL = 4	54
Figure 30: Seamless Burst WRITE – WL = 1, BL = 4, ^t CCD = 2	54
Figure 31: WRITE Burst Interrupt Timing – WL = 1, BL = 8, ^t CCD = 2	55
Figure 32: Burst WRITE Truncated by BST – WL = 1, BL = 16	56
Figure 33: Burst READ Truncated by BST – RL = 3, BL = 16	57
Figure 34: Data Mask Timing	57
Figure 35: Write Data Mask – Second Data Bit Masked	58
Figure 36: READ Burst Followed by PRECHARGE – RL = 3, BL = 8, RU(^t RTP(MIN)/ ^t CK) = 2	59
Figure 37: READ Burst Followed by PRECHARGE – RL = 3, BL = 4, RU(^t RTP(MIN)/ ^t CK) = 3	60
Figure 38: WRITE Burst Followed by PRECHARGE – WL = 1, BL = 4	61
Figure 39: READ Burst with Auto Precharge – RL = 3, BL = 4, RU(^t RTP(MIN)/ ^t CK) = 2	62
Figure 40: WRITE Burst with Auto Precharge – WL = 1, BL = 4	63
Figure 41: ^t SRF Definition	67
Figure 42: Regular Distributed Refresh Pattern	69
Figure 43: Supported Transition from Repetitive REFRESH Burst	70
Figure 44: Nonsupported Transition from Repetitive REFRESH Burst	71
Figure 45: Recommended Self Refresh Entry and Exit	72
Figure 46: All-Bank REFRESH Operation	73
Figure 47: Per-Bank REFRESH Operation	73
Figure 48: SELF REFRESH Operation	74
Figure 49: MRR Timing – RL = 3, ^t MRR = 2	76
Figure 50: READ to MRR Timing – RL = 3, ^t MRR = 2	77



Figure 51: Burst WRITE Followed by MRR – RL = 3, WL = 1, BL = 4	78
Figure 52: Temperature Sensor Timing	80
Figure 53: MR32 and MR40 DQ Calibration Timing – RL = 3, $t^{MRR} = 2$	81
Figure 54: MODE REGISTER WRITE Timing – RL = 3, $t^{MRW} = 5$	82
Figure 55: ZQ Timings	84
Figure 56: Power-Down Entry and Exit Timing	86
Figure 57: CKE Intensive Environment	86
Figure 58: REFRESH-to-REFRESH Timing in CKE Intensive Environments	86
Figure 59: READ to Power-Down Entry	87
Figure 60: READ with Auto Precharge to Power-Down Entry	88
Figure 61: WRITE to Power-Down Entry	89
Figure 62: WRITE with Auto Precharge to Power-Down Entry	90
Figure 63: REFRESH Command to Power-Down Entry	91
Figure 64: ACTIVATE Command to Power-Down Entry	91
Figure 65: PRECHARGE Command to Power-Down Entry	91
Figure 66: MRR Command to Power-Down Entry	92
Figure 67: MRW Command to Power-Down Entry	92
Figure 68: Deep Power-Down Entry and Exit Timing	93
Figure 69: V_{REF} DC Tolerance and V_{REF} AC Noise Limits	108
Figure 70: LPDDR2-466 to LPDDR2-1066 Input Signal	110
Figure 71: LPDDR2-200 to LPDDR2-400 Input Signal	111
Figure 72: Differential AC Swing Time and t^{DVAC}	112
Figure 73: Single-Ended Requirements for Differential Signals	114
Figure 74: V_{IX} Definition	115
Figure 75: Differential Input Slew Rate Definition for CK_t, CK_c, DQS_t, and DQS_c	116
Figure 76: Single-Ended Output Slew Rate Definition	118
Figure 77: Differential Output Slew Rate Definition	119
Figure 78: Overshoot and Undershoot Definition	120
Figure 79: HSUL_12 Driver Output Reference Load for Timing and Slew Rate	121
Figure 80: Output Driver	122
Figure 81: Output Impedance = 240 Ohms, I-V Curves After ZQRESET	125
Figure 82: Output Impedance = 240 Ohms, I-V Curves After Calibration	126
Figure 83: Typical Slew Rate and $t^{VAC} - t^{IS}$ for CA and CS_n Relative to Clock	141
Figure 84: Typical Slew Rate – t^{IH} for CA and CS_n Relative to Clock	142
Figure 85: Tangent Line – t^{IS} for CA and CS_n Relative to Clock	143
Figure 86: Tangent Line – t^{IH} for CA and CS_n Relative to Clock	144
Figure 87: Typical Slew Rate and $t^{VAC} - t^{DS}$ for DQ Relative to Strobe	148
Figure 88: Typical Slew Rate – t^{DH} for DQ Relative to Strobe	149
Figure 89: Tangent Line – t^{DS} for DQ with Respect to Strobe	150
Figure 90: Tangent Line – t^{DH} for DQ with Respect to Strobe	151

List of Tables

Table 1: Key Timing Parameters	1
Table 2: S4 Configuration Addressing	1
Table 3: Package Codes and Descriptions	2
Table 4: I _{DD} Specifications – Dual Die, Dual Channel	10
Table 5: I _{DD6} Full-Array Self Refresh Current at 45°C for Dual die product	12
Table 6: I _{DD6} Partial-Array Self Refresh Current at 85°C for Dual die product	12
Table 7: I _{DD} Specifications – Dual Die, Dual Channel	13
Table 8: I _{DD6} Partial-Array Self Refresh Current at 105°C Dual die for Dual die product	15
Table 9: Ball/Pad Descriptions	24
Table 10: Initialization Timing Parameters	30
Table 11: Power-Off Timing	31
Table 12: Mode Register Assignments	32
Table 13: MR0 Device Information (MA[7:0] = 00h)	33
Table 14: MR0 Op-Code Bit Definitions	33
Table 15: MR1 Device Feature 1 (MA[7:0] = 01h)	33
Table 16: MR1 Op-Code Bit Definitions	33
Table 17: Burst Sequence by Burst Length (BL), Burst Type (BT), and Wrap Control (WC)	34
Table 18: No-Wrap Restrictions	35
Table 19: MR2 Device Feature 2 (MA[7:0] = 02h)	35
Table 20: MR2 Op-Code Bit Definitions	36
Table 21: MR3 I/O Configuration 1 (MA[7:0] = 03h)	36
Table 22: MR3 Op-Code Bit Definitions	36
Table 23: MR4 Device Temperature (MA[7:0] = 04h)	36
Table 24: MR4 Op-Code Bit Definitions	37
Table 25: MR5 Basic Configuration 1 (MA[7:0] = 05h)	37
Table 26: MR5 Op-Code Bit Definitions	37
Table 27: MR6 Basic Configuration 2 (MA[7:0] = 06h)	38
Table 28: MR6 Op-Code Bit Definitions	38
Table 29: MR7 Basic Configuration 3 (MA[7:0] = 07h)	38
Table 30: MR7 Op-Code Bit Definitions	38
Table 31: MR8 Basic Configuration 4 (MA[7:0] = 08h)	38
Table 32: MR8 Op-Code Bit Definitions	38
Table 33: MR9 Test Mode (MA[7:0] = 09h)	39
Table 34: MR10 Calibration (MA[7:0] = 0Ah)	39
Table 35: MR10 Op-Code Bit Definitions	39
Table 36: MR[11:15] Reserved (MA[7:0] = 0Bh–0Fh)	40
Table 37: MR16 PASR Bank Mask (MA[7:0] = 010h)	40
Table 38: MR16 Op-Code Bit Definitions	40
Table 39: MR16 Bank and OP corresponding table	40
Table 40: MR17 PASR Segment Mask (MA[7:0] = 011h)	41
Table 41: MR17 PASR Segment Mask Definitions (1Gb - 8Gb only)	41
Table 42: MR17 PASR Row Address Ranges in Masked Segments	41
Table 43: Reserved Mode Registers	42
Table 44: MR32 DQ Calibration Pattern A (MA[7:0] = 20H)	42
Table 45: MR40 DQ Calibration Pattern B (MA[7:0] = 28H)	42
Table 46: MR63 RESET (MA[7:0] = 3Fh) – MRW Only	42
Table 47: Bank Selection for PRECHARGE by Address Bits	59
Table 48: PRECHARGE and Auto Precharge Clarification	63
Table 49: REFRESH Command Scheduling Separation Requirements	65
Table 50: Bank and Segment Masking Example	75



Table 51: Temperature Sensor Definitions and Operating Conditions	79
Table 52: Data Calibration Pattern Description	82
Table 53: Truth Table for MRR and MRW	82
Table 54: Command Truth Table	94
Table 55: CKE Truth Table	96
Table 56: Current State Bank <i>n</i> to Command to Bank <i>n</i> Truth Table	97
Table 57: Current State Bank <i>n</i> to Command to Bank <i>m</i> Truth Table	99
Table 58: DM Truth Table	101
Table 59: Absolute Maximum DC Ratings	102
Table 60: Input/Output Capacitance	102
Table 61: Switching for CA Input Signals	103
Table 62: Switching for I _{DD4R}	103
Table 63: Switching for I _{DD4W}	104
Table 64: I _{DD} Specification Parameters and Operating Conditions	104
Table 65: Recommended DC Operating Conditions	106
Table 66: Input Leakage Current	106
Table 67: Operating Temperature Range	107
Table 68: Single-Ended AC and DC Input Levels for CA and CS _n Inputs	107
Table 69: Single-Ended AC and DC Input Levels for CKE	107
Table 70: Single-Ended AC and DC Input Levels for DQ and DM	108
Table 71: Differential AC and DC Input Levels	112
Table 72: CK _t /CK _c and DQS _t /DQS _c Time Requirements Before Ringback (^t DVAC)	113
Table 73: Single-Ended Levels for CK _t , CK _c , DQS _t , DQS _c	114
Table 74: Crosspoint Voltage for Differential Input Signals (CK _t , CK _c , DQS _t , DQS _c)	115
Table 75: Differential Input Slew Rate Definition	116
Table 76: Single-Ended AC and DC Output Levels	116
Table 77: Differential AC and DC Output Levels	117
Table 78: Single-Ended Output Slew Rate Definition	117
Table 79: Single-Ended Output Slew Rate	118
Table 80: Differential Output Slew Rate Definition	119
Table 81: Differential Output Slew Rate	119
Table 82: AC Overshoot/Undershoot Specification	120
Table 83: Output Driver DC Electrical Characteristics with ZQ Calibration	122
Table 84: Output Driver Sensitivity Definition	123
Table 85: Output Driver Temperature and Voltage Sensitivity	123
Table 86: Output Driver DC Electrical Characteristics Without ZQ Calibration	123
Table 87: I-V Curves	124
Table 88: Definitions and Calculations	127
Table 89: ^t CK(abs), ^t CH(abs), and ^t CL(abs) Definitions	128
Table 90: Refresh Requirement Parameters (Per Density)	131
Table 91: AC Timing	131
Table 92: CA and CS _n Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate)	138
Table 93: CA and CS _n Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate)	138
Table 94: Derating Values for AC/DC-Based ^t IS/ ^t IH (AC220)	139
Table 95: Derating Values for AC/DC-Based ^t IS/ ^t IH (AC300)	139
Table 96: Required Time for Valid Transition – ^t VAC > V _{IH(AC)} and < V _{IL(AC)}	139
Table 97: Data Setup and Hold Base Values (>400 MHz, 1 V/ns Slew Rate)	145
Table 98: Data Setup and Hold Base Values (<400 MHz, 1 V/ns Slew Rate)	146
Table 99: Derating Values for AC/DC-Based ^t DS/ ^t DH (AC220)	146
Table 100: Derating Values for AC/DC-Based ^t DS/ ^t DH (AC300)	147
Table 101: Required Time for Valid Transition – ^t VAC > V _{IH(AC)} OR < V _{IL(AC)}	147

LPDDR2 Array Configuration

The 4Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 4,294,967,296-bits. The device is internally configured as an eight-bank DRAM. Each of the x16's 536,870,912-bit banks is organized as 16,384 rows by 2048 columns by 16 bits. Each of the x32's 536,870,912-bit banks is organized as 16,384 rows by 1024 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

I_{DD} Specifications

Table 4: I_{DD} Specifications – Dual Die, Dual Channel

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –40°C to +85°C

Symbol	Supply	Speed	Unit	Parameter/Condition
		1066		
I _{DD01}	V _{DD1}	16	mA	All devices in operating one bank active-precharge Conditions for operating devices are: t _{CK} = t _{CK} (avg) MIN; t _{RC} = t _{RC} (MIN); CKE is HIGH; CS _n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD02}	V _{DDQ} V _{DDQ}	100		
I _{DD2P1}	V _{DD1}	0.8	mA	All devices in idle power-down standby current t _{CK} = t _{CK} (avg) MIN; CKE is LOW; CS _n is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD2P2}	V _{DDQ} V _{DDQ}	1.8		
I _{DD2PS1}	V _{DD1}	0.8	mA	All devices in idle power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is LOW; CS _n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD2PS2}	V _{DDQ} V _{DDQ}	1.8		
I _{DD2N1}	V _{DD1}	1.2	mA	All devices in idle non power-down standby current. t _{CK} = t _{CK} (avg) MIN; CKE is HIGH; CS _n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD2N2}	V _{DDQ} V _{DDQ}	26		
I _{DD2NS1}	V _{DD1}	1.2	mA	All devices in idle non power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is HIGH; CS _n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD2NS2}	V _{DDQ} V _{DDQ}	12		
I _{DD3P1}	V _{DD1}	1.6	mA	All devices in active power-down standby current t _{CK} = t _{CK} (avg) MIN; CKE is LOW; CS _n is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD3P2}	V _{DDQ} V _{DDQ}	10		
I _{DD3PS1}	V _{DD1}	1.6	mA	All devices in active power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is LOW; CS _n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD3PS2}	V _{DDQ} V _{DDQ}	10		

Table 4: I_{DD} Specifications – Dual Die, Dual Channel (Continued)

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –40°C to +85°C

Symbol	Supply	Speed	Unit	Parameter/Condition
		1066		
I _{DD3N1}	V _{DD1}	2.4	mA	All devices in active non power-down standby current t ^{CK} = t ^{CK} (avg) MIN; CKE is HIGH; CS _n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD3N2}	V _{DDQ} V _{DDQ}	38		
I _{DD3NS1}	V _{DD1}	2.4	mA	All devices in active non power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is HIGH; CS _n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD3NS2}	V _{DDQ} V _{DDQ}	24		
I _{DD4R1}	V _{DD1}	4	mA	All devices in operating burst read t ^{CK} = t ^{CK} (avg) MIN; CS _n is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I _{DD4R2}	V _{DDQ} V _{DDQ}	840		
I _{DD4W1}	V _{DD1}	4	mA	All devices in operating burst write t ^{CK} = t ^{CK} (avg) MIN; CS _n is HIGH between valid commands; One bank is active; BL = 4; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I _{DD4W2}	V _{DDQ} V _{DDQ}	300		
I _{DD51}	V _{DD1}	40	mA	All devices in all bank auto-refresh t ^{CK} = t ^{CK} (avg) MIN; CKE is HIGH between valid commands; t ^{RC} = t ^{RC} cab (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD52}	V _{DDQ} V _{DDQ}	240		
I _{DD5AB1}	V _{DD1}	8	mA	All devices in all bank auto-refresh t ^{CK} = t ^{CK} (avg) MIN; CKE is HIGH between valid commands; t ^{RC} = t ^{REFI} ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD5AB2}	V _{DDQ} V _{DDQ}	40		
I _{DD5PB1}	V _{DD1}	8	mA	All devices in per bank auto-refresh t ^{CK} = t ^{CK} (avg) MIN; CKE is HIGH between valid commands; t ^{RC} = t ^{REFI} pb; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD5PB2}	V _{DDQ} V _{DDQ}	40		

- Notes: 1. Published I_{DD} values are the maximum of the distribution of the arithmetic mean.
2. I_{DD} current specifications are tested after the device is properly initialized.

3. V_{DD2} and V_{DDQ} are connected internally in the package.
4. The Quad die product I_{DD} for each channel will be the sum of the I_{DD}'s for the state of operation for each rank (CS) in the channel.

Table 5: I_{DD6} Full-Array Self Refresh Current at 45°C for Dual die product

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V _{DD1}	400	μA	All devices in self refresh CK _t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V _{DDQ} V _{DDQ}	1600		
1/2 array	V _{DD1}	320		
	V _{DDQ} V _{DDQ}	1000		
1/4 array	V _{DD1}	260		
	V _{DDQ} V _{DDQ}	600		
1/8 array	V _{DD1}	240		
	V _{DDQ} V _{DDQ}	400		

Note: 1. I_{DD6} 45°C is the typical of the distribution of the arithmetic mean, Quad die product will be double these values when all die are in self refresh mode.

Table 6: I_{DD6} Partial-Array Self Refresh Current at 85°C for Dual die product

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V _{DD1}	1800	μA	All devices in self refresh CK _t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V _{DDQ} V _{DDQ}	6400		
1/2 array	V _{DD1}	1300		
	V _{DDQ} V _{DDQ}	4400		
1/4 array	V _{DD1}	1100		
	V _{DDQ} V _{DDQ}	3400		
1/8 array	V _{DD1}	1000		
	V _{DDQ} V _{DDQ}	2800		

Note: 1. I_{DD6} 85°C is the maximum of the distribution of the arithmetic mean, Quad die product will be double these values when all die are in self refresh mode.

Table 7: I_{DD} Specifications – Dual Die, Dual Channel

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –40°C to +105°C

Symbol	Supply	Speed	Unit	Parameter/Condition
		1066		
I _{DD01}	V _{DD1}	16	mA	All devices in operating one bank active-precharge Conditions for operating devices are: t ^{CK} = t ^{CK} (avg) MIN; t ^{RC} = t ^{RC} (MIN); CKE is HIGH; CS _n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD02}	V _{DD2} , V _{DDQ}	100		
I _{DD2P1}	V _{DD1}	0.8	mA	All devices in idle power-down standby current t ^{CK} = t ^{CK} (avg) MIN; CKE is LOW; CS _n is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD2P2}	V _{DD2} , V _{DDQ}	1.8		
I _{DD2PS1}	V _{DD1}	0.8	mA	All devices in idle power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is LOW; CS _n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD2PS2}	V _{DD2} , V _{DDQ}	1.8		
I _{DD2N1}	V _{DD1}	1.2	mA	All devices in idle non power-down standby current. t ^{CK} = t ^{CK} (avg) MIN; CKE is HIGH; CS _n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD2N2}	V _{DD2} , V _{DDQ}	30		
I _{DD2NS1}	V _{DD1}	1.2	mA	All devices in idle non power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is HIGH; CS _n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD2NS2}	V _{DD2} , V _{DDQ}	16		
I _{DD3P1}	V _{DD1}	1.8	mA	All devices in active power-down standby current t ^{CK} = t ^{CK} (avg) MIN; CKE is LOW; CS _n is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD3P2}	V _{DD2} , V _{DDQ}	14		
I _{DD3PS1}	V _{DD1}	1.8	mA	All devices in active power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is LOW; CS _n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD3PS2}	V _{DD2} , V _{DDQ}	14		
I _{DD3N1}	V _{DD1}	2.8	mA	All devices in active non power-down standby current t ^{CK} = t ^{CK} (avg) MIN; CKE is HIGH; CS _n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD3N2}	V _{DD2} , V _{DDQ}	44		

Table 7: I_{DD} Specifications – Dual Die, Dual Channel (Continued)

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –40°C to +105°C

Symbol	Supply	Speed	Unit	Parameter/Condition
		1066		
I _{DD3NS1}	V _{DD1}	2.8	mA	All devices in active non power-down standby current with clock stop CK _t = LOW, CK _c = HIGH; CKE is HIGH; CS _n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I _{DD3NS2}	V _{DD2} , V _{DDQ}	30		
I _{DD4R1}	V _{DD1}	4	mA	All devices in operating burst read t _{CK} = t _{CK(ave)} MIN; CS _n is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I _{DD4R2}	V _{DD2} , V _{DDQ}	840		
I _{DD4W1}	V _{DD1}	4	mA	All devices in operating burst write t _{CK} = t _{CK(ave)} MIN; CS _n is HIGH between valid commands; One bank is active; BL = 4; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I _{DD4W2}	V _{DD2} , V _{DDQ}	300		
I _{DD51}	V _{DD1}	40	mA	All devices in all bank auto-refresh t _{CK} = t _{CK(ave)} MIN; CKE is HIGH between valid commands; t _{RC} = t _{RFCab} (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD52}	V _{DD2} , V _{DDQ}	240		
I _{DD5AB1}	V _{DD1}	12	mA	All devices in all bank auto-refresh t _{CK} = t _{CK(ave)} MIN; CKE is HIGH between valid commands; t _{RC} = t _{REFI} ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD5AB2}	V _{DD2} , V _{DDQ}	56		
I _{DD5PB1}	V _{DD1}	12	mA	All devices in per bank auto-refresh t _{CK} = t _{CK(ave)} MIN; CKE is HIGH between valid commands; t _{RC} = t _{REFIpb} ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I _{DD5PB2}	V _{DD2} , V _{DDQ}	56		

- Notes:
1. Published I_{DD} values are the maximum of the distribution of the arithmetic mean.
 2. I_{DD} current specifications are tested after the device is properly initialized.
 3. V_{DD2} and V_{DDQ} are connected internally in the package.
 4. The Quad die product I_{DD} for each channel will be the sum of the I_{DD}'s for the state of operation for each rank (CS) in the channel.



Table 8: I_{DD6} Partial-Array Self Refresh Current at 105°C Dual die for Dual die product

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V _{DD1}	4800	μA	All devices in self refresh CK _t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V _{DDQ} V _{DDQ}	28000		
1/2 array	V _{DD1}	3200		
	V _{DDQ} V _{DDQ}	15600		
1/4 array	V _{DD1}	2200		
	V _{DDQ} V _{DDQ}	9600		
1/8 array	V _{DD1}	1800		
	V _{DDQ} V _{DDQ}	6400		

Note: 1. I_{DD6} 105°C is the maximum of the distribution of the arithmetic mean, Quad die product will be double these values when all die are in self refresh mode.

Package Block Diagrams

Figure 2: Dual Die Single Rank, Dual Channel Package Block Diagram

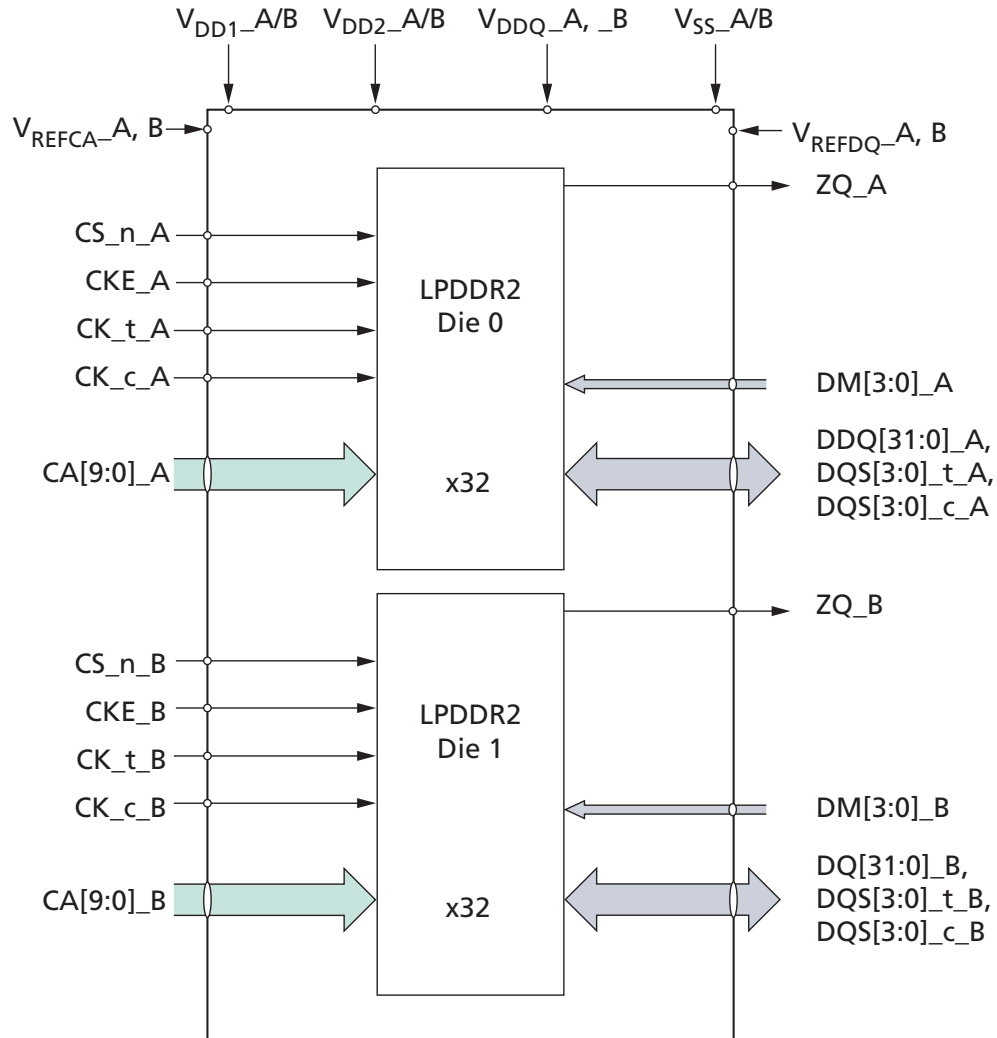


Figure 3: Quad Die Dual Rank, Dual Channel Package Block Diagram

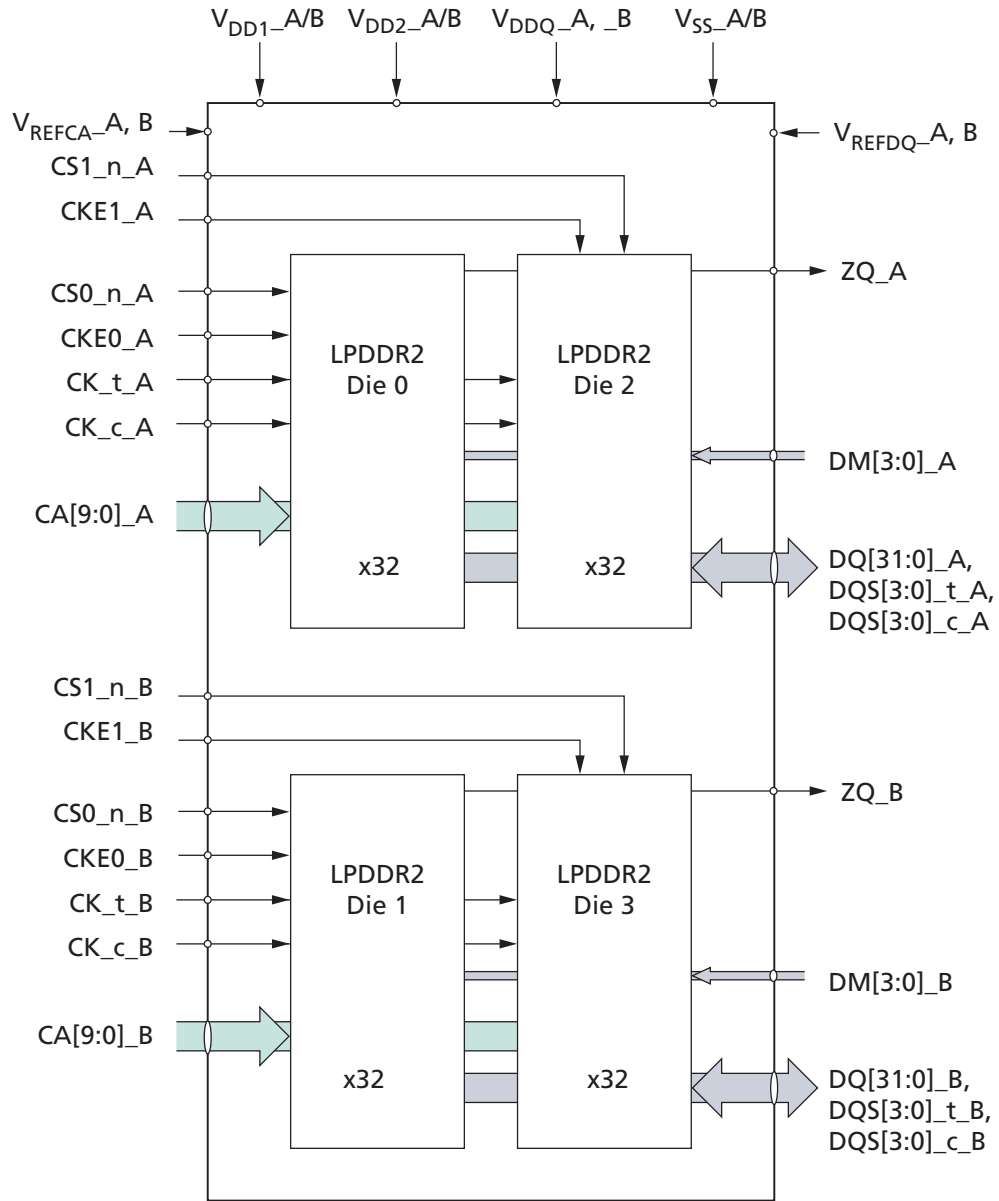
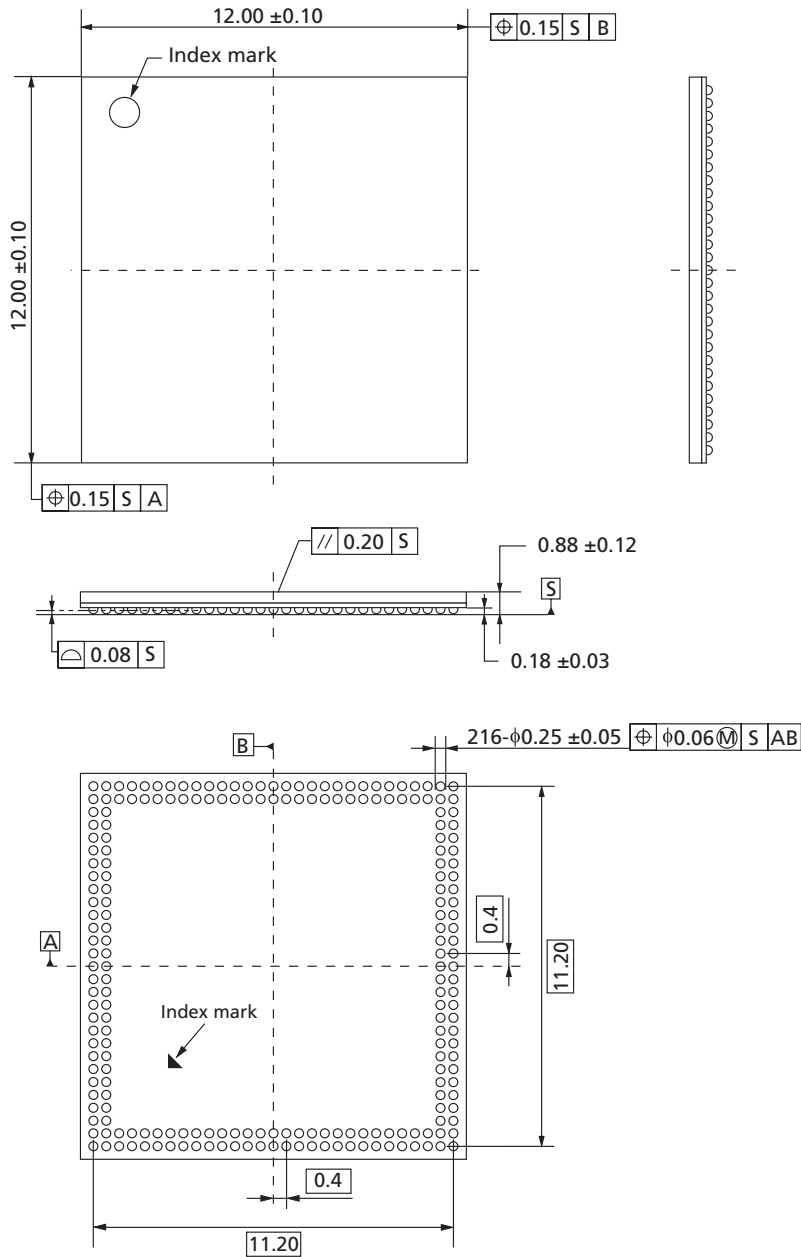
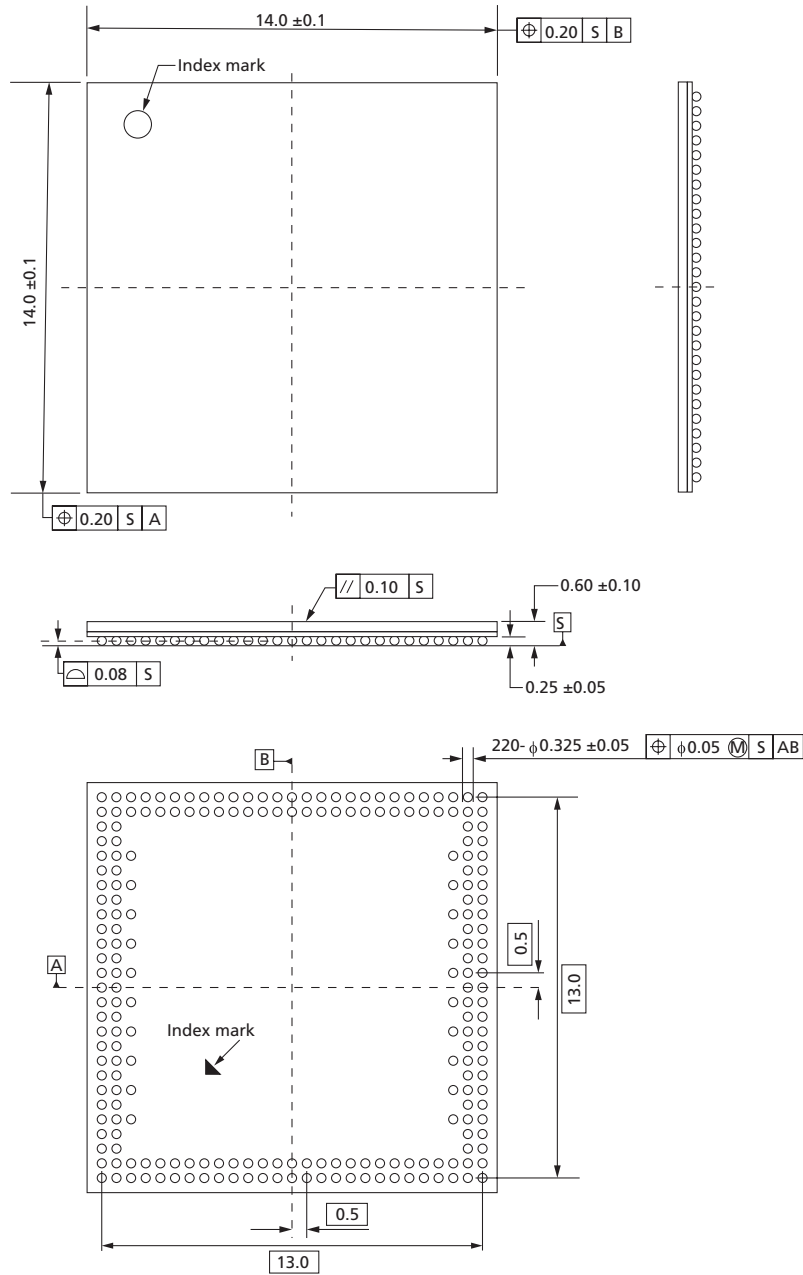


Figure 5: 216-Ball FBGA (12mm x 12mm x 1.0mm) – EDBA164B2PR



Note: 1. All dimensions are in millimeters.

Figure 6: 220-Ball FBGA (14mm x 14mm x 0.7mm) – EDB8164B4PK



Note: 1. All dimensions are in millimeters.

Ball Assignments

Figure 7: 216-Ball Dual-Channel FBGA – 2 x 4Gb Die

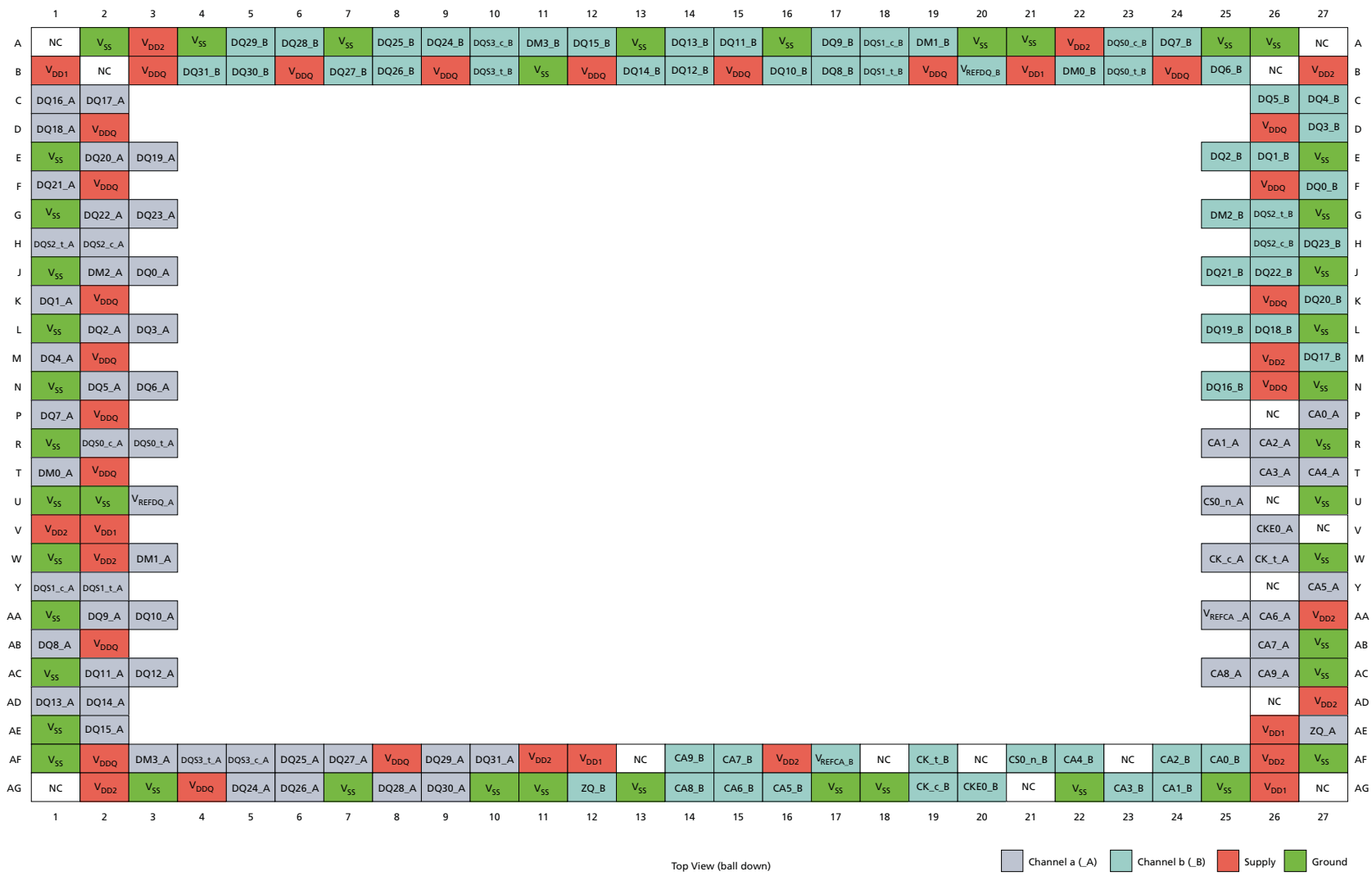
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	NC	V _{DD2}	V _{DD2}	DQ30_A	DQ29_A	V _{SS}	DQ26_A	DQ25_A	V _{SS}	DQS3_c_A	V _{SS}	DQ14_A	DQ13_A	V _{SS}	V _{DD1}	V _{DD2}	DQ11_A	DQ10_A	DQ9_A	DQS1_l_A	DM1_A	V _{DDQ}	DQS0_l_A	DQ7_A	DQ6_A	DQ4_A	DQ3_A	V _{SS}	NC
B	V _{SS}	NC	DQ31_A	V _{DDQ}	DQ28_A	DQ27_A	V _{DDQ}	DQ24_A	V _{DDQ}	DQS3_l_A	DM3_A	DQ15_A	V _{DDQ}	V _{SS}	V _{REFDQ_A}	V _{DD2}	DQ12_A	V _{DDQ}	DQ8_A	DQS1_c_A	V _{SS}	DM0_A	DQS0_c_A	V _{SS}	V _{DDQ}	DQ5_A	DQ2_A	NC	V _{SS}
C	V _{DD1}	DQ16_B																										V _{DD1}	V _{DD2}
D	DQ17_B	V _{DDQ}																										DQ1_A	V _{DDQ}
E	DQ18_B	DQ19_B																										V _{SS}	DQ0_A
F	V _{SS}	DQ20_B																									DM2_A	V _{DDQ}	
G	DQ21_B	V _{DDQ}																									DQS2_L_A	DQS2_c_A	
H	DQ22_B	DQ23_B																										V _{SS}	DQ23_A
J	V _{SS}	V _{DDQ}																										V _{DDQ}	DQ22_A
K	DQS2_c_B	DQS2_l_B																										DQ20_A	DQ21_A
L	DM2_B	DQ0_B																										DQ19_A	V _{SS}
M	DQ1_B	V _{SS}																										V _{DDQ}	DQ18_A
N	DQ2_B	V _{DD1}																										DQ16_A	DQ17_A
P	V _{SS}	V _{SS}																										V _{DD2}	V _{DD1}
R	V _{DD1}	V _{REFDQ_B}																										V _{SS}	CA0_B
T	V _{DD2}	V _{DD2}																										NC	CA1_B
U	V _{DDQ}	DQ3_B																										V _{REFCA_B}	CA2_B
V	DQ4_B	V _{SS}																										V _{SS}	CA3_B
W	DQ6_B	DQ5_B																										CA4_B	NC
Y	V _{DDQ}	DQ7_B																										CS_n_B	NC
AA	DQS0_l_B	DQS0_c_B																										V _{SS}	CKE_B
AB	DM0_B	V _{SS}																										CK_t_B	CK_c_B
AC	V _{DDQ}	DM1_B																										NC	CA5_B
AD	DQS1_c_B	DQS1_l_B																										CA7_B	CA6_B
AE	DQ8_B	V _{SS}																										CA8_B	NC
AF	DQ9_B	V _{DDQ}																										V _{SS}	CA9_B
AG	DQ10_B	DQ11_B																										V _{DD2}	ZQ_B
AH	V _{SS}	V _{DD1}	V _{DD2}	DQ13_B	V _{SS}	DQ15_B	DM3_B	DQS3_l_B	V _{DDQ}	DQ26_B	DQ27_B	V _{DDQ}	DQ30_B	V _{SS}	V _{DD2}	V _{REFCA_A}	CA9_A	V _{SS}	CA7_A	CA6_A	CK_c_A	NC	CKE_A	CS_n_A	CA3_A	CA2_A	CA1_A	V _{DD1}	V _{SS}
AJ	NC	V _{SS}	DQ12_B	V _{DDQ}	DQ14_B	V _{DDQ}	V _{SS}	DQS3_c_B	DQ24_B	DQ25_B	V _{SS}	DQ28_B	DQ29_B	DQ31_B	V _{DD1}	V _{SS}	ZQ_A	CA8_A	NC	CA5_A	CK_l_A	V _{SS}	NC	NC	CA4_A	NC	CA0_A	V _{SS}	NC

Top View (ball down)

Channel a (A)
 Channel b (B)
 Supply
 Ground

Ball Assignments

Figure 8: 220-Ball Dual-Channel FBGA – 2 x 4Gb Die



Top View (ball down)

Channel a (A)
 Channel b (B)
 Supply
 Ground

Ball Assignments

Figure 9: 216-Ball Dual-Channel FBGA – 4 x 4Gb Die

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	NC	V _{SS}	V _{DD2}	DQ30_A	DQ29_A	V _{SS}	DQ26_A	DQ25_A	V _{SS}	DQS3_c_A	V _{SS}	DQ14_A	DQ13_A	V _{SS}	V _{DD1}	V _{DD2}	DQ11_A	DQ10_A	DQ9_A	DQS1_L_A	DM1_A	V _{DDQ}	DQS0_L_A	DQ7_A	DQ6_A	DQ4_A	DQ3_A	V _{SS}	NC
B	V _{SS}	NC	DQ31_A	V _{DDQ}	DQ28_A	DQ27_A	V _{DDQ}	DQ24_A	V _{DDQ}	DQS3_L_A	DM3_A	DQ15_A	V _{DDQ}	V _{SS}	V _{REFDQ_A}	V _{DD2}	DQ12_A	V _{DDQ}	DQ8_A	DQS1_c_A	V _{SS}	DM0_A	DQS0_c_A	V _{SS}	V _{DDQ}	DQ5_A	DQ2_A	NC	V _{SS}
C	V _{DD1}	DQ16_B																										V _{DD1}	V _{DD2}
D	DQ17_B	V _{DDQ}																										DQ1_A	V _{DDQ}
E	DQ18_B	DQ19_B																										V _{SS}	DQ0_A
F	V _{SS}	DQ20_B																									DM2_A	V _{DDQ}	
G	DQ21_B	V _{DDQ}																										DQS2_L_A	DQS2_c_A
H	DQ22_B	DQ23_B																										V _{SS}	DQ23_A
J	V _{SS}	V _{DDQ}																										V _{DDQ}	DQ22_A
K	DQS2_c_B	DQS2_L_B																										DQ20_A	DQ21_A
L	DM2_B	DQ0_B																										DQ19_A	V _{SS}
M	DQ1_B	V _{SS}																										V _{DDQ}	DQ18_A
N	DQ2_B	V _{DD1}																										DQ16_A	DQ17_A
P	V _{SS}	V _{SS}																										V _{DD2}	V _{DD1}
R	V _{DD1}	V _{REFDQ_B}																										V _{SS}	CA0_B
T	V _{DD2}	V _{DD2}																										NC	CA1_B
U	V _{DDQ}	DQ3_B																										V _{REFCA_B}	CA2_B
V	DQ4_B	V _{SS}																										V _{SS}	CA3_B
W	DQ6_B	DQ5_B																										CA4_B	CS1_n_B
Y	V _{DDQ}	DQ7_B																										CS0_n_B	CKE1_B
AA	DQS0_L_B	DQS0_c_B																										V _{SS}	CKE0_B
AB	DM0_B	V _{SS}																										CK_t_B	CK_c_B
AC	V _{DDQ}	DM1_B																										NC	CA5_B
AD	DQS1_c_B	DQS1_L_B																										CA7_B	CA6_B
AE	DQ8_B	V _{SS}																										CA8_B	NC
AF	DQ9_B	V _{DDQ}																										V _{SS}	CA9_B
AG	DQ10_B	DQ11_B																										V _{DD2}	ZQ_B
AH	V _{SS}	V _{DD1}	V _{DD2}	DQ13_B	V _{SS}	DQ15_B	DM3_B	DQS3_L_B	V _{DDQ}	DQ26_B	DQ27_B	V _{DDQ}	DQ30_B	V _{SS}	V _{DD2}	V _{REFCA_A}	CA9_A	V _{SS}	CA7_A	CA6_A	CK_c_A	NC	CKE0_A	CS0_n_A	CA3_A	CA2_A	CA1_A	V _{DD1}	V _{SS}
AJ	NC	V _{SS}	DQ12_B	V _{DDQ}	DQ14_B	V _{DDQ}	V _{SS}	DQS3_c_B	DQ24_B	DQ25_B	V _{SS}	DQ28_B	DQ29_B	DQ31_B	V _{DD1}	V _{SS}	ZQ_A	CA8_A	NC	CA5_A	CK_L_A	V _{SS}	CKE1_A	CS1_n_A	CA4_A	NC	CA0_A	V _{SS}	NC

Top View (ball down)

Channel a (A)
 Channel b (B)
 Supply
 Ground

Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See Ball Assignments for information specific to this device.

Table 9: Ball/Pad Descriptions

Symbol	Type	Description
CA[9:0]_A, CA[9:0]_B	Input	Command/address inputs: Provide the command and address inputs according to the command truth table. A separate CA[9:0] is provided for each channel (A and B).
CK_t_A, CK_t_B CK_c_A, CK_c_B	Input	Clock: Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock. A separate CK_t/CK_c is provided for each channel (A and B).
CKE[1:0]_A, CKE[1:0]_B	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK. A separate CKE is provided for each channel (A and B).
CS[1:0]_n_A, CS[1:0]_n_B	Input	Chip select: Considered part of the command code and is sampled on the rising edge of CK. A separate CS_n is provided for each channel (A and B).
DM[3:0]_A, DM[3:0]_B	Input	Input data mask: Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively. A separate DM[3:0] is provided for each channel (A and B).
DQ[31:0]_A, DQ[31:0]_B	I/O	Data input/output: Bidirectional data bus. A separate DQ[11:0] is provided for each channel (A and B).
DQS[3:0]_t_A, DQS[3:0]_t_B, DQS[3:0]_c_A, DQS[3:0]_c_B	I/O	Data strobe: Bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively. A separate DQS[3:0]_t and DQS[3:0]_c is provided for each channel (A and B).
V _{DDQ} _A, V _{DDQ} _B	Supply	DQ power supply: Isolated on the die for improved noise immunity.
V _{SSQ} _A/B	Supply	DQ ground: Isolated on the die for improved noise immunity.
V _{DD1} _A/B	Supply	Core power: Supply 1.
V _{DD2} _A/B	Supply	Core power: Supply 2.
V _{SS} _A/B	Supply	Common ground.
V _{REFCA} _A, V _{REFCA} _B V _{REFDQ} _A, V _{REFDQ} _B	Supply	Reference voltage: V _{REFCA} is reference for command/address input buffers, V _{REFDQ} is reference for DQ input buffers. A separate V _{REFCA} and V _{REFDQ} provided for each channel (A and B).
ZQ_A, ZQ_B	Reference	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (RZQ), which is tied to V _{SSQ} . A separate ZQ is provided for each channel (A and B).
NU	–	Not usable: Do not connect.
NC	–	No connect: Not internally connected.
(NC)	–	No connect: Balls indicated as (NC) are no connects; however, they could be connected together internally.

Functional Description

Mobile LPDDR2 is a high-speed SDRAM internally configured as a 4- or 8-bank memory device. The device uses a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

The LPDDR2-S4 device uses a double data rate architecture on the DQ pins to achieve high-speed operation. The double data rate architecture is essentially a $4n$ prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single $4n$ -bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write access is burst oriented; access starts at a selected location and continues for a programmed number of locations in a programmed sequence.

Access begins with the registration of an ACTIVATE command followed by a READ or WRITE command. Registered address and BA bits that coincide with the ACTIVATE command are used to select the row and bank to be accessed. Registered address bits that coincide with the READ or WRITE command are used to select the bank and the starting column location for the burst access.