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LPDDR2 SDRAM

EDB8164B4PR, EDB8164B4PK, EDB8164B4PT, EDBA164B2PR

Features

- Ultra-low-voltage core and I/O power supplies
- Frequency range
  - 533 MHz (data rate: 1066 Mb/s/pin)
- 4*n* prefetch DDR architecture
- 8 internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on each CK_t/CK_c edge
- Bidirectional/differential data strobe per byte of data (DQS_t/DQS_c)
- Programmable READ and WRITE latencies (RL/WL)
- Burst length: 4, 8, and 16
- Per-bank refresh for concurrent operation
- Auto temperature-compensated self refresh (ATCSR) by built-in temperature sensor
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock-stop capability
- Lead-free (RoHS-compliant) and halogen-free packaging

Table 1: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL
1D	533	1066	8	4

Options — Marking

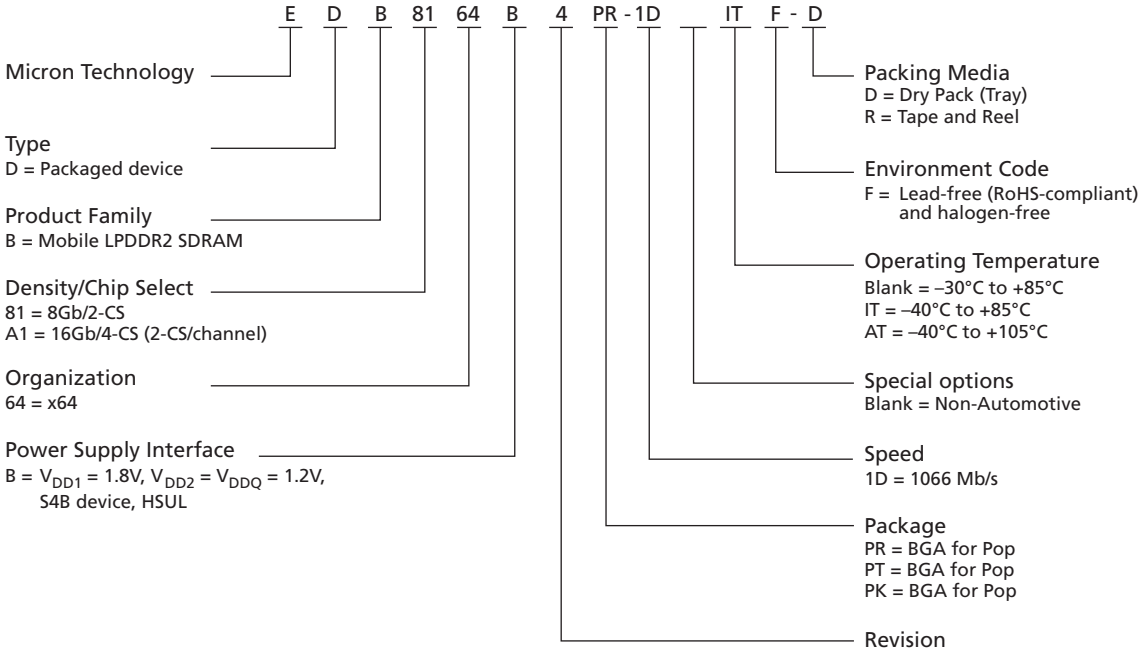
- Density/Page Size
  - 8Gb/2-CS – dual die — 81
  - 16Gb/4-CS – quad die — A1
- Organization
  - x64 — 64
- $V_{DD1}/V_{DD2}/V_{DDQ}$: 1.8V/1.2V/1.2V — B
- Revision
  - Dual die — 4
  - Quad die — 2
- FBGA "green" package
  - 12mm x 12mm x 0.8mm, 216-ball PoP FBGA package, dual die — PR
  - 12mm x 12mm x 0.8mm, 216-ball PoP FBGA package, dual die — PT
  - 12mm x 12mm x 1.0mm, 216-ball PoP FBGA package, quad die — PR
  - 14mm x 14mm x 0.7mm, 220-ball PoP FBGA package, dual die — PK
- Timing – cycle time
  - 1.875ns @ RL = 8 — -1D
- Special options
  - Non-Automotive — blank
- Operating temperature range
  - From –30°C to +85°C — blank
  - From –40°C to +85°C — IT
  - From –40°C to +105°C — AT

Table 2: S4 Configuration Addressing

Architecture	128 Meg x 64	256 Meg x 64
Die configuration	16 Meg x 32 x 8 banks x 2 channel	32 Meg x 32 x 8 banks x 2 channel
Row addressing	16K A[13:0]	16K A[13:0]
Column addressing	1K A[9:0]	1K A[9:0]
Number of die	2	4
Die per rank	1	2
Ranks per channel	1	2

Note: 1. A channel is a complete LPDRAM interface, including command/address and data pins.

Figure 1: LPDDR2 Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

Table 3: Package Codes and Descriptions

Package Code	Ball Count	# Ranks	# Chan-nels	Size (mm)	Die per Package	Solder Ball Composition
PR	216	1	2	12mm x 12mm x 0.80mm, 0.40 pitch	DDP	SAC302
PT	216	1	2	12mm x 12mm x 0.80mm, 0.40 pitch	DDP	SAC302
PR	216	2	2	12mm x 12mm x 1.00mm, 0.40 pitch	QDP	SAC302
PK	220	1	2	14mm x 14mm x 0.70mm, 0.50 pitch	DDP	SAC302

Notes: 1. DDP = dual-die package, QDP = quad-die package
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

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LPDDR2 Array Configuration

The 4Gb Mobile Low-Power DDR2 SDRAM (LPDDR2) is a high-speed CMOS, dynamic random-access memory containing 4,294,967,296-bits. The device is internally configured as an eight-bank DRAM. Each of the x16's 536,870,912-bit banks is organized as 16,384 rows by 2048 columns by 16 bits. Each of the x32's 536,870,912-bit banks is organized as 16,384 rows by 1024 columns by 32 bits.

General Notes

Throughout the data sheet, figures and text refer to DQs as "DQ." DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

"DQS" and "CK" should be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise. "BA" includes all BA pins used for a given density.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

I_{DD} Specifications

Table 4: I_{DD} Specifications – Dual Die, Dual Channel

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –40°C to +85°C

Symbol	Supply	Speed	Unit	Parameter/Condition
		1066		
I_{DD01}	V_{DD1}	16	mA	All devices in operating one bank active-precharge Conditions for operating devices are: ^tCK = ^tCK(avg) MIN; ^tRC = ^tRC (MIN); CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD02}	$V_{DDQ}V_{DDQ}$	100		
I_{DD2P1}	V_{DD1}	0.8	mA	All devices in idle power-down standby current ^tCK = ^tCK(avg) MIN; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD2P2}	$V_{DDQ}V_{DDQ}$	1.8		
I_{DD2PS1}	V_{DD1}	0.8	mA	All devices in idle power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD2PS2}	$V_{DDQ}V_{DDQ}$	1.8		
I_{DD2N1}	V_{DD1}	1.2	mA	All devices in idle non power-down standby current. ^tCK = ^tCK(avg) MIN; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD2N2}	$V_{DDQ}V_{DDQ}$	26		
I_{DD2NS1}	V_{DD1}	1.2	mA	All devices in idle non power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD2NS2}	$V_{DDQ}V_{DDQ}$	12		
I_{DD3P1}	V_{DD1}	1.6	mA	All devices in active power-down standby current ^tCK = ^tCK(avg) MIN; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD3P2}	$V_{DDQ}V_{DDQ}$	10		
I_{DD3PS1}	V_{DD1}	1.6	mA	All devices in active power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD3PS2}	$V_{DDQ}V_{DDQ}$	10		

Table 4: I_{DD} Specifications – Dual Die, Dual Channel (Continued)

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –40°C to +85°C

Symbol	Supply	Speed 1066	Unit	Parameter/Condition
I_{DD3N1}	V_{DD1}	2.4	mA	All devices in active non power-down standby current ^tCK = ^tCK(avg) MIN; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD3N2}	$V_{DDQ}V_{DDQ}$	38		
I_{DD3NS1}	V_{DD1}	2.4	mA	All devices in active non power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD3NS2}	$V_{DDQ}V_{DDQ}$	24		
I_{DD4R1}	V_{DD1}	4	mA	All devices in operating burst read ^tCK = ^tCK(avg) MIN; CS_n is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I_{DD4R2}	$V_{DDQ}V_{DDQ}$	840		
I_{DD4W1}	V_{DD1}	4	mA	All devices in operating burst write ^tCK = ^tCK(avg) MIN; CS_n is HIGH between valid commands; One bank is active; BL = 4; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I_{DD4W2}	$V_{DDQ}V_{DDQ}$	300		
I_{DD51}	V_{DD1}	40	mA	All devices in all bank auto-refresh ^tCK = ^tCK(avg) MIN; CKE is HIGH between valid commands; ^tRC = ^tRFCab (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD52}	$V_{DDQ}V_{DDQ}$	240		
I_{DD5AB1}	V_{DD1}	8	mA	All devices in all bank auto-refresh ^tCK = ^tCK(avg) MIN; CKE is HIGH between valid commands; ^tRC = ^tREFI; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD5AB2}	$V_{DDQ}V_{DDQ}$	40		
I_{DD5PB1}	V_{DD1}	8	mA	All devices in per bank auto-refresh ^tCK = ^tCK(avg) MIN; CKE is HIGH between valid commands; ^tRC = ^tREFIpb; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD5PB2}	$V_{DDQ}V_{DDQ}$	40		

Notes:
1. Published I_{DD} values are the maximum of the distribution of the arithmetic mean.
2. I_{DD} current specifications are tested after the device is properly initialized.

3. V_{DD2} and V_{DDQ} are connected internally in the package.
4. The Quad die product I_{DD} for each channel will be the sum of the I_{DD}'s for the state of operation for each rank (CS) in the channel.

Table 5: I_{DD6} Full-Array Self Refresh Current at 45°C for Dual die product

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V_{DD1}	400	µA	All devices in self refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	$V_{DDQ}V_{DDQ}$	1600		
1/2 array	V_{DD1}	320		
	$V_{DDQ}V_{DDQ}$	1000		
1/4 array	V_{DD1}	260		
	$V_{DDQ}V_{DDQ}$	600		
1/8 array	V_{DD1}	240		
	$V_{DDQ}V_{DDQ}$	400		

Note: 1. I_{DD6} 45°C is the typical of the distribution of the arithmetic mean, Quad die product will be double these values when all die are in self refresh mode.

Table 6: I_{DD6} Partial-Array Self Refresh Current at 85°C for Dual die product

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V_{DD1}	1800	µA	All devices in self refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	$V_{DDQ}V_{DDQ}$	6400		
1/2 array	V_{DD1}	1300		
	$V_{DDQ}V_{DDQ}$	4400		
1/4 array	V_{DD1}	1100		
	$V_{DDQ}V_{DDQ}$	3400		
1/8 array	V_{DD1}	1000		
	$V_{DDQ}V_{DDQ}$	2800		

Note: 1. I_{DD6} 85°C is the maximum of the distribution of the arithmetic mean, Quad die product will be double these values when all die are in self refresh mode.

Table 7: I_{DD} Specifications – Dual Die, Dual Channel

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –40°C to +105°C

Symbol	Supply	Speed	Unit	Parameter/Condition
		1066		
I_{DD01}	V_{DD1}	16	mA	All devices in operating one bank active-precharge Conditions for operating devices are: ^tCK = ^tCK(avg) MIN; ^tRC = ^tRC (MIN); CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD02}	V_{DD2}, V_{DDQ}	100		
I_{DD2P1}	V_{DD1}	0.8	mA	All devices in idle power-down standby current ^tCK = ^tCK(avg) MIN; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD2P2}	V_{DD2}, V_{DDQ}	1.8		
I_{DD2PS1}	V_{DD1}	0.8	mA	All devices in idle power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD2PS2}	V_{DD2}, V_{DDQ}	1.8		
I_{DD2N1}	V_{DD1}	1.2	mA	All devices in idle non power-down standby current. ^tCK = ^tCK(avg) MIN; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD2N2}	V_{DD2}, V_{DDQ}	30		
I_{DD2NS1}	V_{DD1}	1.2	mA	All devices in idle non power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD2NS2}	V_{DD2}, V_{DDQ}	16		
I_{DD3P1}	V_{DD1}	1.8	mA	All devices in active power-down standby current ^tCK = ^tCK(avg) MIN; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD3P2}	V_{DD2}, V_{DDQ}	14		
I_{DD3PS1}	V_{DD1}	1.8	mA	All devices in active power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD3PS2}	V_{DD2}, V_{DDQ}	14		
I_{DD3N1}	V_{DD1}	2.8	mA	All devices in active non power-down standby current ^tCK = ^tCK(avg) MIN; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD3N2}	V_{DD2}, V_{DDQ}	44		

Table 7: I_{DD} Specifications – Dual Die, Dual Channel (Continued)

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –40°C to +105°C

Symbol	Supply	Speed	Unit	Parameter/Condition
		1066		
I_{DD3NS1}	V_{DD1}	2.8	mA	All devices in active non power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD3NS2}	V_{DD2}, V_{DDQ}	30		
I_{DD4R1}	V_{DD1}	4	mA	All devices in operating burst read ^tCK = ^tCK(avg) MIN; CS_n is HIGH between valid commands; One bank is active; BL = 4; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I_{DD4R2}	V_{DD2}, V_{DDQ}	840		
I_{DD4W1}	V_{DD1}	4	mA	All devices in operating burst write ^tCK = ^tCK(avg) MIN; CS_n is HIGH between valid commands; One bank is active; BL = 4; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I_{DD4W2}	V_{DD2}, V_{DDQ}	300		
I_{DD51}	V_{DD1}	40	mA	All devices in all bank auto-refresh ^tCK = ^tCK(avg) MIN; CKE is HIGH between valid commands; ^tRC = ^tRFCab (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD52}	V_{DD2}, V_{DDQ}	240		
I_{DD5AB1}	V_{DD1}	12	mA	All devices in all bank auto-refresh ^tCK = ^tCK(avg) MIN; CKE is HIGH between valid commands; ^tRC = ^tREFI; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD5AB2}	V_{DD2}, V_{DDQ}	56		
I_{DD5PB1}	V_{DD1}	12	mA	All devices in per bank auto-refresh ^tCK = ^tCK(avg) MIN; CKE is HIGH between valid commands; ^tRC = ^tREFIpb; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD5PB2}	V_{DD2}, V_{DDQ}	56		

Notes:
1. Published I_{DD} values are the maximum of the distribution of the arithmetic mean.
2. I_{DD} current specifications are tested after the device is properly initialized.
3. V_{DD2} and V_{DDQ} are connected internally in the package.
4. The Quad die product I_{DD} for each channel will be the sum of the I_{DD}'s for the state of operation for each rank (CS) in the channel.

Table 8: I_{DD6} Partial-Array Self Refresh Current at 105°C Dual die for Dual die prodct

V_{DD2}, V_{DDQ} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V_{DD1}	4800	µA	All devices in self refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	$V_{DDQ}V_{DDQ}$	28000		
1/2 array	V_{DD1}	3200		
	$V_{DDQ}V_{DDQ}$	15600		
1/4 array	V_{DD1}	2200		
	$V_{DDQ}V_{DDQ}$	9600		
1/8 array	V_{DD1}	1800		
	$V_{DDQ}V_{DDQ}$	6400		

Note: 1. I_{DD6} 105°C is the maximum of the distribution of the arithmetic mean, Quad die product will be double these values when all die are in self refresh mode.

Package Block Diagrams

Figure 2: Dual Die Single Rank, Dual Channel Package Block Diagram

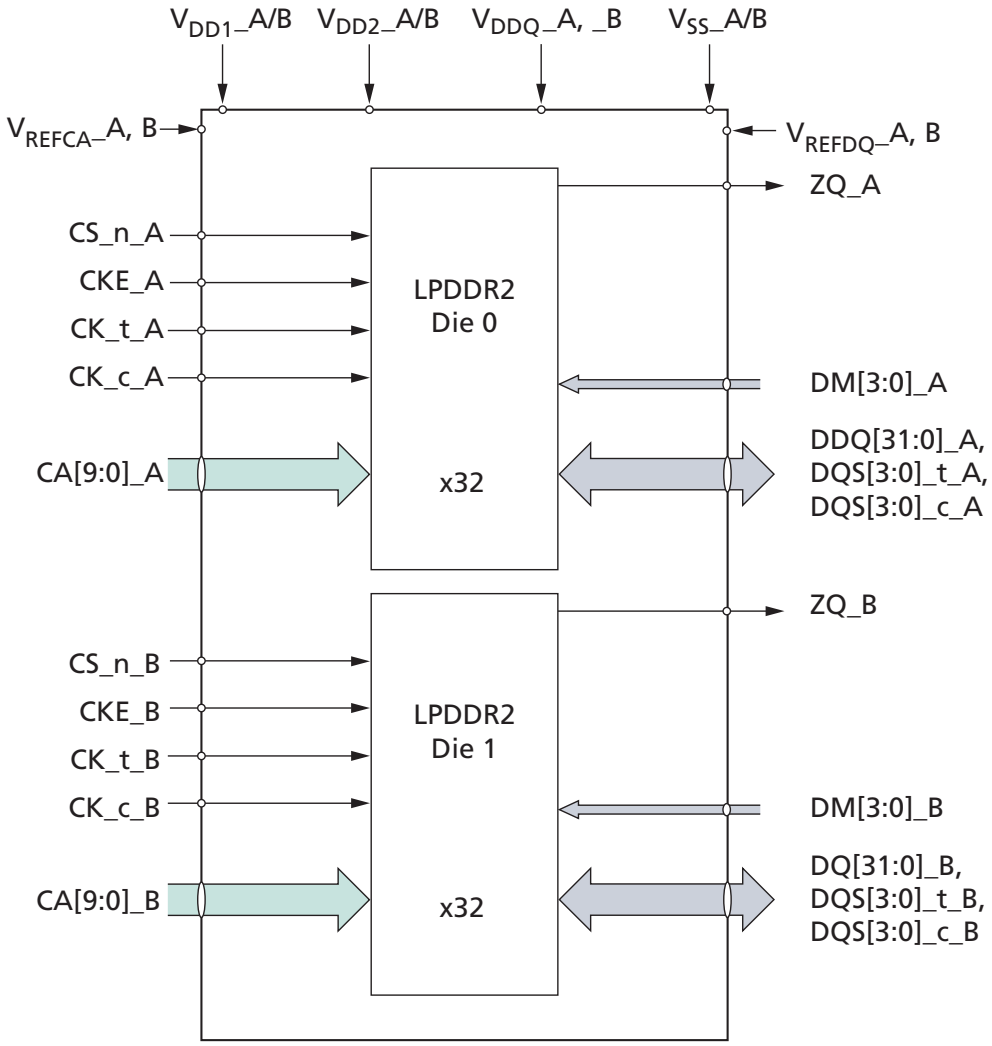
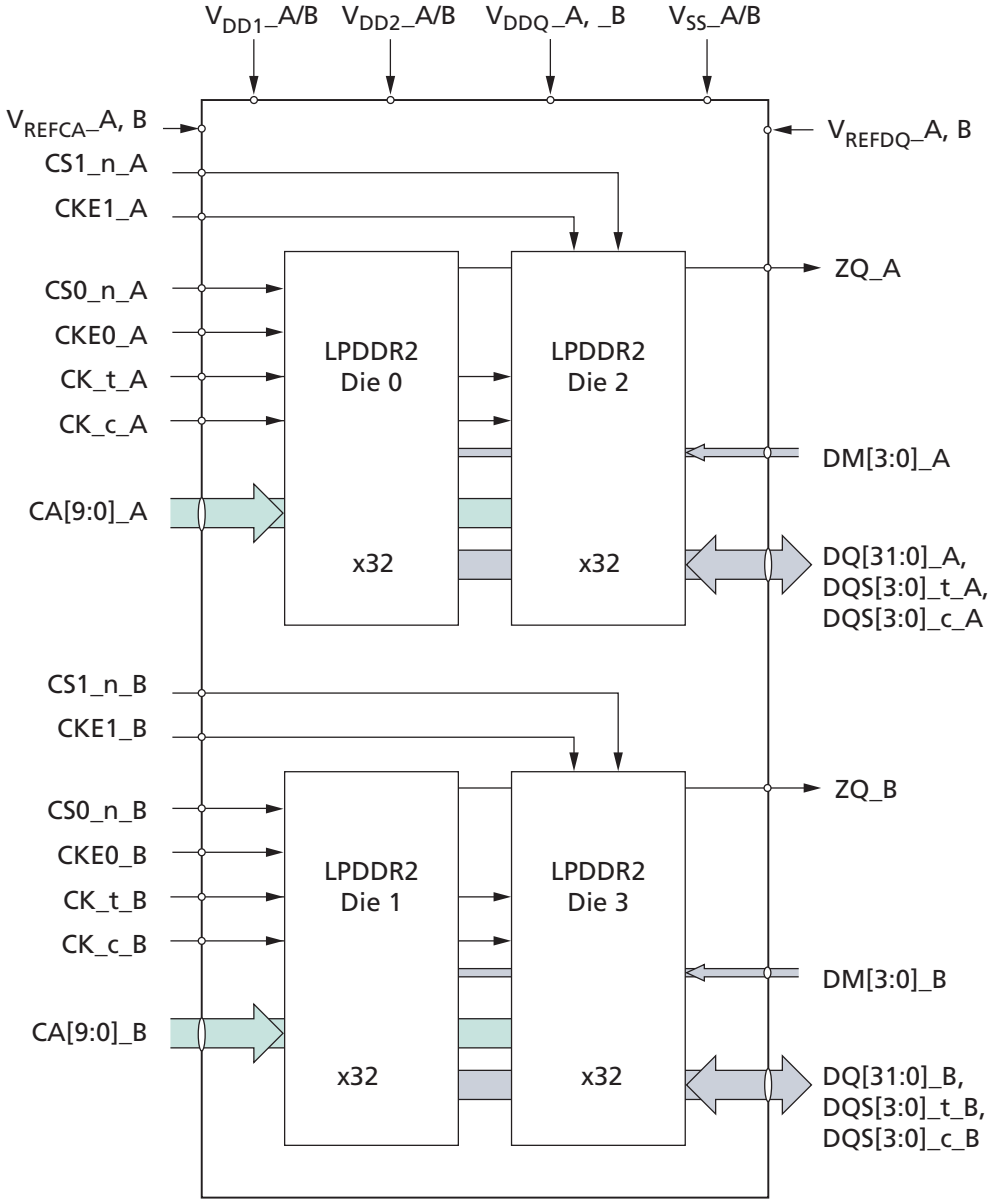
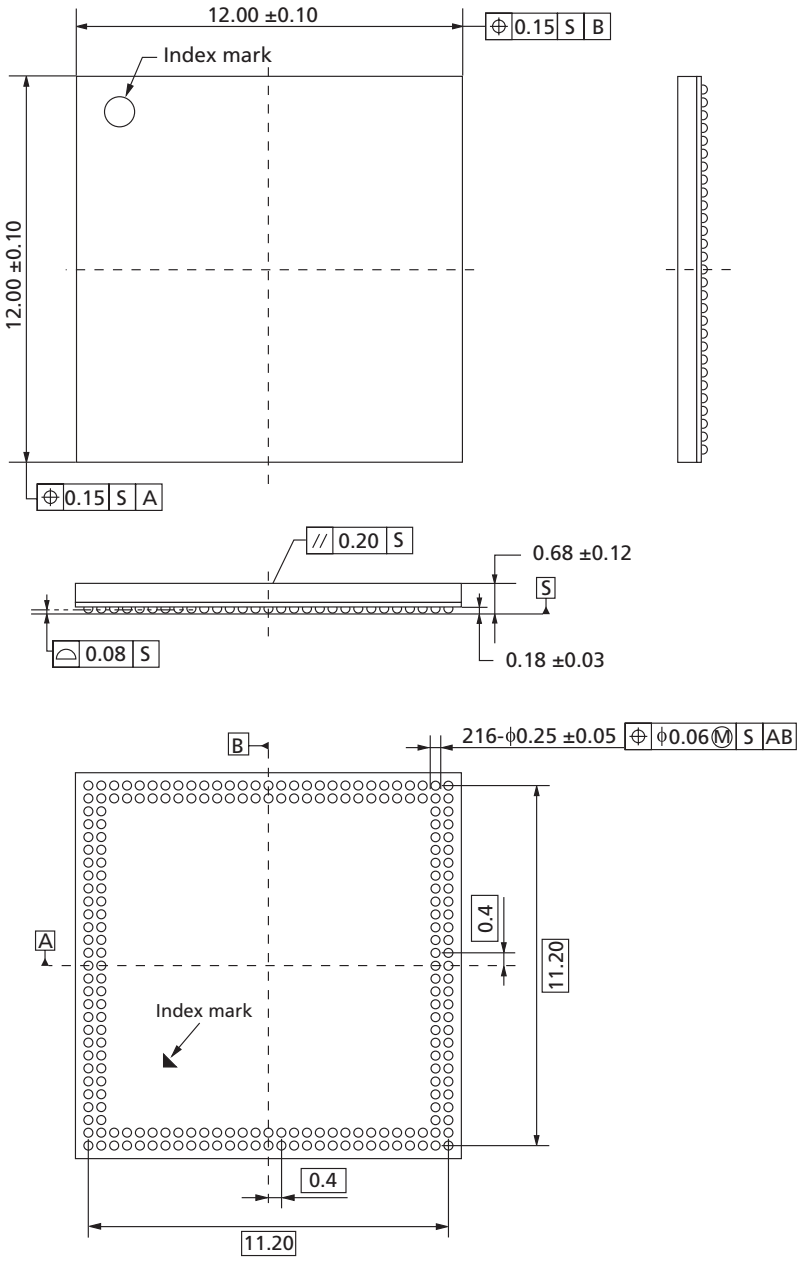


Figure 3: Quad Die Dual Rank, Dual Channel Package Block Diagram



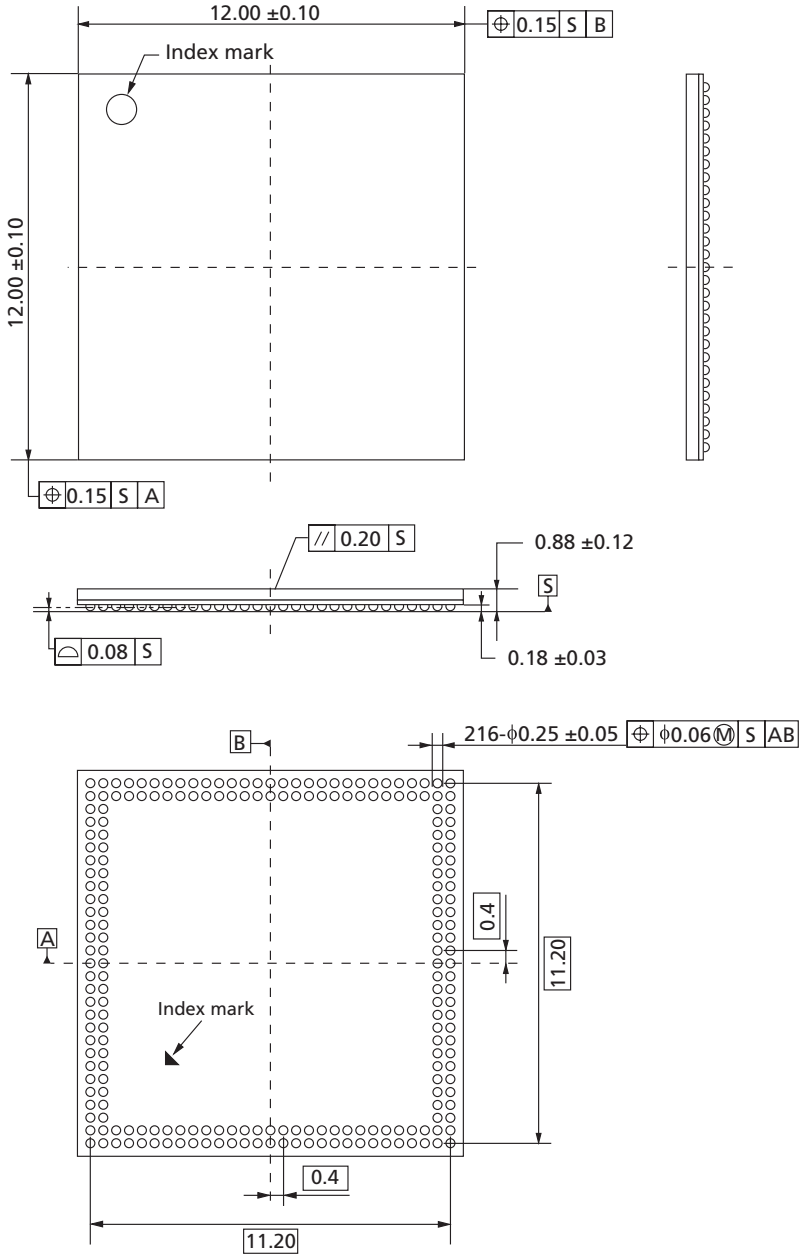
Package Dimensions

Figure 4: 216-Ball FBGA (12mm x 12mm x 0.8mm) – EDB8164B4PR, EDB8164B4PT



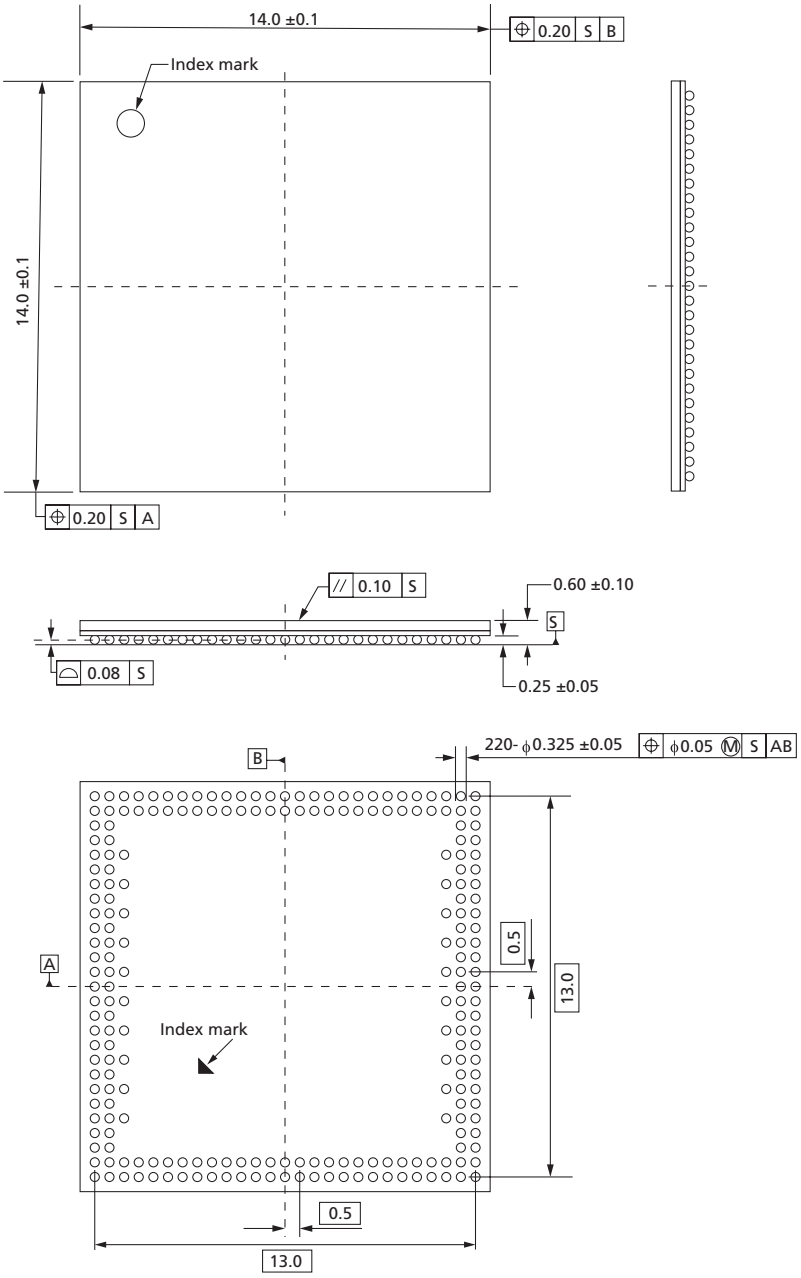
Note: 1. All dimensions are in millimeters.

Figure 5: 216-Ball FBGA (12mm x 12mm x 1.0mm) – EDBA164B2PR



Note: 1. All dimensions are in millimeters.

Figure 6: 220-Ball FBGA (14mm x 14mm x 0.7mm) – EDB8164B4PK



Note: 1. All dimensions are in millimeters.

Ball Assignments

Figure 7: 216-Ball Dual-Channel FBGA – 2 x 4Gb Die

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	NC	V_{SS}	V_{DD2}	DQ30_A	DQ29_A	V_{SS}	DQ26_A	DQ25_A	V_{SS}	DQS3_c_A	V_{SS}	DQ14_A	DQ13_A	V_{SS}	V_{DD1}	V_{DD2}	DQ11_A	DQ10_A	DQ9_A	DQS1_t_A	DM1_A	V_{DDQ}	DQS0_t_A	DQ7_A	DQ6_A	DQ4_A	DQ3_A	V_{SS}	NC
B	V_{SS}	NC	DQ31_A	V_{DDQ}	DQ28_A	DQ27_A	V_{DDQ}	DQ24_A	V_{DDQ}	DQS3_t_A	DM3_A	DQ15_A	V_{DDQ}	V_{SS}	V_{REFDQ_A}	V_{DD2}	DQ12_A	V_{DDQ}	DQ8_A	DQS1_c_A	V_{SS}	DM0_A	DQS0_c_A	V_{SS}	V_{DDQ}	DQ5_A	DQ2_A	NC	V_{SS}
C	V_{DD1}	DQ16_B																										V_{DD1}	V_{DD2}
D	DQ17_B	V_{DDQ}																										DQ1_A	V_{DDQ}
E	DQ18_B	DQ19_B																										V_{SS}	DQ0_A
F	V_{SS}	DQ20_B																										DM2_A	V_{DDQ}
G	DQ21_B	V_{DDQ}																										DQS2_t_A	DQS2_c_A
H	DQ22_B	DQ23_B																										V_{SS}	DQ23_A
J	V_{SS}	V_{DDQ}																										V_{DDQ}	DQ22_A
K	DQS2_c_B	DQS2_t_B																										DQ20_A	DQ21_A
L	DM2_B	DQ0_B																										DQ19_A	V_{SS}
M	DQ1_B	V_{SS}																										V_{DDQ}	DQ18_A
N	DQ2_B	V_{DD1}																										DQ16_A	DQ17_A
P	V_{SS}	V_{SS}																										V_{DD2}	V_{DD1}
R	V_{DD1}	V_{REFDQ_B}																										V_{SS}	CA0_B
T	V_{DD2}	V_{DD2}																										NC	CA1_B
U	V_{DDQ}	DQ3_B																										V_{REFCA_B}	CA2_B
V	DQ4_B	V_{SS}																										V_{SS}	CA3_B
W	DQ6_B	DQ5_B																										CA4_B	NC
Y	V_{DDQ}	DQ7_B																										CS_n_B	NC
AA	DQS0_t_B	DQS0_c_B																										V_{SS}	CKE_B
AB	DM0_B	V_{SS}																										CK_t_B	CK_c_B
AC	V_{DDQ}	DM1_B																										NC	CA5_B
AD	DQS1_c_B	DQS1_t_B																										CA7_B	CA6_B
AE	DQ8_B	V_{SS}																										CA8_B	NC
AF	DQ9_B	V_{DDQ}																										V_{SS}	CA9_B
AG	DQ10_B	DQ11_B																										V_{DD2}	ZQ_B
AH	V_{SS}	V_{DD1}	V_{DD2}	DQ13_B	V_{SS}	DQ15_B	DM3_B	DQS3_t_B	V_{DDQ}	DQ26_B	DQ27_B	V_{DDQ}	DQ30_B	V_{SS}	V_{DD2}	V_{REFCA_A}	CA9_A	V_{SS}	CA7_A	CA6_A	CK_c_A	NC	CKE_A	CS_n_A	CA3_A	CA2_A	CA1_A	V_{DD1}	V_{SS}
AJ	NC	V_{SS}	DQ12_B	V_{DDQ}	DQ14_B	V_{DDQ}	V_{SS}	DQS3_c_B	DQ24_B	DQ25_B	V_{SS}	DQ28_B	DQ29_B	DQ31_B	V_{DD1}	V_{SS}	ZQ_A	CA8_A	NC	CA5_A	CK_t_A	V_{SS}	NC	NC	CA4_A	NC	CA0_A	V_{SS}	NC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29

Top View (ball down)

Channel a (_A) Channel b (_B) Supply Ground

Ball Assignments

Figure 8: 220-Ball Dual-Channel FBGA – 2 x 4Gb Die

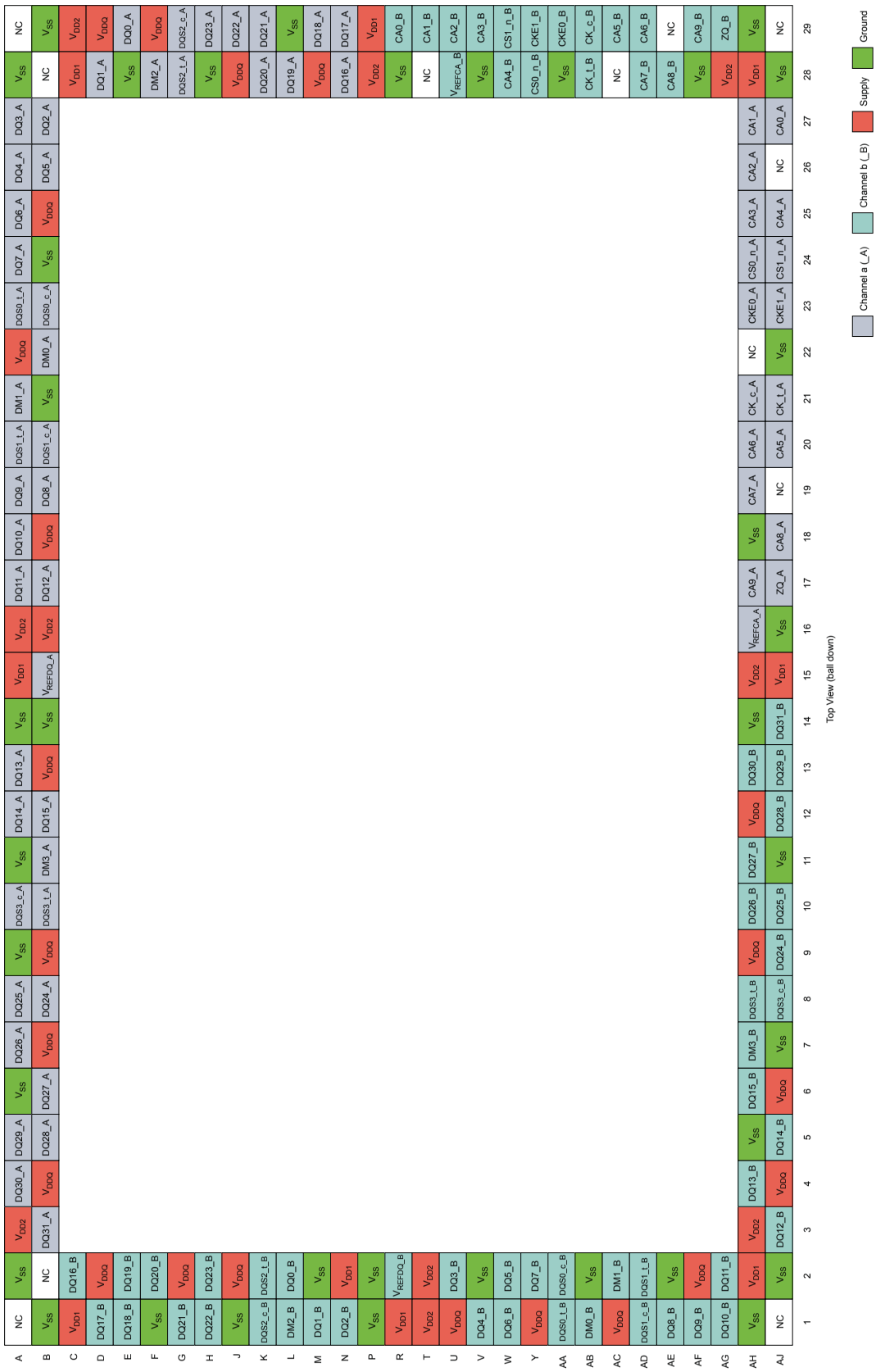
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	NC	V_{SS}	V_{DD2}	V_{SS}	DQ29_B	DQ28_B	V_{SS}	DQ25_B	DQ24_B	DQS3_c_B	DM3_B	DQ15_B	V_{SS}	DQ13_B	DQ11_B	V_{SS}	DQ9_B	DQS1_c_B	DM1_B	V_{SS}	V_{SS}	V_{DD2}	DQS0_c_B	DQ7_B	V_{SS}	V_{SS}	NC	A
B	V_{DD1}	NC	V_{DDQ}	DQ31_B	DQ30_B	V_{DDQ}	DQ27_B	DQ26_B	V_{DDQ}	DQS3_t_B	V_{SS}	V_{DDQ}	DQ14_B	DQ12_B	V_{DDQ}	DQ10_B	DQ8_B	DQS1_t_B	V_{DDQ}	V_{REFDQ_B}	V_{DD1}	DM0_B	DQS0_t_B	V_{DDQ}	DQ6_B	NC	V_{DD2}	B
C	DQ16_A	DQ17_A																								DQ5_B	DQ4_B	C
D	DQ18_A	V_{DDQ}																								V_{DDQ}	DQ3_B	D
E	V_{SS}	DQ20_A	DQ19_A																						DQ2_B	DQ1_B	V_{SS}	E
F	DQ21_A	V_{DDQ}																								V_{DDQ}	DQ0_B	F
G	V_{SS}	DQ22_A	DQ23_A																						DM2_B	DQS2_t_B	V_{SS}	G
H	DQS2_t_A	DQS2_c_A																								DQS2_c_B	DQ23_B	H
J	V_{SS}	DM2_A	DQ0_A																						DQ21_B	DQ22_B	V_{SS}	J
K	DQ1_A	V_{DDQ}																								V_{DDQ}	DQ20_B	K
L	V_{SS}	DQ2_A	DQ3_A																						DQ19_B	DQ18_B	V_{SS}	L
M	DQ4_A	V_{DDQ}																								V_{DD2}	DQ17_B	M
N	V_{SS}	DQ5_A	DQ6_A																						DQ16_B	V_{DDQ}	V_{SS}	N
P	DQ7_A	V_{DDQ}																								NC	CA0_A	P
R	V_{SS}	DQS0_c_A	DQS0_t_A																						CA1_A	CA2_A	V_{SS}	R
T	DM0_A	V_{DDQ}																								CA3_A	CA4_A	T
U	V_{SS}	V_{SS}	V_{REFDQ_A}																						CS0_n_A	NC	V_{SS}	U
V	V_{DD2}	V_{DD1}																								CKE0_A	NC	V
W	V_{SS}	V_{DD2}	DM1_A																						CK_c_A	CK_t_A	V_{SS}	W
Y	DQS1_c_A	DQS1_t_A																								NC	CA5_A	Y
AA	V_{SS}	DQ9_A	DQ10_A																						V_{REFCA_A}	CA6_A	V_{DD2}	AA
AB	DQ8_A	V_{DDQ}																								CA7_A	V_{SS}	AB
AC	V_{SS}	DQ11_A	DQ12_A																						CA8_A	CA9_A	V_{SS}	AC
AD	DQ13_A	DQ14_A																								NC	V_{DD2}	AD
AE	V_{SS}	DQ15_A																								V_{DD1}	ZQ_A	AE
AF	V_{SS}	V_{DDQ}	DM3_A	DQS3_t_A	DQS3_c_A	DQ25_A	DQ27_A	V_{DDQ}	DQ29_A	DQ31_A	V_{DD2}	V_{DD1}	NC	CA9_B	CA7_B	V_{DD2}	V_{REFCA_B}	NC	CK_t_B	NC	CS0_n_B	CA4_B	NC	CA2_B	CA0_B	V_{DD2}	V_{SS}	AF
AG	NC	V_{DD2}	V_{SS}	V_{DDQ}	DQ24_A	DQ26_A	V_{SS}	DQ28_A	DQ30_A	V_{SS}	V_{SS}	ZQ_B	V_{SS}	CA8_B	CA6_B	CA5_B	V_{SS}	V_{SS}	CK_c_B	CKE0_B	NC	V_{SS}	CA3_B	CA1_B	V_{SS}	V_{DD1}	NC	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

Top View (ball down)

Channel a (_A) Channel b (_B) Supply Ground

Ball Assignments

Figure 9: 216-Ball Dual-Channel FBGA – 4 x 4Gb Die



Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See Ball Assignments for information specific to this device.

Table 9: Ball/Pad Descriptions

Symbol	Type	Description
CA[9:0]_A, CA[9:0]_B	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table. A separate CA[9:0] is provided for each channel (A and B).
CK_t_A, CK_t_B CK_c_A, CK_c_B	Input	**Clock:** Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock. A separate CK_t/CK_c is provided for each channel (A and B).
CKE[1:0]_A, CKE[1:0]_B	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK. A separate CKE is provided for each channel (A and B).
CS[1:0]_n_A, CS[1:0]_n_B	Input	**Chip select:** Considered part of the command code and is sampled on the rising edge of CK. A separate CS_n is provided for each channel (A and B).
DM[3:0]_A, DM[3:0]_B	Input	**Input data mask:** Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively. A separate DM[3:0] is provided for each channel (A and B).
DQ[31:0]_A, DQ[31:0]_B	I/O	**Data input/output:** Bidirectional data bus. A separate DQ[11:0] is provided for each channel (A and B).
DQS[3:0]_t_A, DQS[3:0]_t_B, DQS[3:0]_c_A, DQS[3:0]_c_B	I/O	**Data strobe:** Bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively. A separate DQS[3:0]_t and DQS[3:0]_c is provided for each channel (A and B).
V_{DDQ}_A, V_{DDQ}_B	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}_A/B	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
V_{DD1} _A/B	Supply	**Core power:** Supply 1.
V_{DD2}_A/B	Supply	**Core power:** Supply 2.
V_{SS}_A/B	Supply	**Common ground.**
V_{REFCA}_A, V_{REFCA}_B V_{REFDQ}_A, V_{REFDQ}_B	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers. A separate V_{REFCA} and V_{REFDQ} provided for each channel (A and B).
ZQ_A, ZQ_B	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}. A separate ZQ is provided for each channel (A and B).
NU	–	**Not usable:** Do not connect.
NC	–	**No connect:** Not internally connected.
(NC)	–	**No connect:** Balls indicated as (NC) are no connects; however, they could be connected together internally.

Functional Description

Mobile LPDDR2 is a high-speed SDRAM internally configured as a 4- or 8-bank memory device. The device uses a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

The LPDDR2-S4 device uses a double data rate architecture on the DQ pins to achieve high- speed operation. The double data rate architecture is essentially a 4*n* prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write access is burst oriented; access starts at a selected location and continues for a programmed number of locations in a programmed sequence.

Access begins with the registration of an ACTIVATE command followed by a READ or WRITE command. Registered address and BA bits that coincide with the ACTIVATE command are used to select the row and bank to be accessed. Registered address bits that coincide with the READ or WRITE command are used to select the bank and the starting column location for the burst access.