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Enhanced Universal Platform System-on-Chip Processor

EDB9315A

Engineering Development Board

Technical Reference Manual

AUG '06
DS638DB3

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Table of Contents

List of Figures

1. EDB9315A Kit Contents

Each EDB9315A kit comes with the following:

- EDB9315A Development Board
- Null Modem Serial Cable
- Power Supply: +12V, 5A, 110V/220V with AC Power Cord
- Quick Start Guide
- Registration Card
- (2) IDC10-to-DB9 Cables
- IDE Ribbon Cable
- HDD Power Cable
- 3.5"-to-2.5" Notebook HDD Adapter
- 4x1 Header to HDD Power Connector Adapter
- IAR™ Evaluation CD
- Quick Start Guide
- Board Registration Card
- Trial Software Download Information Card

All documentation, schematics, software, utilities, and related information is available from the download section of the Cirrus Logic ARM Developer's web site, http://arm.cirrus.com.

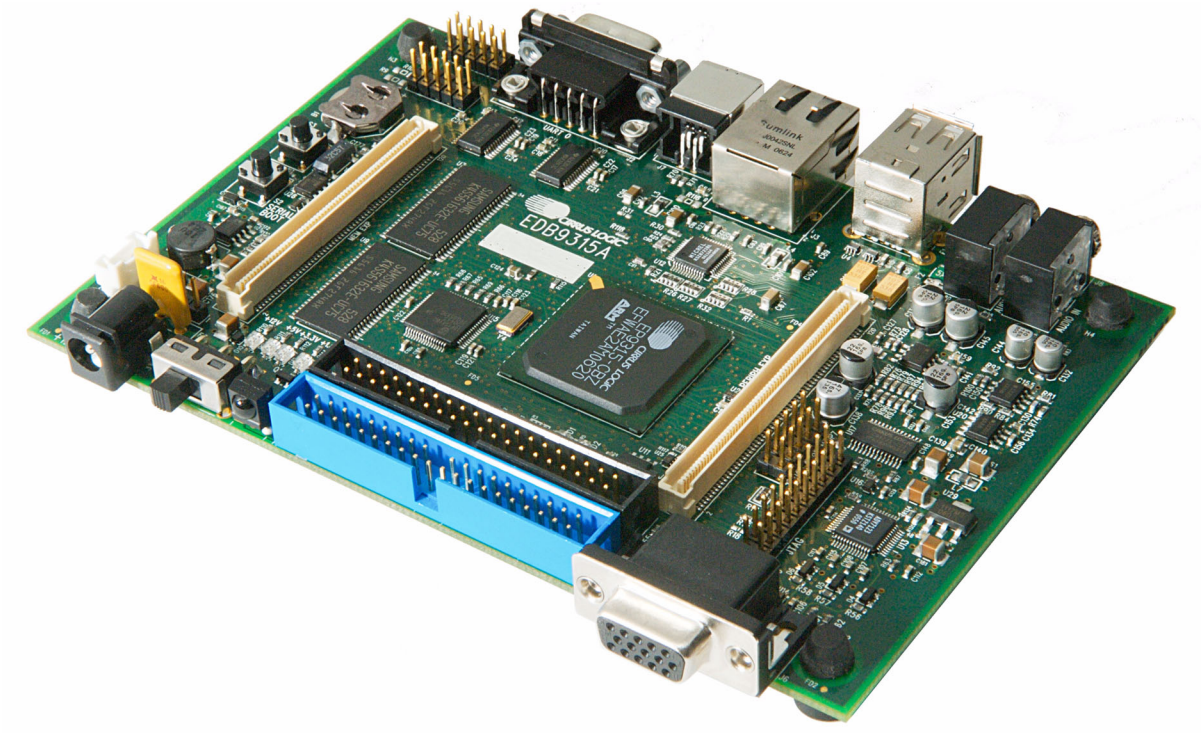

Figure 1. EDB9315A Board

2. Introducing the EDB9315A Engineering Development Board

This document will describe the features and basic operation of the EDB9315A board developed by Cirrus Logic. Detailed information regarding the operation and programming of the EP9315 device are covered by the EP9315 datasheet and User's Guide on the Cirrus Logic web site.

The EDB9315A is a convenient and easy-to-operate evaluation platform. It has been designed to provide the majority of the EP9315 functions on a small 6" x 4" base board. These features include:

- EP9315 Processor Running at 200MHz
- 64MByte SDRAM
- 16MByte NOR Flash Memory
- Two USB 2.0 Full-speed Host Ports
- USB 2.0 High-speed Device Interface
- Audio Out
- Audio In
- Three UARTs
- 10/100 Ethernet Interface
- VGA
- IDE
- JTAG
- Consumer IR (CIR)
- Expansion Connectors
- LCD Interface with Touch Screen Support

Note: The EDB9315A kit does not include a LCD screen. The LCD interface is pin-compatible with previous Cirrus Logic development boards.

Not all features of the EP9315 are on the base board. Two high-density connectors have been provided to allow for daughter card expansion. The full memory bus is connected to one of the connectors and any peripherals not on the development board are attached to the other connector. In addition, some features such as Ethernet MII interface have been brought out to the peripheral connector as well.

2.1 Identifying What's on the Board

Figure 2 shows the top side of the EDB9315A. The accompanying legend identifies the main components of the board.

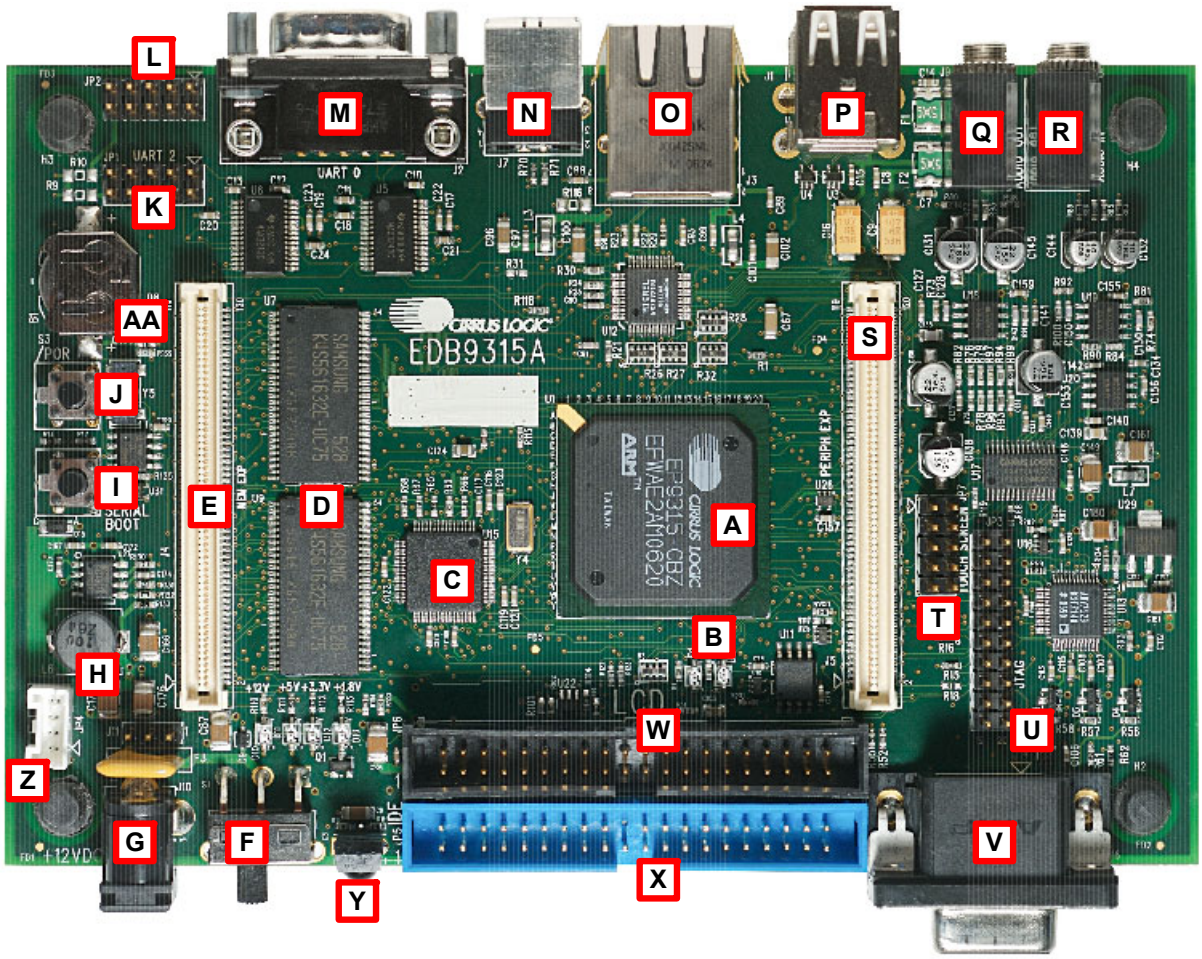

Figure 2. EDB9315A Top View

A. EP9315 processor
B. Processor Status LEDs - one Red and one Green
C. USB 2.0 High-speed Device IC (ISP1581)
D. SDRAM - 2 16-bit devices
E. Memory Bus Expansion Connector
F. Main Power Switch, S1
G. 12V Power Connector
H. 3.3V Voltage Regulator - switching, 3A
I. Serial Boot Pushbutton - labeled "SERIAL BOOT"
J. Reset Pushbutton - labeled "/POR"
K. UART2 Header - 5x2
L. UART1 Header - 5x2
M. UART0, DB9 Male
N. USB Device Connector
O. Ethernet Connector
P. Dual, Stacked USB Host Connector
Q. Audio Out Connector
R. Audio In Connector
S. Peripheral Bus Expansion Connector
T. Touch Screen Connector
U. JTAG Connector
V. VGA Connector - DB15, female
W. LCD Connector
X. IDE Connector
Y. Commercial IR
Z. IDE Power Connector, +12V, +5V, GND
AA. RTC and Battery Backup

One item not listed above is the Flash device. It is located on the bottom side of the board, under item C.

There are no jumpers on the board. The only "jumper" is the serial boot pushbutton. This button is used when the developer wants to use the Cirrus Logic download utility to put new code into Flash memory.

3. Getting Started

3.1 Before you Begin...

The developer will find it useful to have some additional hardware not provided in the EDB9315A kit. Items such as a USB mouse, USB keyboard, VGA monitor and cable, and a set of powered speakers can make using the EDB9315A and the software installed on the board more enjoyable.

Caution: Make sure you are in a static-free environment and are following proper procedures for handling ESD-sensitive electronic equipment.

3.2 Attaching Cables

Before attaching cables to the board make sure you know where pin 1 for each of the connectors is located. Most connectors are keyed. However, some connectors use 2 x n headers, allowing the cable to be plugged in backwards. Prime examples of this are the Touch Screen and JTAG connectors.

There is silkscreen on the PCB identifying each connector and its pin 1 location. Make sure to pay attention to the markings on the PCB for the pin 1 location. The pin 1 identifier is marked by either a number or a triangle.

3.3 Before Applying Power...

In order to use the EDB9315A the user must first connect the peripherals to the EDB9315A as described in the following procedure.

1. Place the EDB9315A on a static free surface.
2. Make sure power switch S1 is in the OFF position.
3. Connect the 12V power supply provided to the board at J10.
4. Connect null modem serial cable provided in the kit from DB9 connector J2 to a serial port on a PC or notebook (if so equipped).
5. Connect a VGA monitor to DB15 connector J6.
6. Launch a terminal program, such as minicom or HyperTerminal. Configure the PC com port for: 38400 baud, 8 data bits, no parity, 1 stop bit, no flow control for WinCE and 57600 baud for Linux.
7. Connect the board to a network that has internet access (optional)
8. Connect a USB mouse and keyboard.
9. Turn power switch S1 to the ON position and the board will boot and shortly display the WinCE 5.0 or

the Qt/Opie desktop on the VGA monitor, depending which OS you have programmed into the board. The EDB9315A comes with WinCE 5.0 installed.

NOTE: The WinCE 5.0 binary is not provided on the support web site. If you erase the image on the board, you will have to download the BSP provided by Cirrus Logic and compile it using Platform Builder.

Due to changes in distribution policy, the Microsoft trial CD/DVD that was formerly included in the kit is no longer available. Please refer to the card in the kit that describes how to download the Microsoft trial software from the Microsoft web site.

4. EDB9315A Circuit Description

This chapter makes reference to the schematics in Appendix A and discusses the main circuit functionality of each schematic page. A detailed block diagram of the EDB9315A Engineering Development Board is shown below.

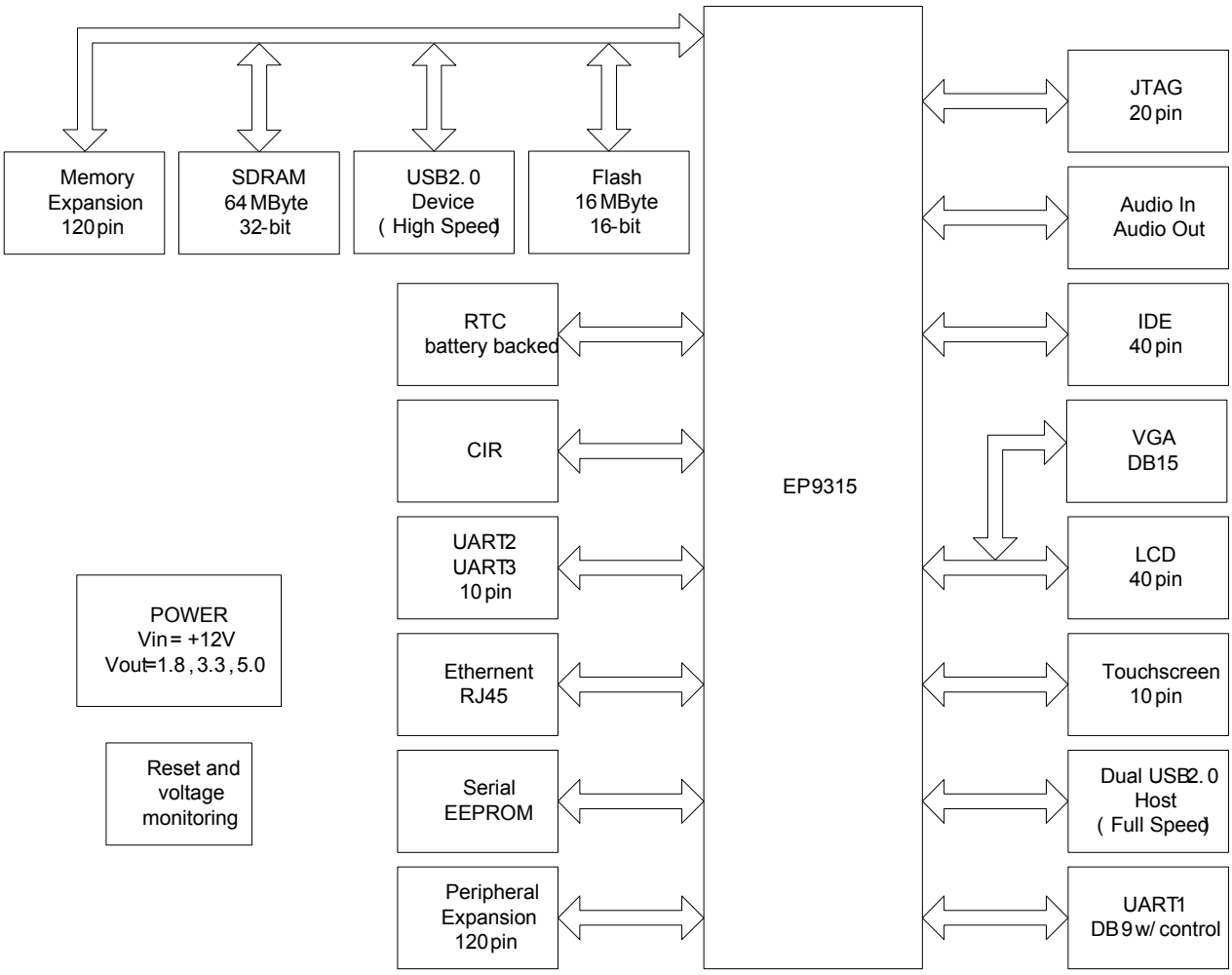

Figure 3. Block Diagram

Detailed information regarding the EP9315 processor and interfaces can be found at www.cirrus.com. The details of this device will not be discussed in this document. Refer to the EP9315 datasheet, User's Guide, and other information on the web site for more information.

4.1 Circuit Operation

The major circuit operation for each page of the schematic will be discussed.

Note: Refer to http://arm.cirrus.com for the latest board schematics. Look under the download link at the top of the page.

Page 1

Block diagram and revision history.

Page 2

There are two main clock inputs to the EP9315 device. One is the 14.7456 MHz crystal oscillator and the other is the 32.768 kHz real time clock (RTC).

The 14.7456 MHz clock can be generated from a crystal circuit as shown in the schematics, or optionally from a 14.7456 MHz oscillator. If a 14.7456 MHz oscillator is used, then only the XTALI pin is driven and the drive level of the clock must be 3.3 V.

The RTC clock may be generated by the circuit shown in the schematics, or optionally an RTC oscillator. Due to the cost of RTC oscillators, the circuit shown in the schematics is used. An external oscillator is made by using an unbuffered '04 inverter. It is very important to use an unbuffered inverter in this application. Using a buffered inverter may make the circuit oscillate in the ~MHz range or not start at all. Refer to application note AN265.

The two LEDs connected to the EP9315 device are used to indicate processor health during boot and general status of the board.

The reset output, RSTON (active-low signal) is buffered by U25. There is a resistor option for the RSTON signal to be either driven by this buffer or bypassed. If the reset signal is not going to be buffered, U25 must be removed and R117 installed. By default, RSTON is buffered.

Page 3

This block shows the peripheral connections from the EP9315 processor.

Page 4

Main items on this page are the USB 2.0 Full-speed Host, USB power, UART, and Commercial IR (CIR) circuits.

The USB Host circuits are connected directly from the EP9315 to U3 and U4 and then on to the stacked USB connector, J1. U3 and U4 provide termination for the USB signals and ESD protection. Note that only two of the three USB ports are routed to USB connectors, the remaining USB port is routed to the Peripheral Expansion header. Power for the USB Host ports comes from the +5V switching regulator and is protected with poly fuses rated for 0.5 A each.

The board has all three UARTs brought out. The main UART interface, UART0, is connected to a standard male DB9 connector and provides for full modem control. The other two UART interfaces are connected to 5x2 headers. There is an option for installing zero-ohm resistors if the developer needs to provide +5V power to an external device. The pinout of the headers matches common IDC10-to-DB9 cables. Two such cables are included with the kit. All UART signals are level shifted from TTL to RS-232.

The CIR uses an enhanced GPIO (EGPIO) line to communicate to the EP9315 device.

Page 5

This is the power section for the EP9315 device. The ADC and PLL supplies are filtered. There is no reason to filter the 3.3 and the 1.8V power rails.

Page 6

The SDRAM interface is comprised of two 16-bit SDRAM devices to form a 32-bit SDRAM bus. The SDRAM is connected to /SDCS0 and is located at physical memory address 0xC000_0000. Single 32-bit SDRAM devices may be used as well.

The Flash interface is made from a single 16-bit device. It uses a "multi-cell" Flash device. The Flash device is connected to /CS6 and is located at physical memory address 0x6000_0000. The reference design uses only one Flash device. However, the EP9315 can be designed with a 32-bit Flash interface as well. The Flash device installed is a 128 Mbit, 16 Mbyte, device.

The serial EEPROM is a 4 Mbit device and may be used for serial "SPI Boot" or for storing the Ethernet MAC address. SPI Boot is not used as the default boot method but may be used by the developer if it fits his/her application. Details about SPI Boot are in the EP9315 User's Guide. The serial EEPROM is accessed only if the EGPIO7 line is configured to the proper level. The SPI™ frame signal and the EGPIO7 "enable" signal are OR'ed to create the enable for the serial EEPROM device. EGPIO7 must be low in order to communicate to the serial EEPROM. Other devices on the SPI bus must be enabled in a similar manner but not enabled simultaneously.

Note: EGPIO7 should be pulled low instead of pulled high. If SPI Boot is desired, remove R201 and pull down EGPIO7.

Page 7

The JTAG interface is connected to a 2x10 header, JP3. This connector is wired for the Multi-ICE debugger.

There are 10 signals that determine how the EP9315 will boot and operate. They are all shown on this page except for BOOT1. BOOT1 is connected to GND. BOOT1 is used for factory testing only. The other nine signals are either pulled up or down external to the EP9315 device. The boot configuration shown sets the EP9315 device to perform an Internal Async boot from a 16-bit-wide memory.

The “Serial Boot” pushbutton, S2, is used to configure the board to perform a serial boot. A serial boot is used to program the Flash device with the Cirrus Logic download utility. Instead of using jumpers, a pushbutton is used. Simply hold the pushbutton down while pressing and releasing the reset pushbutton, S3. Continue to hold S2 until the red LED turns off. Once the red LED is off, release S2.

The ISL1208 is connected to the EP9315 to provided an external, battery backed RTC clock. This device has 2 bytes of battery backed SRAM. The battery is a common lithium coin cell and easily removable if desired.

Page 8

The Micrel KS8721Bl PHY is used to provide the 10/100 Mbit Ethernet interface. The PHY is attached to the EP9315 device MII interface. The PHY also connects to RJ45 connector, J3. The Ethernet connector has integrated magnetics and status LEDs. The Micrel PHY requires external power filtering of the 2.5V supply it produces.

Page 9

The two connectors provide a daughter card interface for making custom circuits. J4 is the Memory Expansion connector and J5 is the Peripheral Expansion connector.

The entire memory bus is connected to J5. It is recommended that the bus signals be buffered if adding additional memory. However if a CPLD or FPGA is attached there is no reason to buffer. Use proper engineering practices when using the high-speed memory bus with daughter cards.

The Peripheral Expansion bus has the signals for features not implemented on the EDB9315A board and for commonly used signals.

Page 10

The IDE interface is connected from the EP9315 device to the IDE connector, JP5, through series termination resistors. These pins are 5V tolerant.

A hard disk drive (HDD) and/or CD-ROM can be connected to the board with the IDE cable provided. Simply plug the blue end of the IDE cable into the blue IDE connector, JP5. Power for the drive(s) is provided by plugging the IDE power cable (included) into the IDE power connector, JP4.

If using a notebook HDD, please use the included 3.5”-to-2.5” IDE power adapter.

Page 11

Two video interfaces are provided. The main video interface is VGA. An LCD interface is also provided however there is no LCD screen included with the development kit. The LCD interface is pin compatible with previous Cirrus Logic ARM9 development boards. A 4-wire touch screen interface is also included and is pin compatible with previous Cirrus Logic ARM9 development boards.

Page 12

An external USB 2.0 High-speed Peripheral device is provided. The USB device allows a Host to see the board as a Mass Storage device. The USB interface chip is connected to the lower 16-bits of the memory bus.

Page 13

Audio is supported by a Cirrus Logic CS4271 device. Two-channel audio out and line-level audio in is supported. The audio device communicates to the EP9315 through the I^2S interface and audio clocks are generated by the EP9315. The audio in is line level, it is not a microphone-level input. Like the serial EEPROM, the CS4271 is controlled by the SPI frame signal and EGPIO6. EGPIO6 must be low in order to communicate to the CS4271 device. As mentioned before, only one SPI™ device can be enabled at a time.

Page 14

Power and reset circuits are shown on this page. Most of the changes made to this revision of the EDB9315A board were made in this section. The most important change made is that the board is now powered from a +12V power supply instead of the former +5V supply.

The board has two connectors for input power. J10 is the standard power connector and is where the power supply provided in the kit attaches. However, a 3x1 header, J11 is also available to supply power to the board.

The 3.3V power rail is generated from a 3A, adjustable, switching regulator, U27. The 5V power rail is generated from an identical 3A switching regulator, U28. The 5V supply requires a diode, D7. The 3.3V supply does not require this diode.

The 1.8V power rail is generated from an 800mA linear regulator. Both the 3.3V and 1.8V power rails are are monitored by U22 and it will issue a reset if either supply falls below the threshold voltage.

The reset pushbutton can connect directly to the voltage monitor reset input or to a supplementary reset-detect circuit. Refer to AN258 for more information. This circuit is implemented by U24 and some passive devices. In general, this circuit is not required with EP9315 Rev E2 devices and may be removed if desired. It is installed by default. If removed, R109 needs to be installed if the use of the reset pushbutton is desired.

5. Software

5.1 Overview

The software programmed into the Flash on the EDB9315A development board is WinCE® 5.0. Linux® 2.6.8.1, from Cirrus Logic, running Qt/Opie is also available for the EDB9315A board

The WinCE 5.0 image programmed into Flash by the factory is not available from Cirrus Logic directly. This image can not be provided to users due to distribution and royalty reasons. If the developer decides to overwrite the factory WinCE 5.0 Flash image with Linux or some other software, and then later desires to put the WinCE 5.0 image back into Flash, they must obtain the WinCE 5.0 BSP from their Cirrus Logic FAE and build the image themselves using the trial version of Platform Builder™ or with a version of Platform Builder they have purchased. Only WinCE 5.0 supports the EDB9315A board. Cirrus Logic technical support for WinCE 4.2 is not available.

Cirrus Logic provides complete source for its Linux 2.6 offering. The Cirrus Logic release images for the EDB9315A are also provided for those who do not want to build the toolchain and environment or want a quick way to load Linux onto the board. If, however, you wish to implement functionality other than that provided in the release package images, you must download the gcc toolchain from the Cirrus Logic User's Development Forum, under the download link at the top of the page http://arm.cirrus.com/files/tools . The other method is to download the buildroot package from the same location and let it download and build all the appropriate packages and toolchain.

Note: Linux development should be done on a Linux PC, not under Windows. Cirrus Logic uses Debian as the default build environment. Red Hat® and other versions of Linux may be used as well, but Cirrus Logic Linux 2.6. development is done under Debian.

5.2 Download Utility

The download utility provides the user with a tool for programming the flash memory on the EDB9315A Development Board with a binary image. Two versions of the download executable are provided: one supporting a PC running Windows/DOS, and one supporting a PC running Linux. The following procedure will allow in-circuit programming of the flash memory via the EP9315 processor:

1. Connect null-modem serial cable to the DB9 connector on the board and to the PC.
2. Run the download utility; make sure all terminal windows are "Disconnected" Assuming the download utility is located in same directory as the binary image…
    a. For Windows: download binary_image_filename.bin
    b. For Linux: download binary_image_filename.bin
3. "Waiting for board to wake up…" message is displayed on the PC.
4. Press and hold down pushbutton S2 "SERIAL BOOT"
5. Press and then release pushbutton S3 "/POR"
6. Wait for the red LED to go off then release pushbutton S2.
7. Messages will be displayed regarding erasing, then programming the flash.
8. "Successfully programmed binary_image_filename.bin" message displayed upon programming completion.
9. Press pushbutton S3 to reboot the board with the new code image.

6. Developer’s User Forum

Many references have been made to the Cirrus Logic Developers User's Forum in this document.

The Cirrus Logic Developers User's Forum is a company-sponsored site and moderated by Cirrus Logic employees. However, it is not the technical help line for the Cirrus Logic ARM® product line. It is intended to be a place where developers can share ideas and ask questions from others.

Developers should become familiar with the Developer's User Forum and the files provided under the download link. Both software and hardware files are provided for Cirrus Logic offerings. Refer to Chapter 7 for useful information related to the Cirrus Logic ARM products.

7. Other Useful Information

Web Sites

- Cirrus Logic main web site: www.cirrus.com
- Developer's Web Site: arm.cirrus.com
- Registration Web Site: www.cirrus.com/boardreg

Processor Information

The following information is located on the www.cirrus.com web site.

- EP9315 Datasheet
- EP9315 User's Guide
- EP9315 Errata

Application Notes

The following information is located on the www.cirrus.com web site.

- AN273, *"EP93xx Silicon Rev E Design Guidelines"*
- AN265, *"EP93xx RTC Oscillator Circuit"*
- AN258, *"EP93xx Power-up and Reset Lockup Workaround"*

Board Information

The following information is located on the arm.cirrus.com web site.

- EDB9315A Technical Reference Manual
- Schematics
- BOM
- Artwork and PCB stackup

Code Information

The following information is located on the arm.cirrus.com web site.

- Linux 2.6
- Board utilities
- Tools

Contact a Cirrus Logic FAE for information regarding the following.

- WinCE 5.0 BSP

The documents listed above are updated periodically and may be more up to date than the information in this document. Check with the web sites for the latest updates.

Appendix A. Schematics

The schematics for the EDB9315A Development Board are located on the Cirrus Logic Developer's Forum website (arm.cirrus.com). The schematics are provided in Adobe's portable document format (PDF) and PADS™ format. OrCAD™ versions of the schematics are not available.

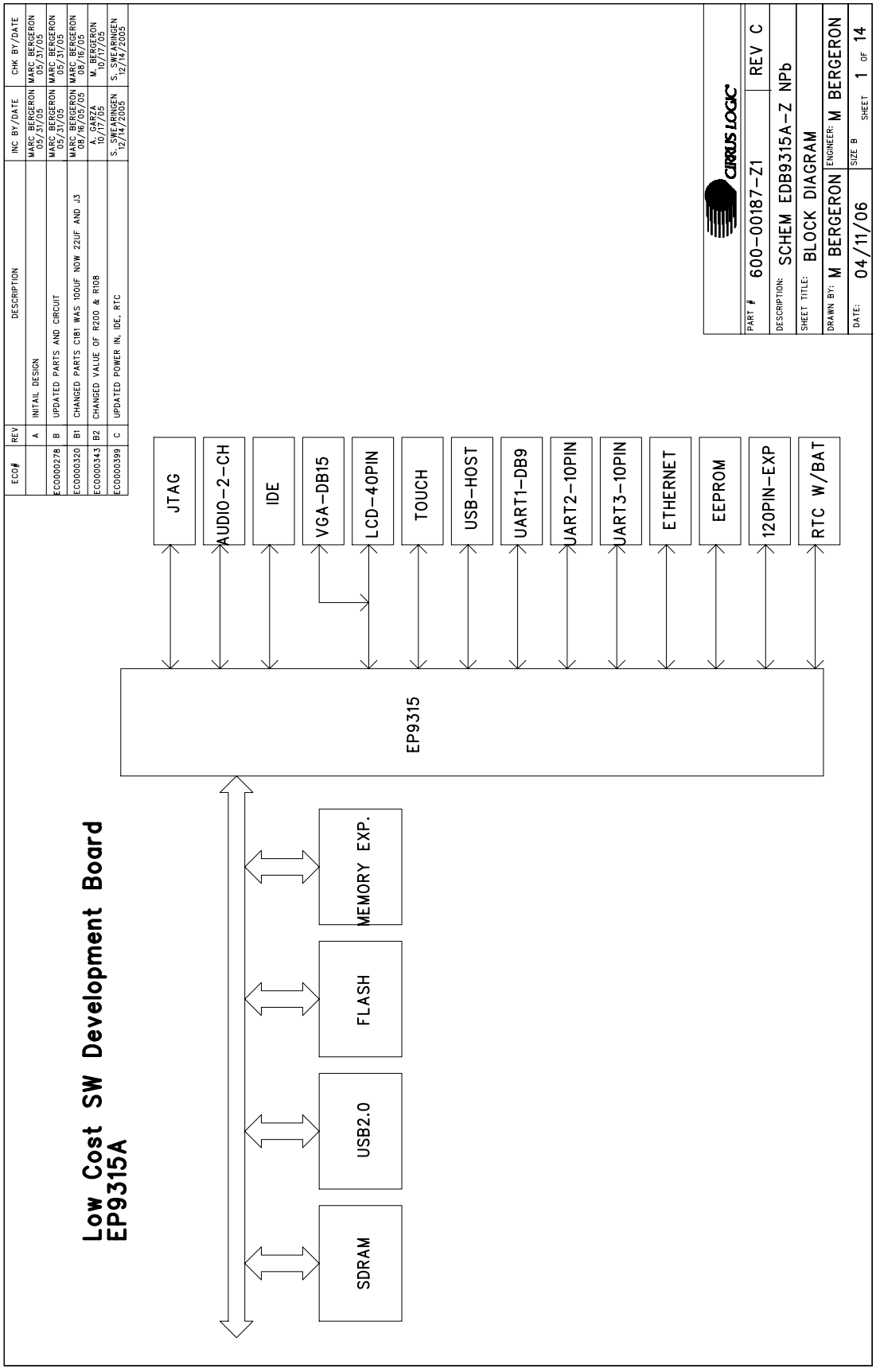

Figure 4. Schematic Page 1 - Block Diagram

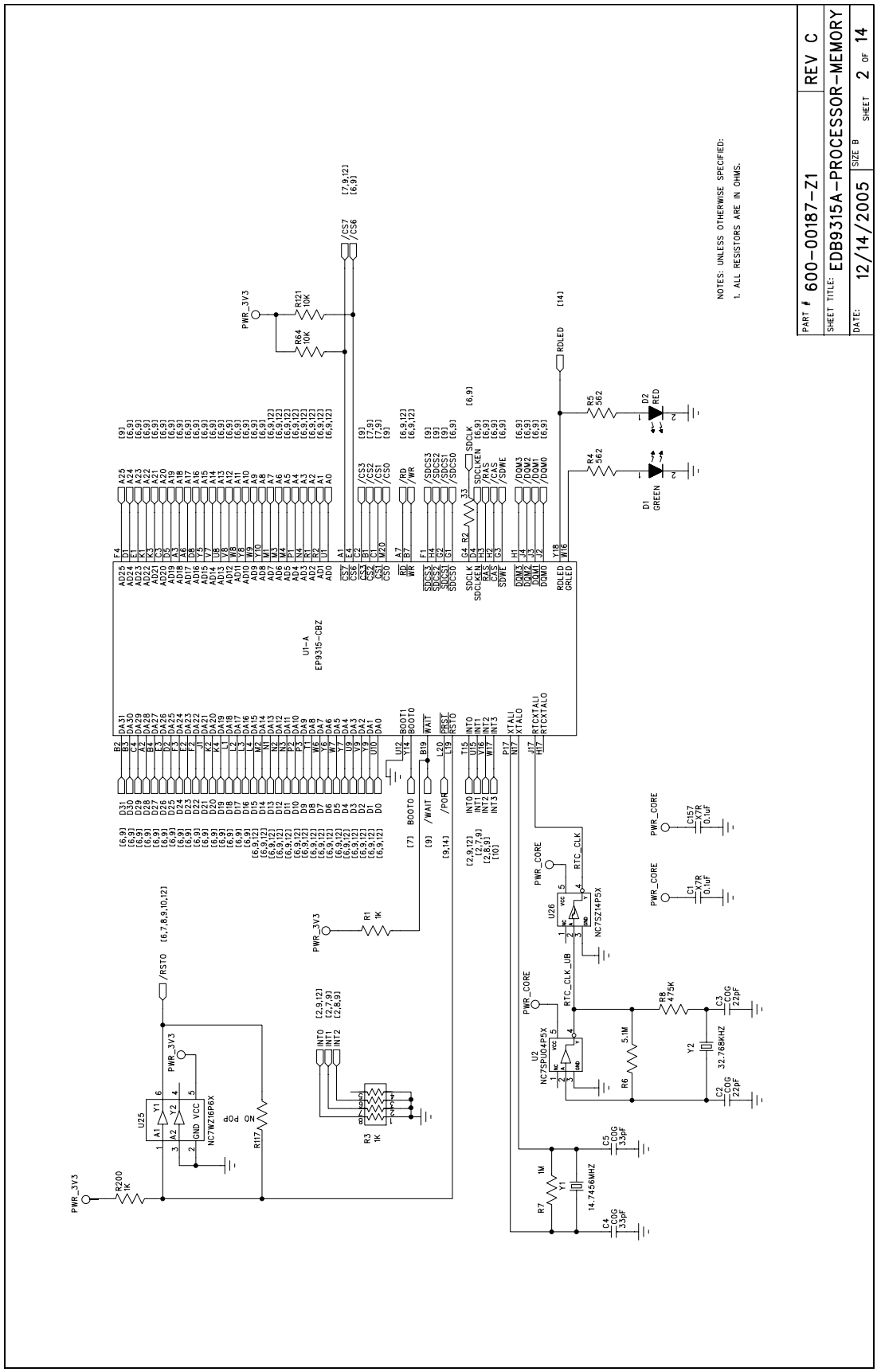

Figure 5. Schematic Page 2 - Processor & Memory

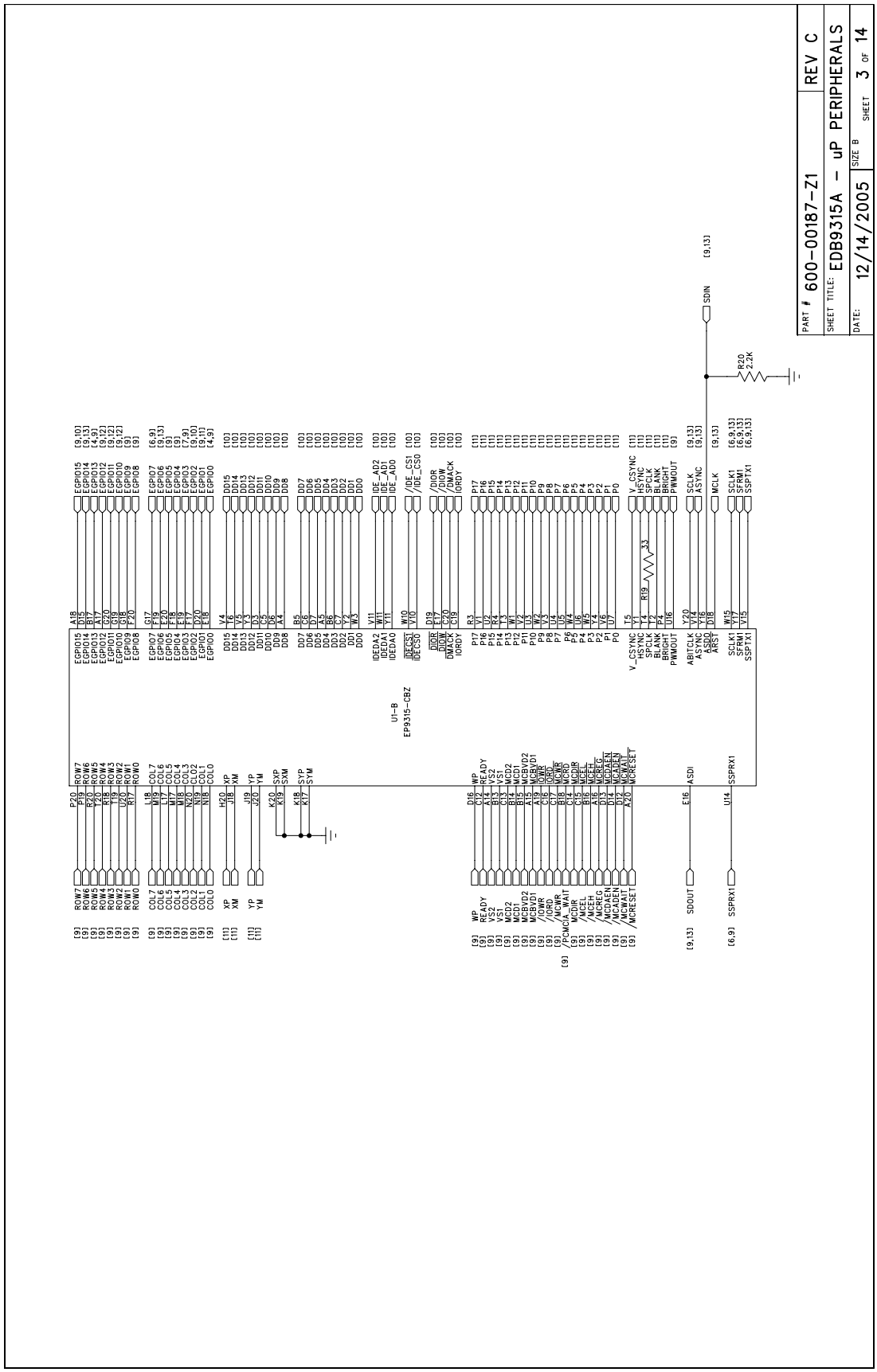

Figure 6. Schematic Page 3 - Peripherals

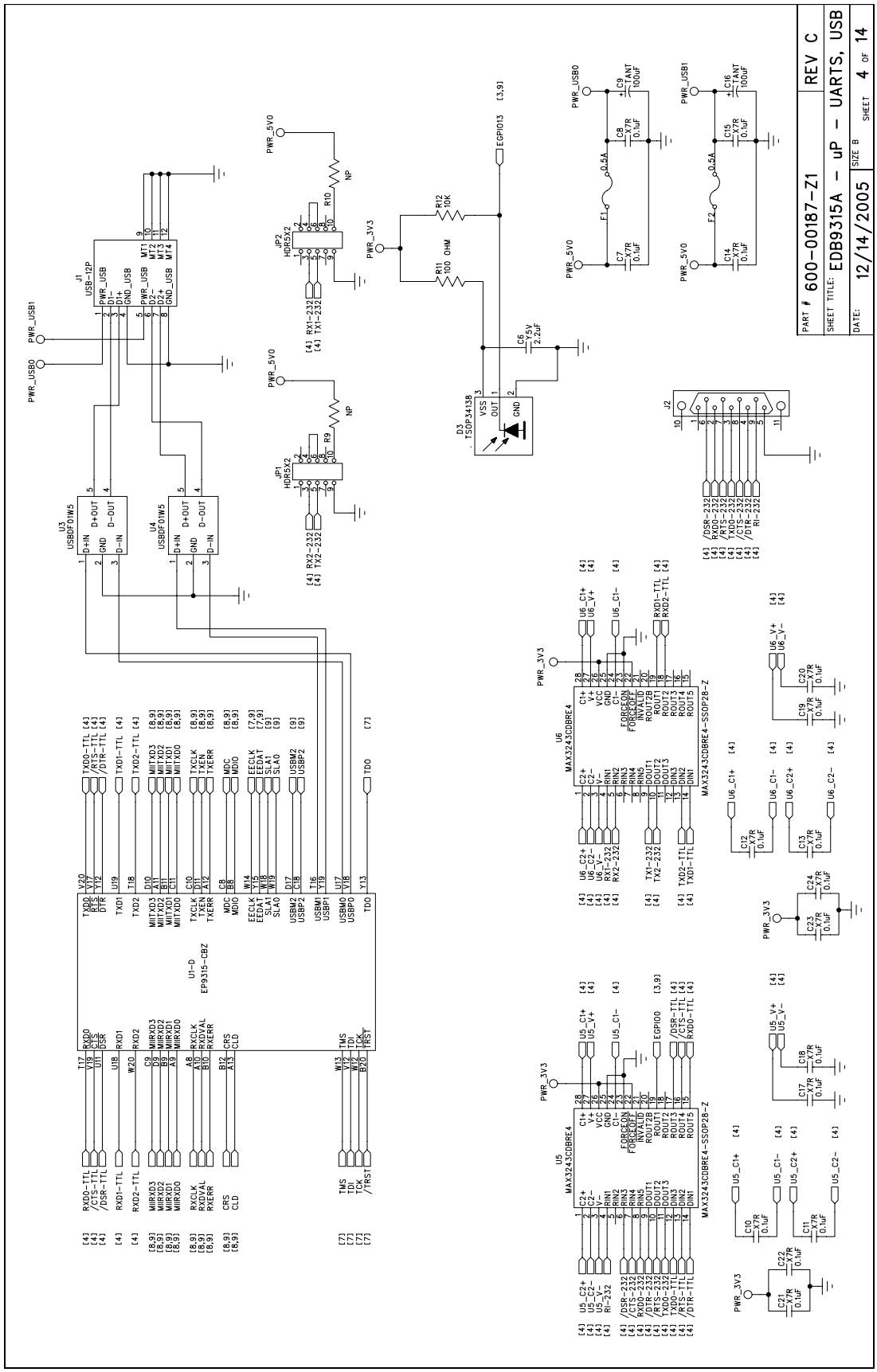

Figure 7. Schematic Page 4 - UARTs & USB

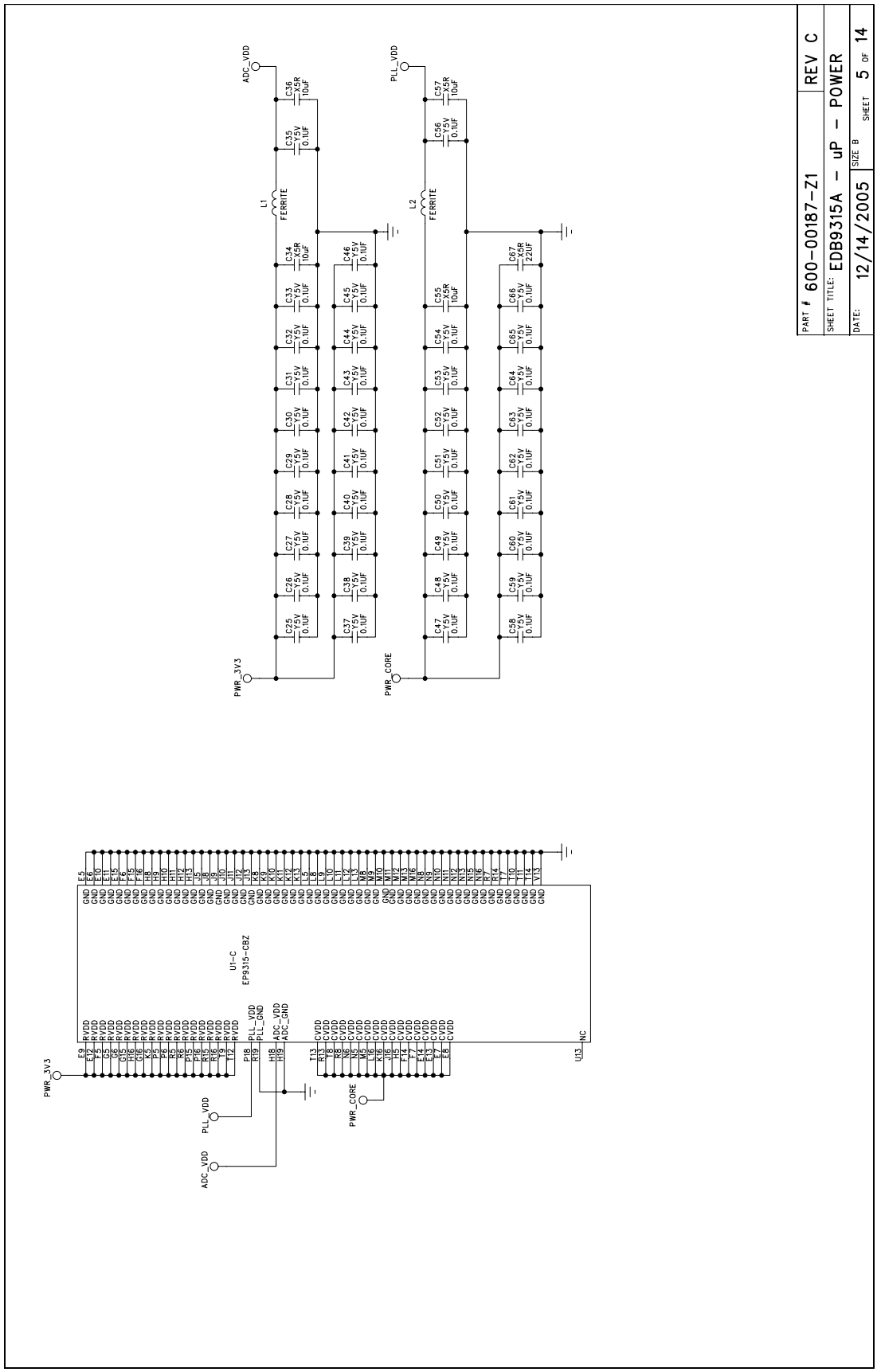

Figure 8. Schematic Page 5 - µP Power

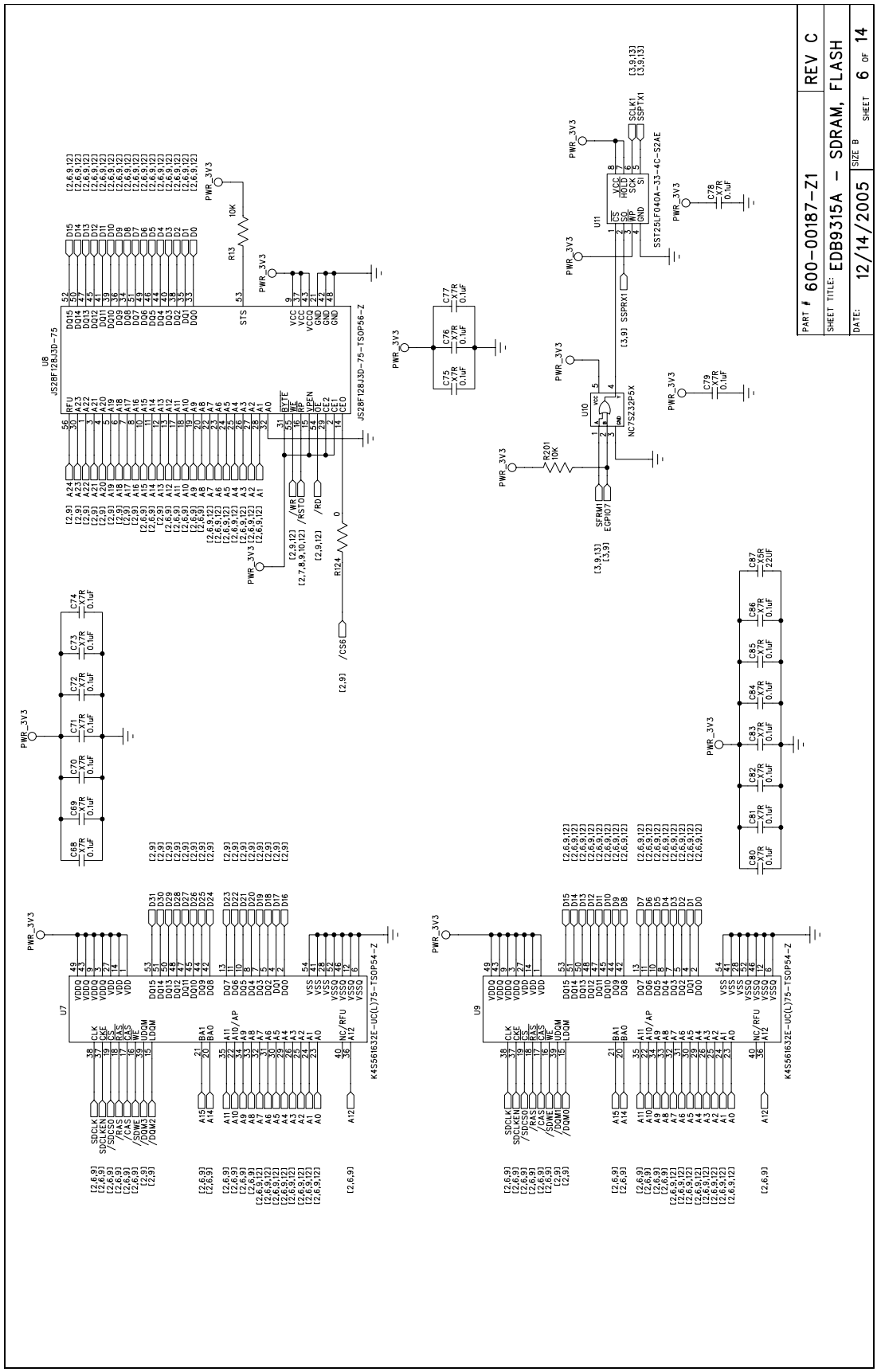

Figure 9. Schematic Page 6 - SDRAM & Flash

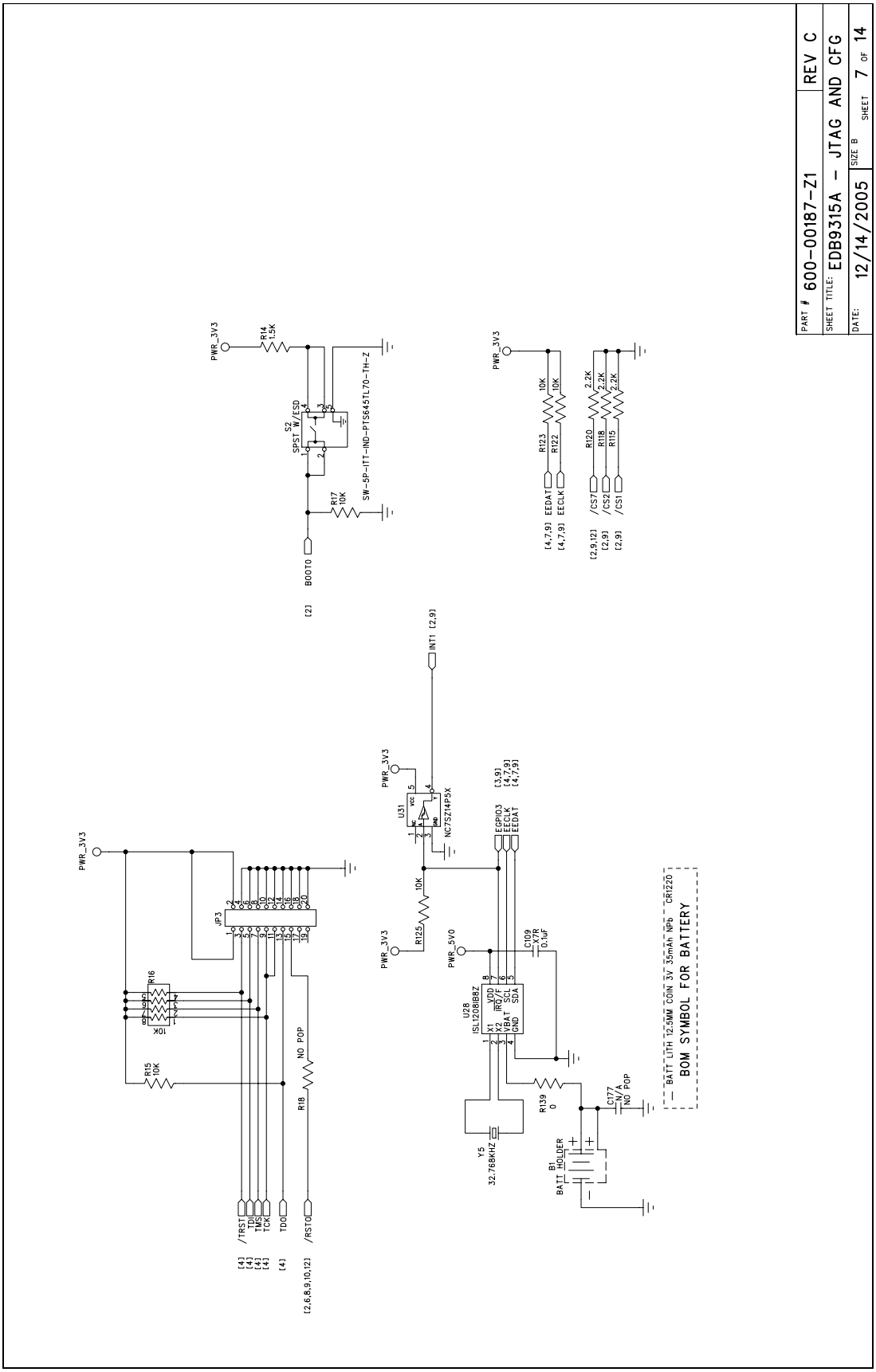

Figure 10. Schematic Page 7 - JTAG & CFG