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Mobile LPDDR2 SDRAM

EDB4432BBPA, EDB8132B4PM, EDBM432B3PB, EDBM432B3PF, EDBA232B2PB, EDBA232B2PF

Features

- Ultra-low-voltage core and I/O power supplies
- Frequency range
  - 533 MHz (data rate: 1066 Mb/s/pin)
- 4*n* prefetch DDR architecture
- 8 internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on each CK_t/CK_c edge
- Bidirectional/differential data strobe per byte of data (DQS_t/DQS_c)
- Programmable READ and WRITE latencies (RL/WL)
- Burst length: 4, 8 and 16
- Per-bank refresh for concurrent operation
- Auto temperature-compensated self refresh (ATCSR) by built-in temperature sensor
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock-stop capability
- Lead-free (RoHS-compliant) and halogen-free packaging

Options

- $V_{DD1}/V_{DD2}/V_{DDQ}$: 1.8V/1.2V/1.2V
- Array configuration
  - 128 Meg x 32 (SDP)
  - 256 Meg x 32 (DDP)
  - 384 Meg x 32 (3DP)
  - 512 Meg x 32 (QDP)
- Packaging
  - 12mm x 12mm, 168-ball PoP FBGA package
- Operating temperature range
  - From –30°C to +85°C

Table 1: Configuration Addressing

Architecture		128 Meg x 32	256 Meg x 32	384 Meg x 32	512 Meg x 32
Density per package		4Gb	8Gb	12Gb	16Gb
Die per package		1	2	3	4
Ranks (CS_n) per channel		1	2	2	2
Die per rank	CS0_n	1	1	2	2
	CS1_n	0	1	1	2
Configuration per rank (CS_n)	CS0_n	16 Meg x 32 x 8 banks	16 Meg x 32 x 8 banks	32 Meg x 16 x 8 banks x 2	32 Meg x 16 x 8 banks x 2
	CS1_n	N/A	16 Meg x 32 x 8 banks	16 Meg x 32 x 8 banks	32 Meg x 16 x 8 banks x 2
Row addressing		16K A[13:0]	16K A[13:0]	16K A[13:0]	16K A[13:0]
Column addressing/CS_n	CS0_n	1K A[9:0]	1K A[9:0]	2K A[10:0]	2K A[10:0]
	CS1_n	N/A	1K A[9:0]	1K A[9:0]	2K A[10:0]

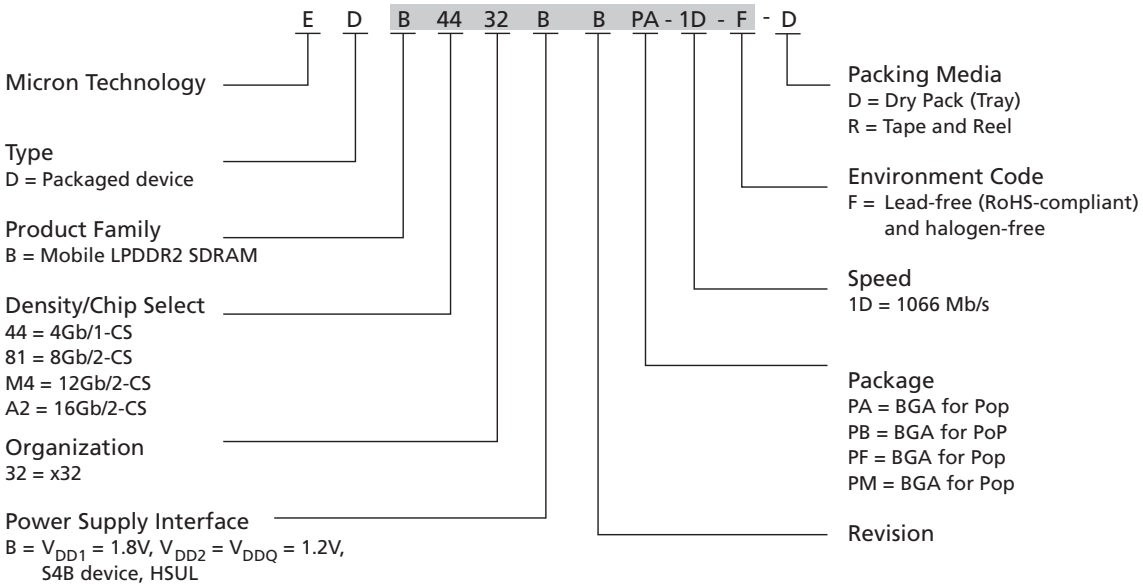
Table 2: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency	READ Latency
1D	533	1066	4	8

Table 3: Part Number Description

Part Number	Total Density	Configuration	Ranks	Channels	Package Size	Ball Pitch
EDB4432BBPA-1D-F-R, EDB4432BBPA-1D-F-D	4Gb	128 Meg x 32	1	1	12mm x 12mm (0.80mm MAX height)	0.50mm
EDB8132B4PM-1D-F-R, EDB8132B4PM-1D-F-D	8Gb	256 Meg x 32	2	1	12mm x 12mm (0.82mm MAX height)	0.50mm
EDBM432B3PB-1D-F-R, EDBM432B3PB-1D-F-D	12Gb	384 Meg x 32	2	1	12mm x 12mm (0.90mm MAX height)	0.50mm
EDBM432B3PF-1D-F-R, EDBM432B3PF-1D-F-D	12Gb	384 Meg x 32	2	1	12mm x 12mm (0.92mm MAX height)	0.50mm
EDBA232B2PB-1D-F-R, EDBA232B2PB-1D-F-D	16Gb	512 Meg x 32	2	1	12mm x 12mm (1.00mm MAX height)	0.50mm
EDBA232B2PF-1D-F-R, EDBA232B2PF-1D-F-D	16Gb	512 Meg x 32	2	1	12mm x 12mm (1.02mm MAX height)	0.50mm

Figure 1: Marketing Part Number Chart



Note: 1. The characters highlighted in gray indicate the physical part marking found on the device.

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Ball Assignments

Figure 2: 168-Ball Single-Channel FBGA – 1 x 4Gb Die

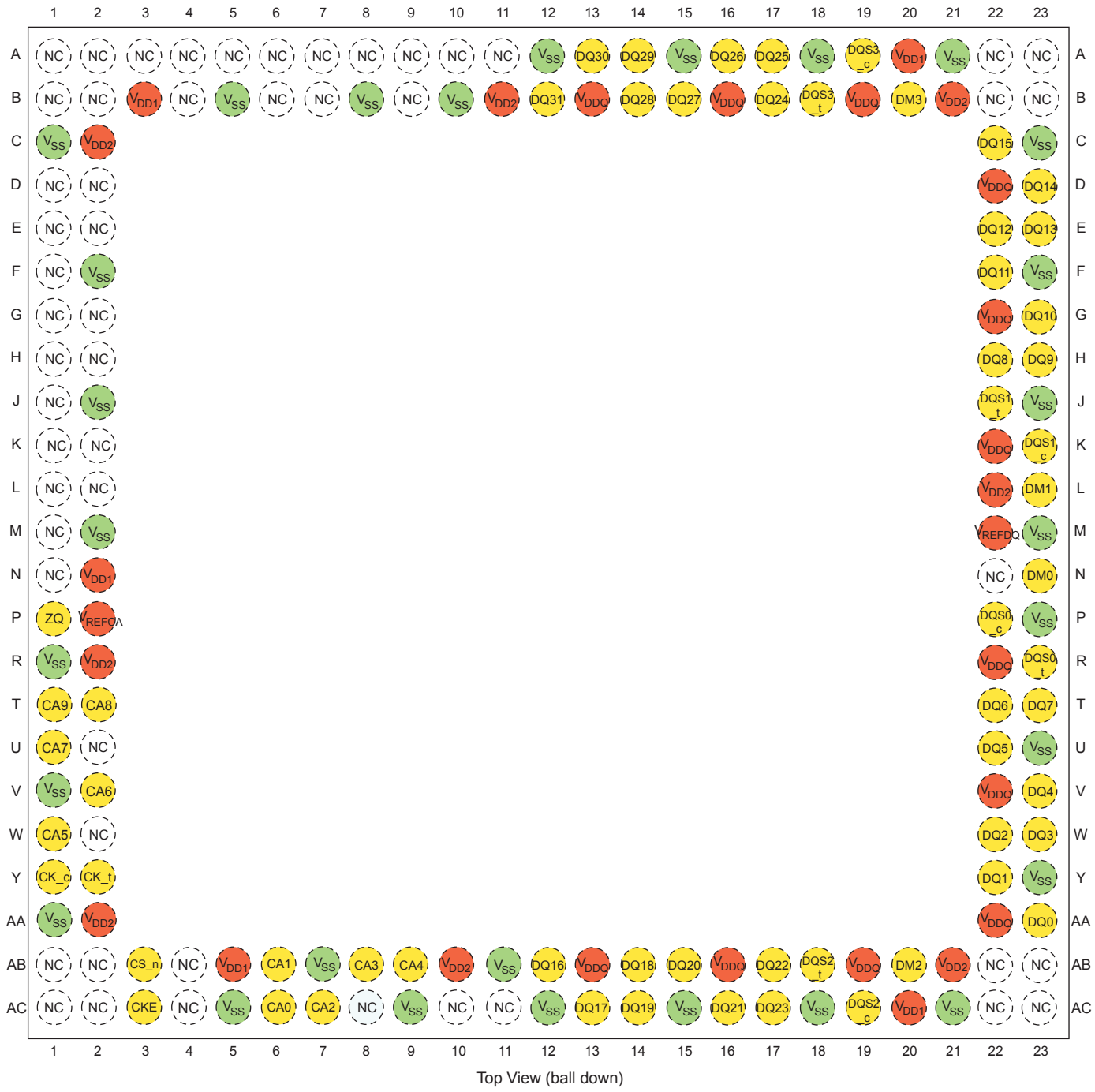
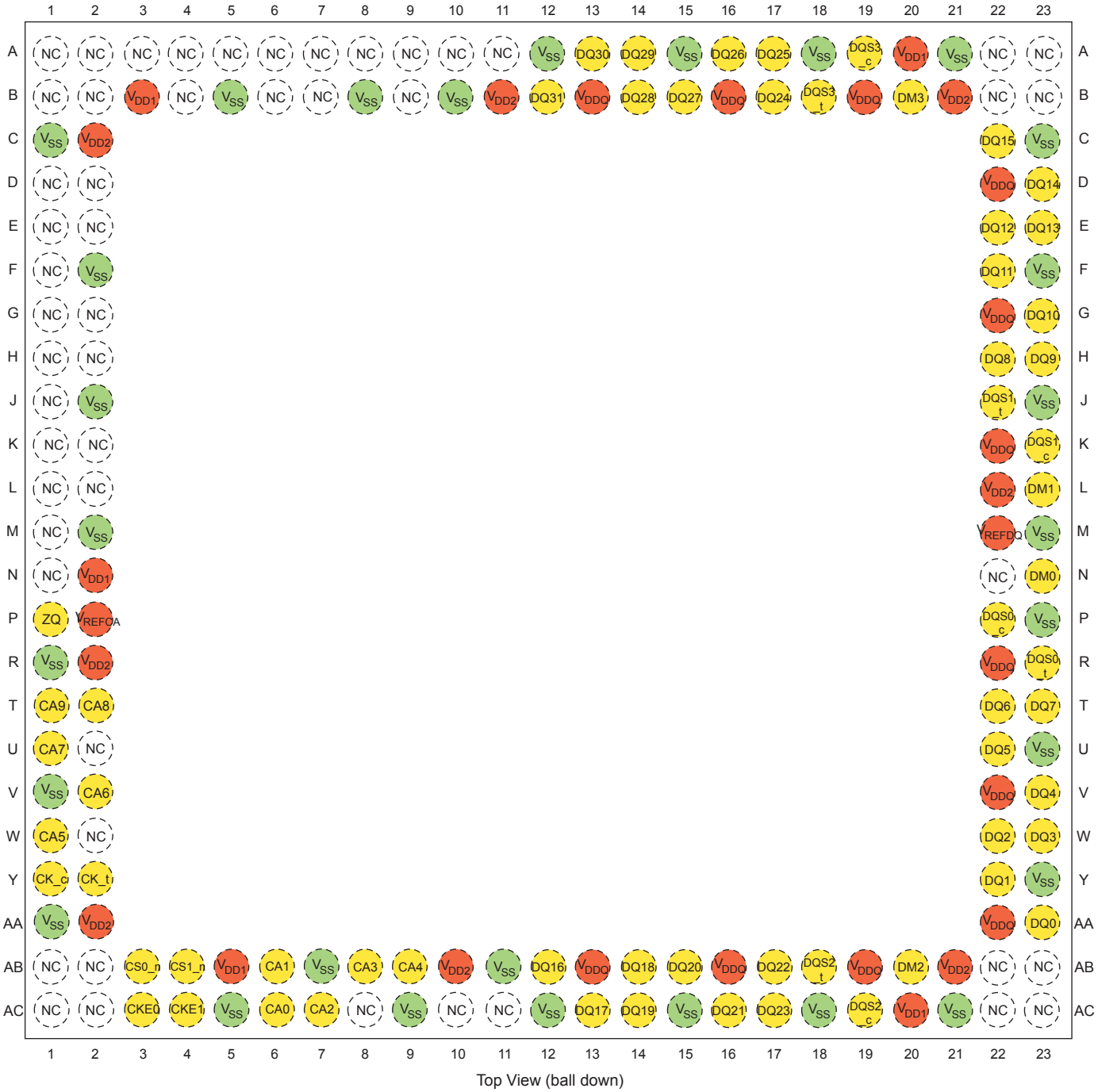
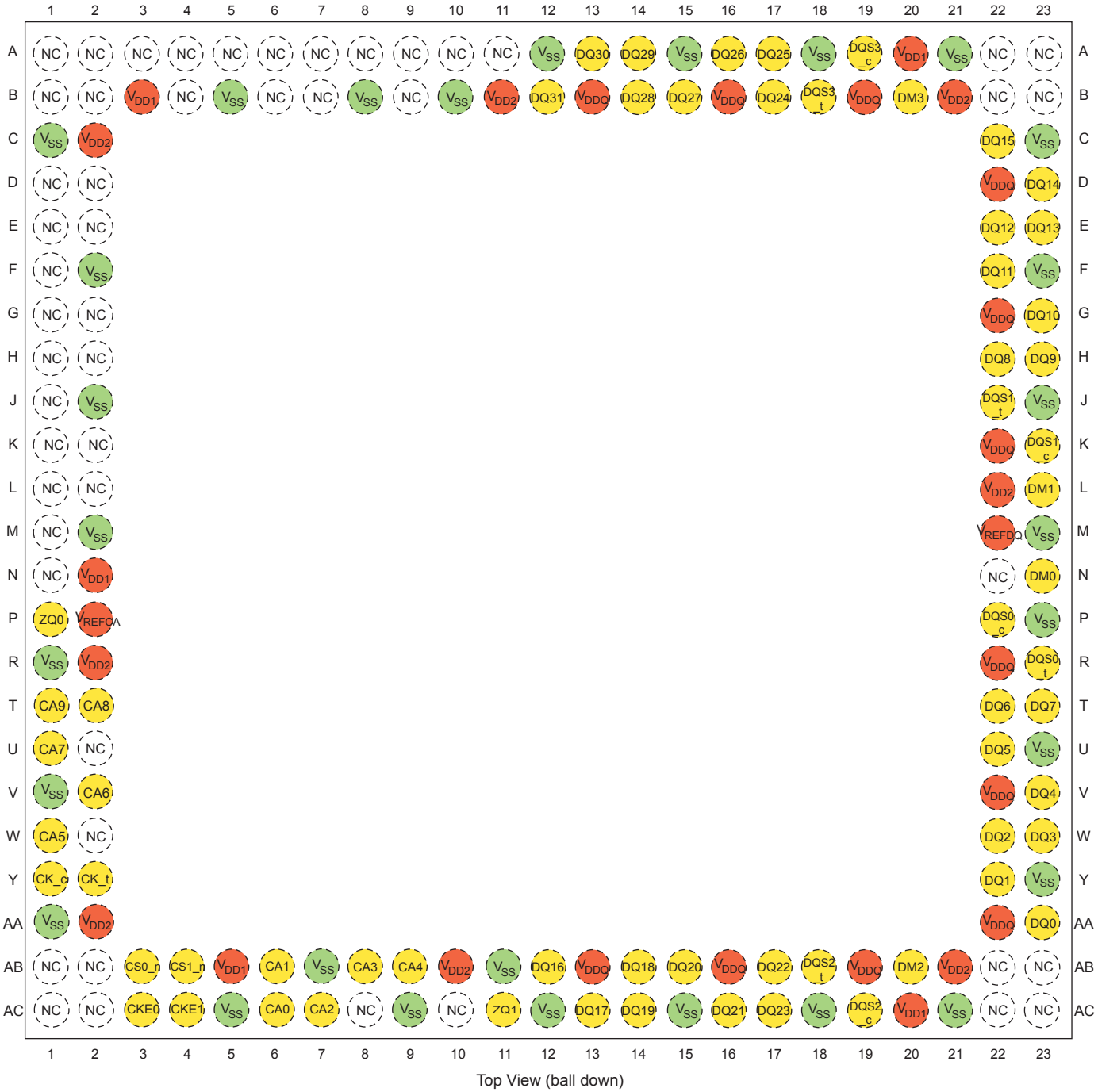


Figure 3: 168-Ball Single-Channel FBGA – 2 x 4Gb Die



Top View (ball down)

Figure 4: 168-Ball Single-Channel FBGA – 3 or 4 x 4Gb Die



Top View (ball down)

Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See Ball Assignments for information specific to this device.

Table 4: Ball/Pad Descriptions

Symbol	Type	Description
CA[9:0]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
CK_t, CK_c	Input	**Clock:** Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE[1:0]	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK.
CS[1:0]_n	Input	**Chip select:** Considered part of the command code and is sampled on the rising edge of CK.
DM[3:0]	Input	**Input data mask:** Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively.
DQ[31:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[3:0]_t, DQS[3:0]_c	I/O	**Data strobe:** Bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively.
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{SS}	Supply	**Common ground.**
V_{REFCA}, V_{REFDQ}	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers.
ZQ[1:0]	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NU	–	**Not usable:** Do not connect.
NC	–	**No connect:** Not internally connected.
(NC)	–	**No connect:** Balls indicated as (NC) are no connects; however, they could be connected together internally.

Package Block Diagrams

Figure 5: Single-Die, Single-Channel Package Block Diagram

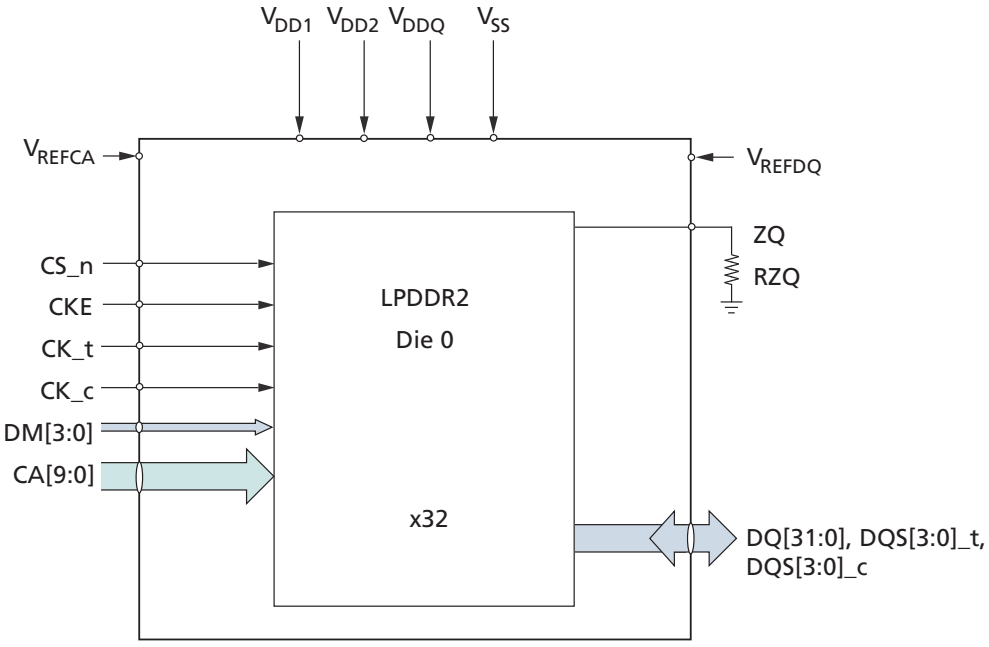


Figure 6: Dual-Die, Single-Channel Package Block Diagram

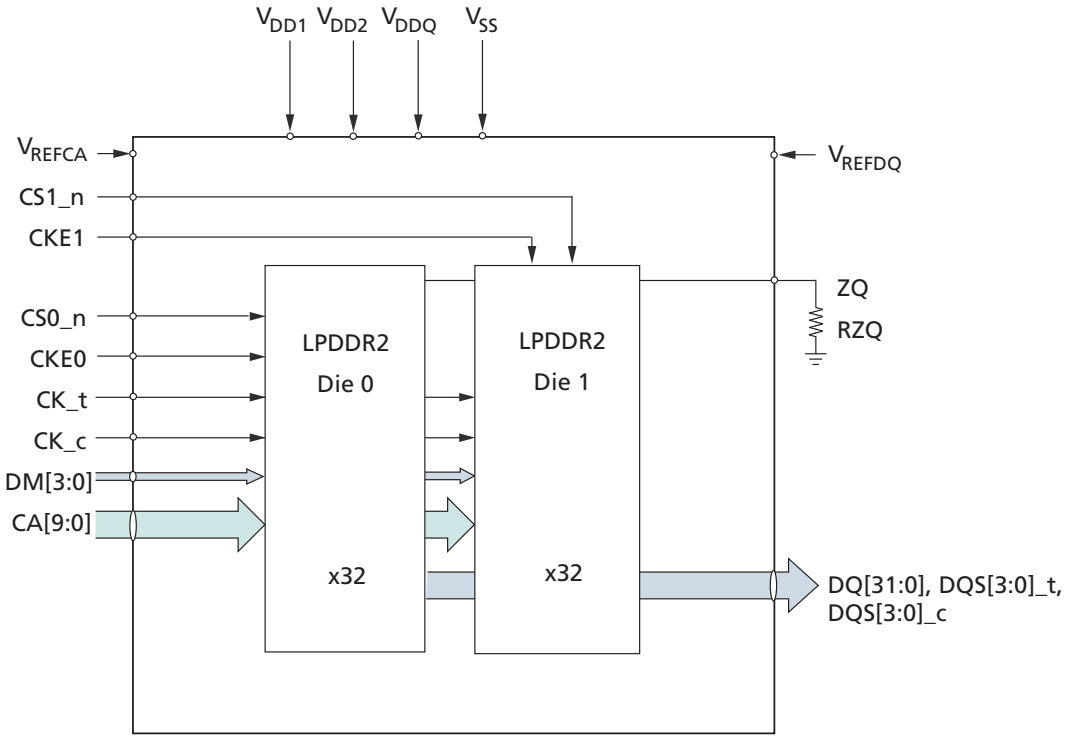


Figure 7: 3-Die, Single-Channel Package Block Diagram

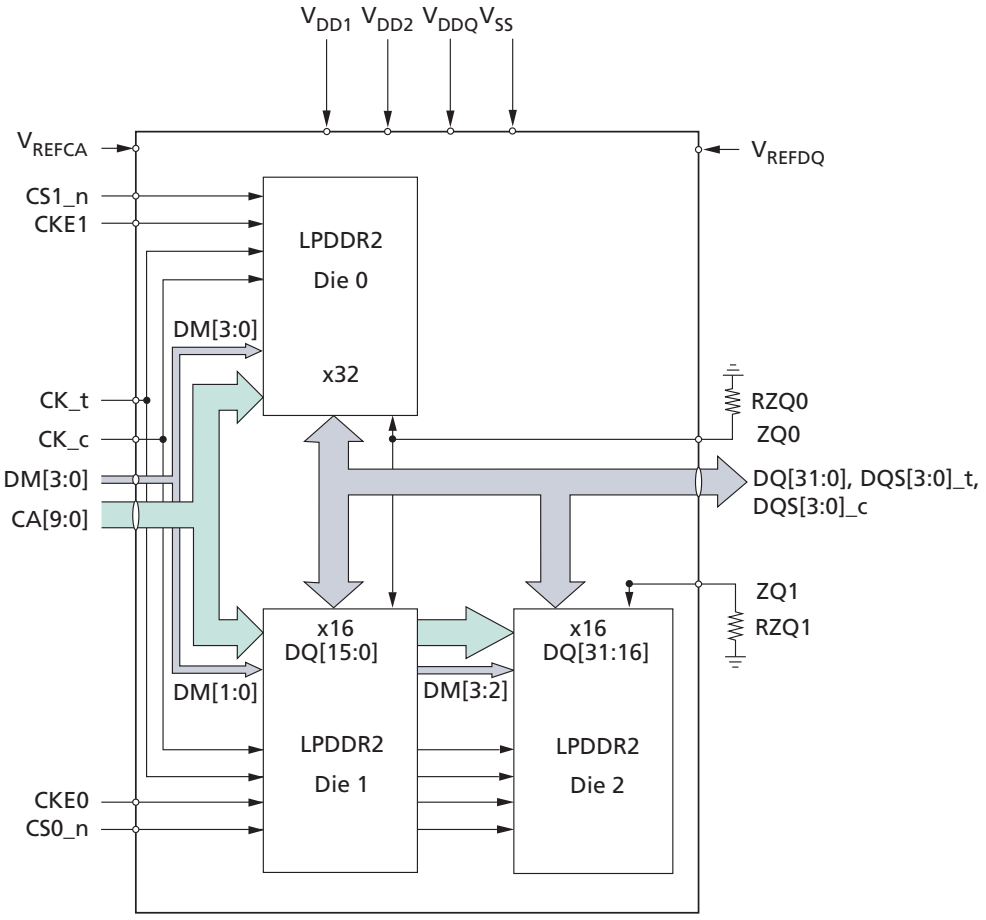
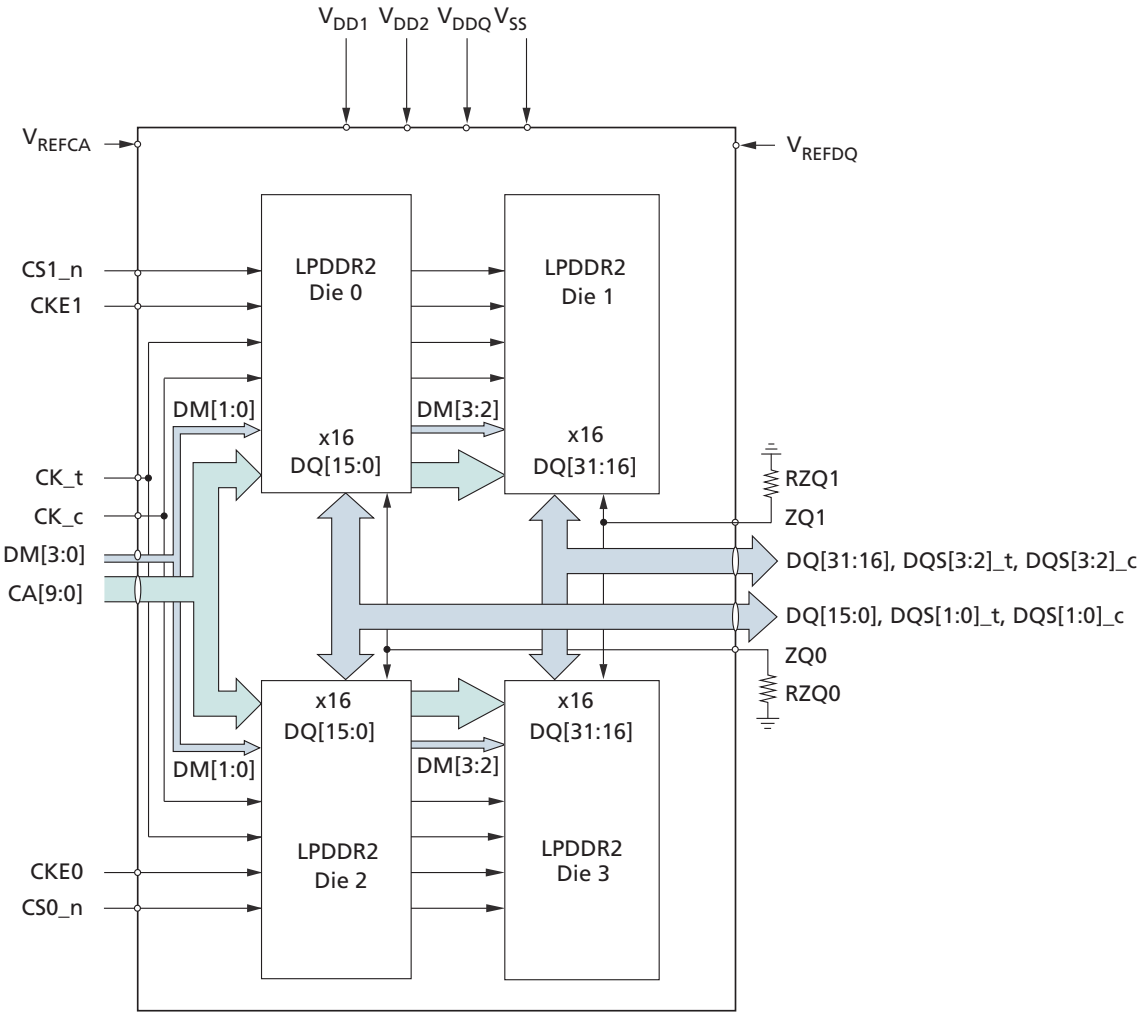
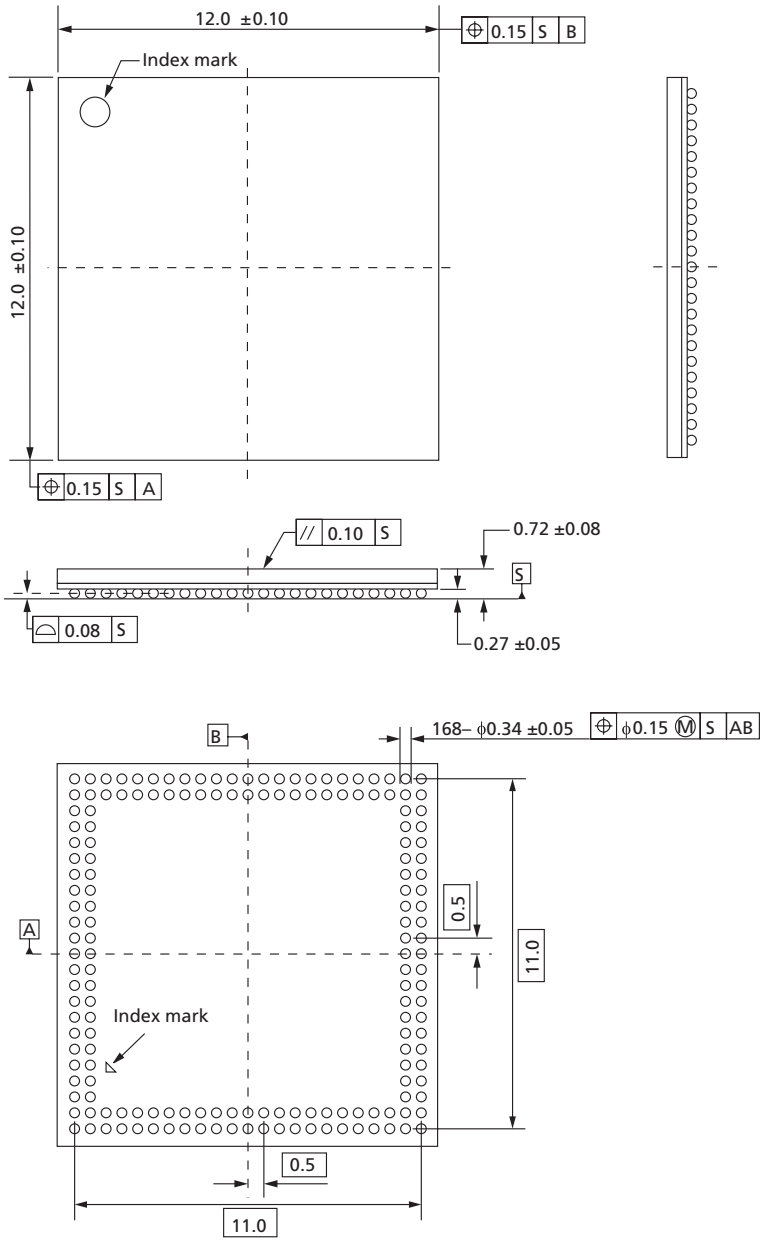


Figure 8: Quad-Die, Single-Channel Package Block Diagram



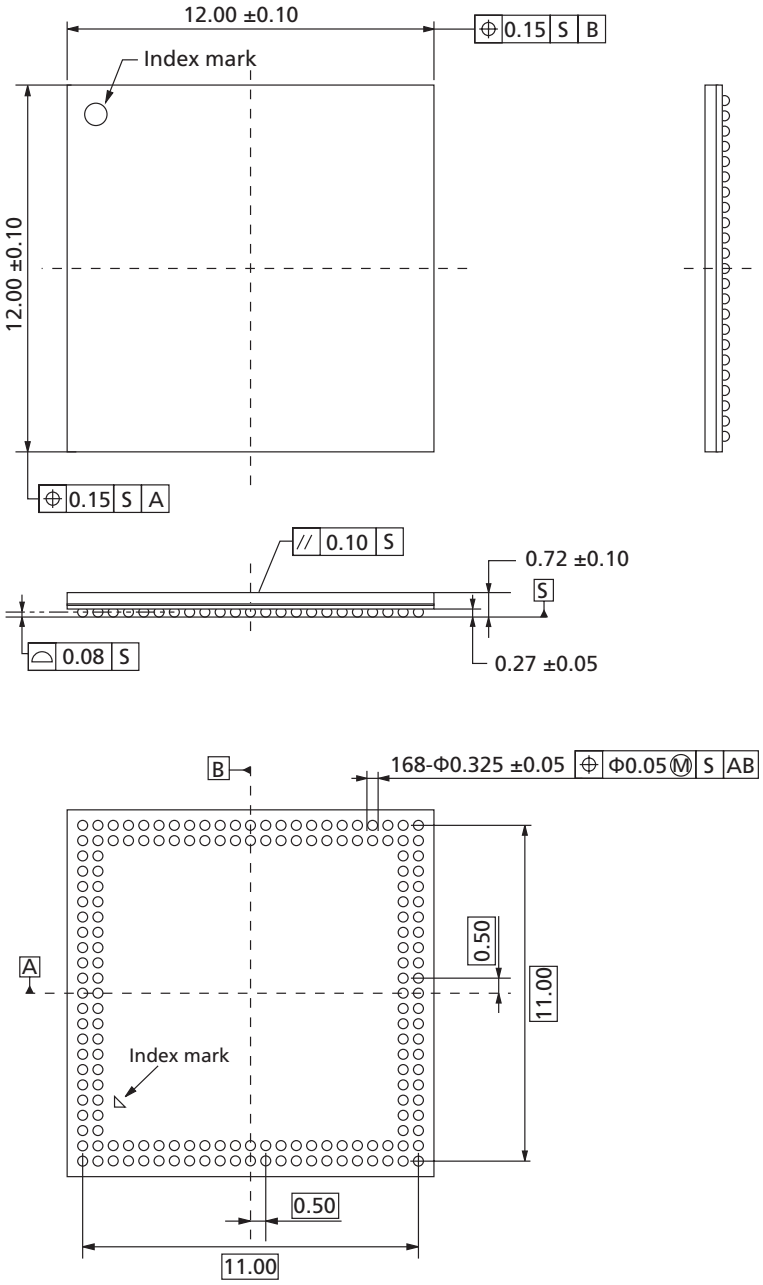
Package Dimensions

Figure 9: 168-Ball FBGA (12mm x 12mm) – EDB4432BBPA



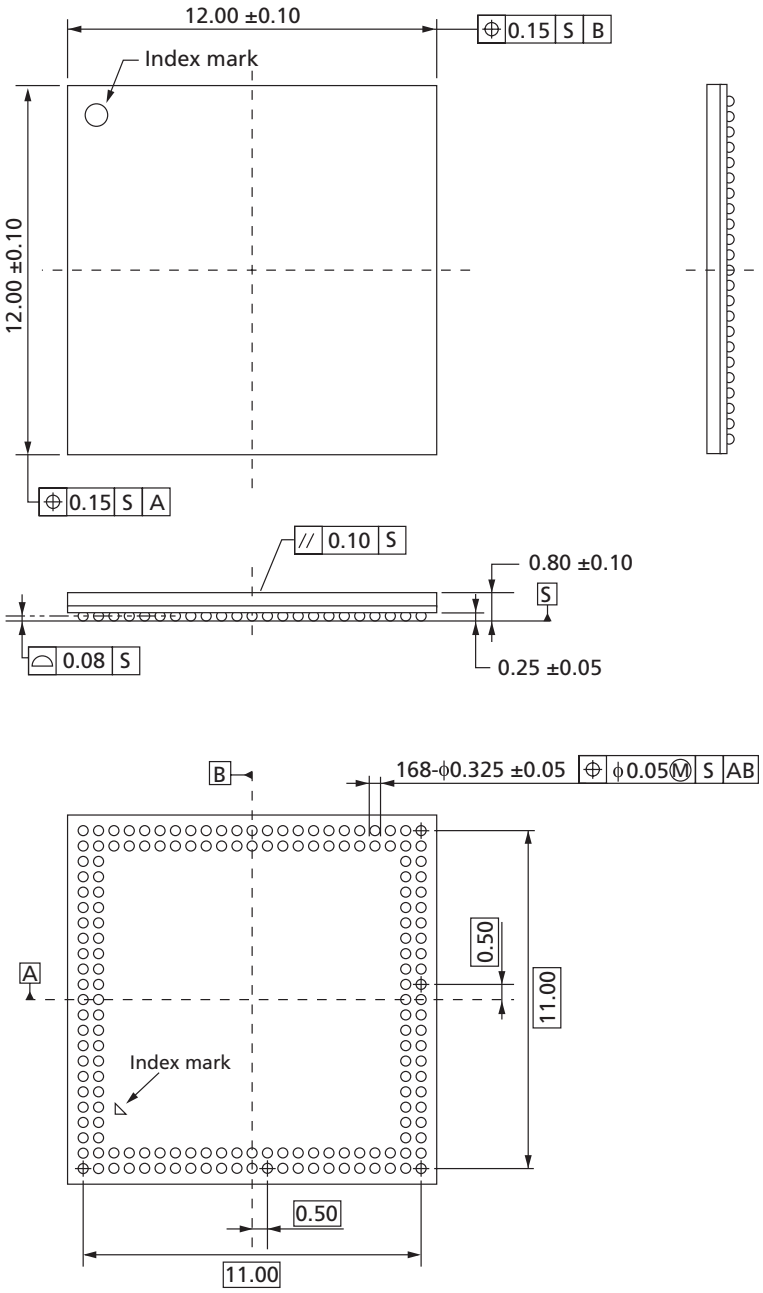
Notes:
1. Package drawing: ECA-TS2-0445-01.
2. All dimensions are in millimeters.

Figure 10: 168-Ball FBGA (12mm x 12mm) – EDB8132B4PM



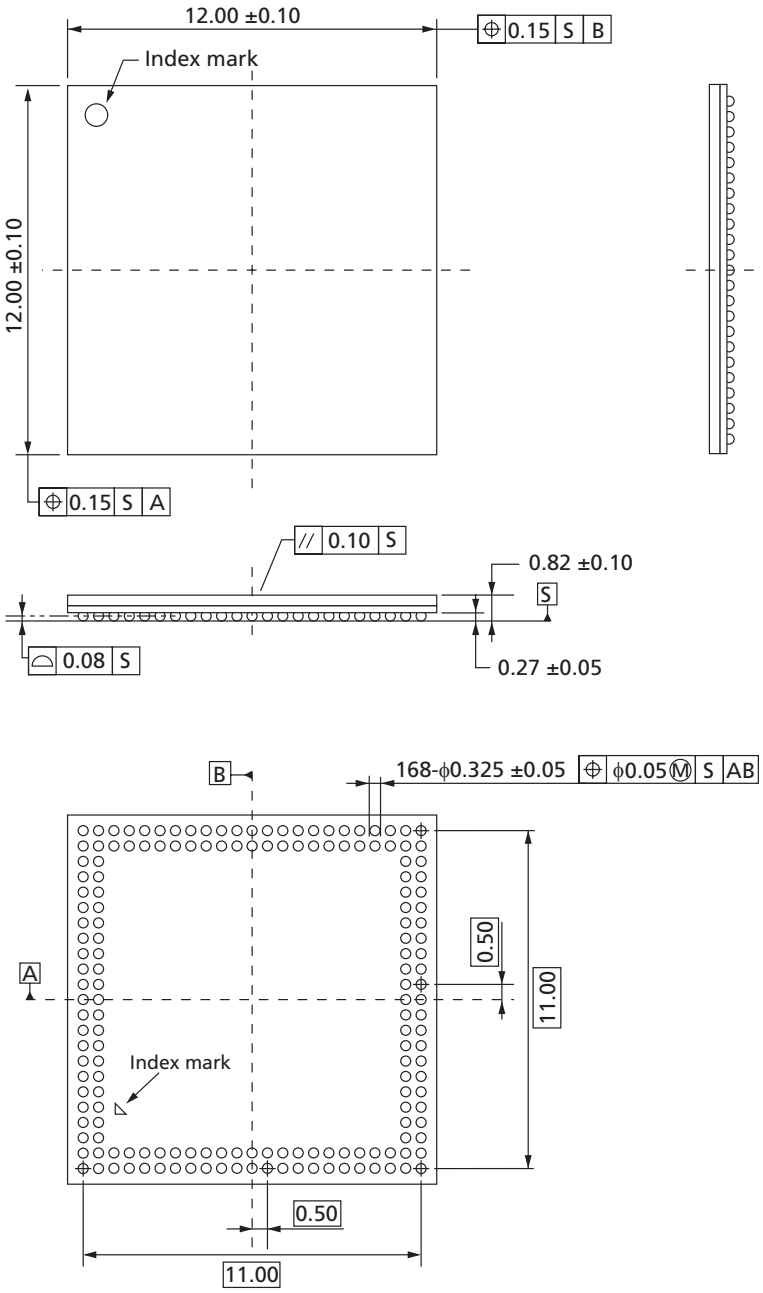
Notes:
1. Package drawing: ECA-TS2-0531-01.
2. All dimensions are in millimeters.

Figure 11: 168-Ball FBGA (12mm x 12mm) – EDBM432B3PB



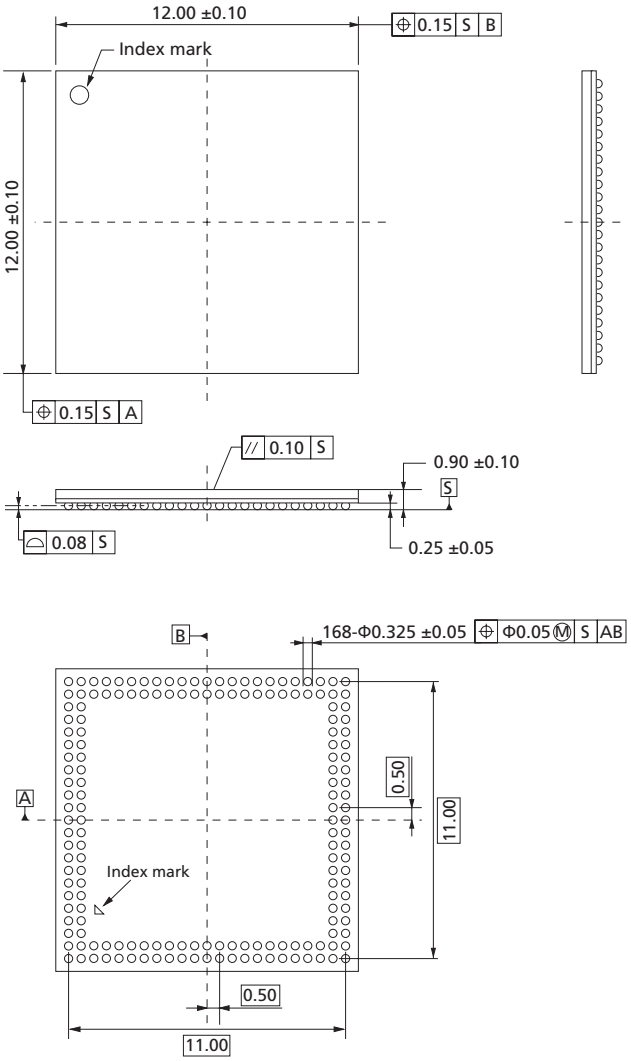
Notes:
1. Package drawing: ECA-TS2-0517-02.
2. All dimensions are in millimeters.

Figure 12: 168-Ball FBGA (12mm x 12mm) – EDBM432B3PF



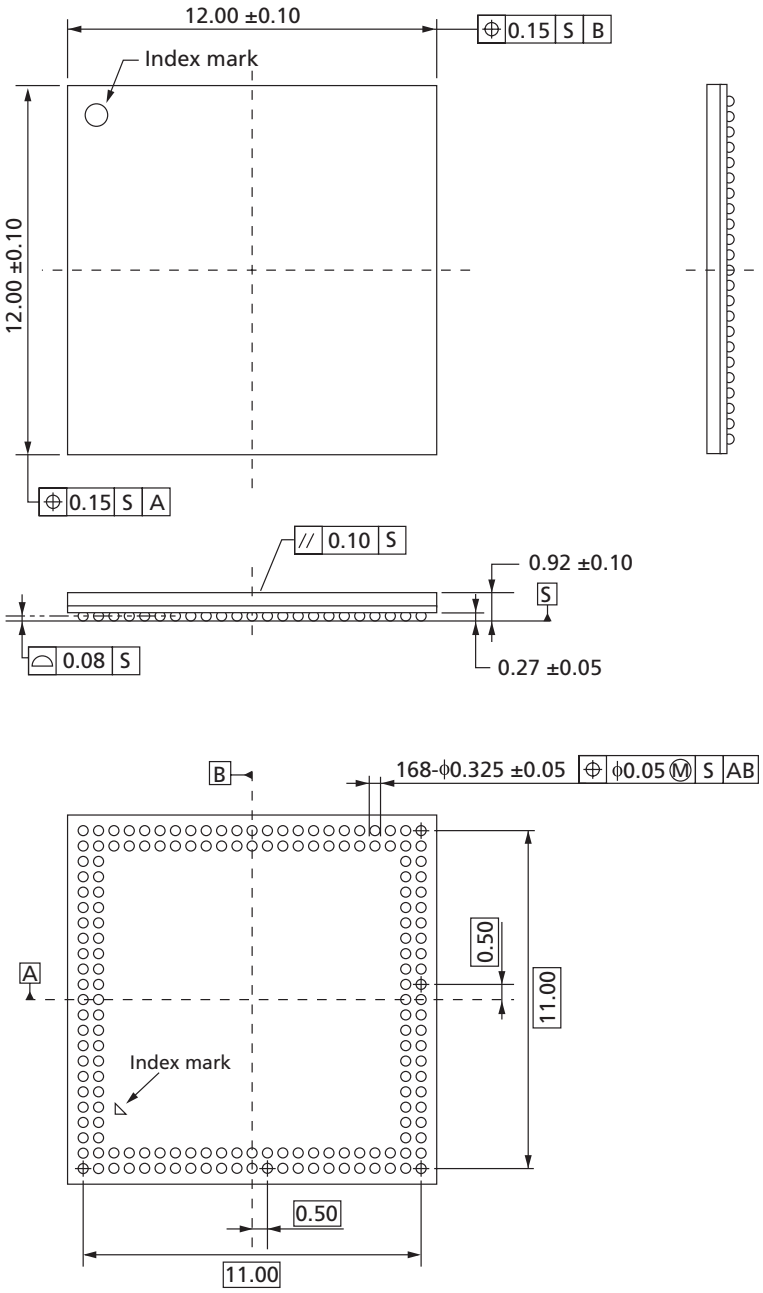
Notes:
1. Package drawing: ECA-TS2-0530-01.
2. All dimensions are in millimeters.

Figure 13: 168-Ball FBGA (12mm x 12mm) – EDBA232B2PB



Notes:
1. Package drawing: ECA-TS2-0516-02.
2. All dimensions are in millimeters.

Figure 14: 168-Ball FBGA (12mm x 12mm) – EDBA232B2PF



Notes:
1. Package drawing: ECA-TS2-0532-01.
2. All dimensions are in millimeters.

MR5–MR8 Readout

Table 5: Mode Register Contents

Part Number	Total Density	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR5									
EDB4432BBPA	4Gb	Manufacturer ID = 0000 0011b:							
EDB8132B4PM	8Gb								
EDBM432B3PB, EDBM432B3PF	12Gb								
EDBA232B2PB, EDBA232B2PF	16Gb								
MR6									
EDB4432BBPA	4Gb	Revision ID1 = 0000 0001b: Revision B							
EDB8132B4PM	8Gb								
EDBM432B3PB, EDBM432B3PF	12Gb								
EDBA232B2PB, EDBA232B2PF	16Gb								
MR7									
EDB4432BBPA	4Gb	Revision ID2 = (RFU)							
EDB8132B4PM	8Gb								
EDBM432B3PB, EDBM432B3PF	12Gb								
EDBA232B2PB, EDBA232B2PF	16Gb								

MR8		I/O Width/CS_n		Density	Type
		CS0_n	CS1_n		
EDB4432BBPA	4Gb	00b: x32	N/A	0110b: 4Gb	00b: S4
EDB8132B4PM	8Gb	00b: x32	00b: x32	0110b: 4Gb	00b: S4
EDBM432B3PB, EDBM432B3PF	12Gb	01b: x16	00b: x32	0110b: 4Gb	00b: S4
EDBA232B2PB, EDBA232B2PF	16Gb	01b: x16	01b: x16	0110b: 4Gb	00b: S4

Note: 1. The contents of MR5-MR8 will reflect information specific to each in these packages.