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Embedded LPDDR3 SDRAM

EDF8164A3PK, EDFA164A2PK

Features

- Ultra-low-voltage core and I/O power supplies
- Frequency range
  - 800/933 MHz (data rate: 1600/1866 Mb/s/pin)
- 8*n* prefetch DDR architecture
- 8 internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on each CK_t/CK_c edge
- Bidirectional/differential data strobe per byte of data (DQS_t/DQS_c)
- Programmable READ and WRITE latencies (RL/WL)
- Burst length: 8
- Per-bank refresh for concurrent operation
- Auto temperature-compensated self refresh (ATCSR) by built-in temperature sensor
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock-stop capability
- Lead-free (RoHS-compliant) and halogen-free packaging

Options

- $V_{DD1}/V_{DD2}/V_{DDCA}/V_{DDQ}$: 1.8V/1.2V/1.2V/1.2V
- Array configuration
  - 128 Meg x 64 (DDP)
  - 256 Meg x 64 (QDP)
- Packaging
  - 12mm x 12mm, 216-ball PoP FBGA package
- Operating temperature range
  - From –30°C to +85°C

Table 1: Configuration Addressing

Architecture	128 Meg x 64	256 Meg x 64
Density per package	8Gb	16Gb
Die per package	2	4
Ranks (CS_n) per channel	1	2
Die per channel	1	2
Configuration	16 Meg x 32 x 8 banks x 2 channel	16 Meg x 32 x 8 banks x 2 rank x 2 channel
Row addressing	16K A[13:0]	16K A[13:0]
Column addressing (same for each die)	1K A[9:0]	1K A[9:0]

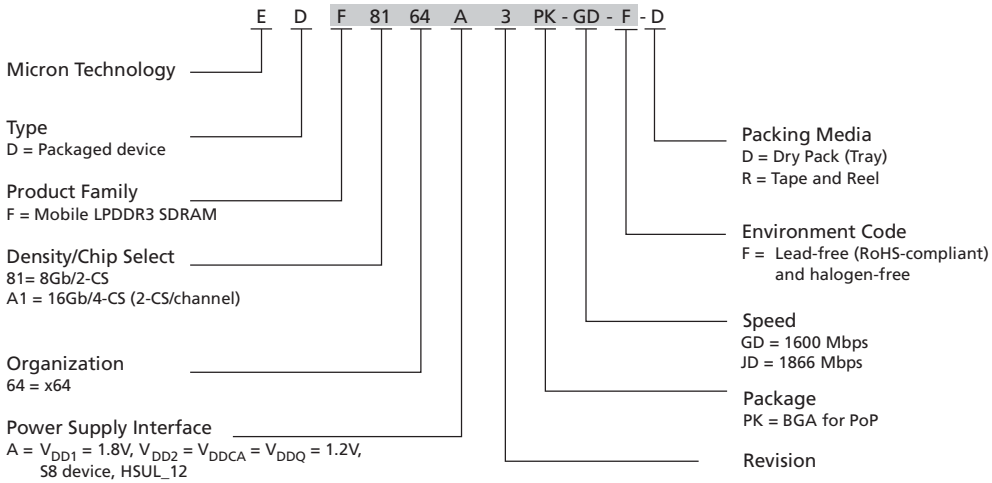
Table 2: Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency (Set A/B)	READ Latency
GD	800	1600	6/9	12
JD	933	1866	8/11	14

Table 3: Part Number Description

Part Number	Total Density	Configuration	Ranks	Channels	Package Size	Ball Pitch
EDF8164A3PK-GD-F-D EDF8164A3PK-GD-F-R EDF8164A3PK-JD-F-D EDF8164A3PK-JD-F-R	8Gb	128 Meg x 64	1	2	12mm x 12mm (0.70mm MAX height)	0.40mm
EDFA164A2PK-GD-F-D EDFA164A2PK-GD-F-R EDFA164A2PK-JD-F-D EDFA164A2PK-JD-F-R	16Gb	256 Meg x 64	2	2	12mm x 12mm (0.80mm MAX height)	0.40mm

Figure 1: Marketing Part Number Chart



Note: 1. The characters highlighted in gray indicate the physical part marking found on the device.

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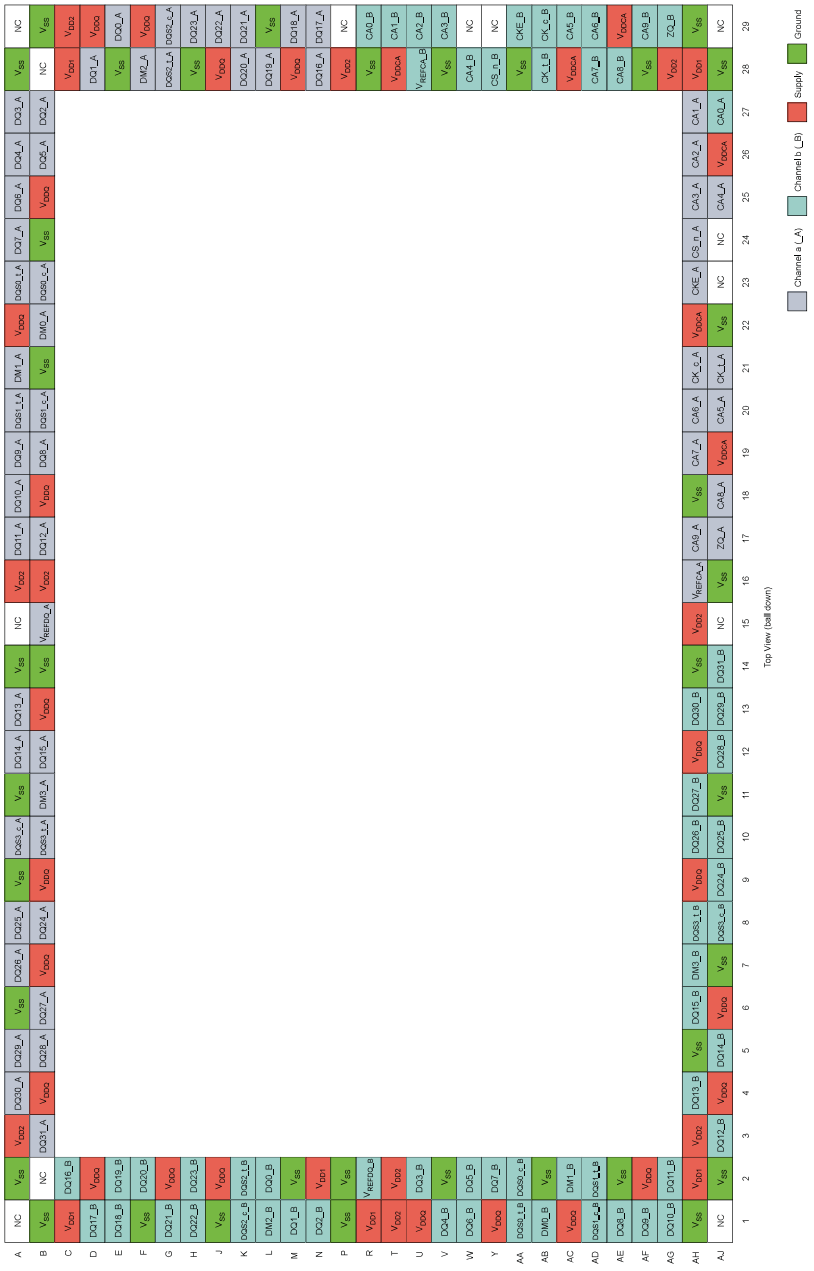
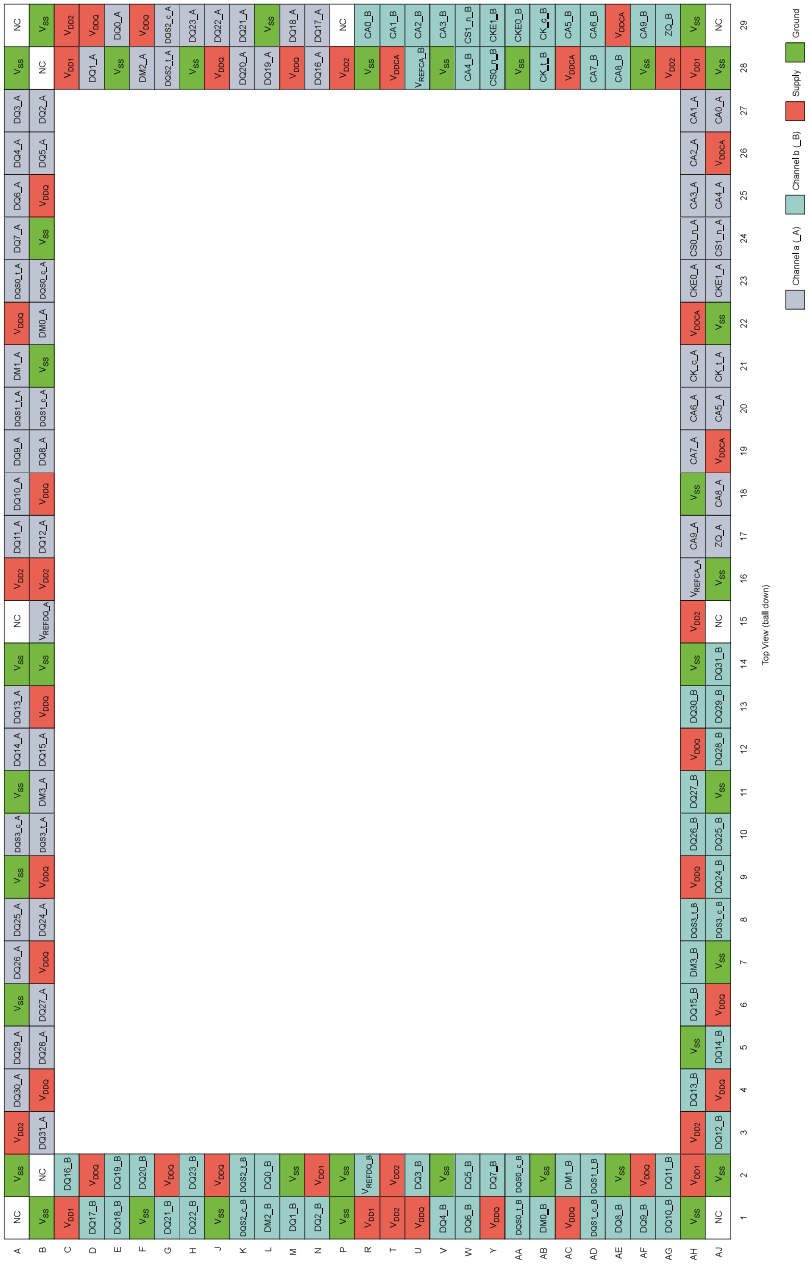
Ball Assignments

Figure 2: 216-Ball FBGA – 2 x 4Gb Die



Ball Assignments

Figure 3: 216-Ball FBGA – 4 x 4Gb Die



Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See ball assignments for information specific to this device.

Table 4: Ball/Pad Descriptions

Symbol	Type	Description
CA[9:0]_A, CA[9:0]_B	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table. A separate CA[9:0] is provided for each channel (A and B).
CK_t_B, CK_t_A CK_c_B, CK_c_A	Input	**Clock:** Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock. A separate CK_t/CK_c is provided for each channel (A and B).
CKE[1:0]_A, CKE[1:0]_B	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK. A separate CKE is provided for each channel (A and B).
CS[1:0]_n_A, CS[1:0]_n_B	Input	**Chip select:** Considered part of the command code and is sampled on the rising edge of CK. A separate CS_n is provided for each channel (A and B).
DM[3:0]_B, DM[3:0]_A	Input	**Input data mask:** Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively. A separate DM[3:0] is provided for each channel (A and B).
ODT_B, ODT_A	Input	**On-die termination:** Enables and disables termination on the DRAM DQ bus according to the specified mode register settings. For packages that do not support ODT, the ODT signal may be grounded internally. A separate ODT provided for each channel (A and B).
DQ[31:0]_B, DQ[31:0]_A	I/O	**Data input/output:** Bidirectional data bus. A separate DQ[11:0] is provided for each channel (A and B).
DQS[3:0]_t_B, DQS[3:0]_t_A, DQS[3:0]_c_B, DQS[3:0]_c_A	I/O	**Data strobe:** Bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively. A separate DQS[3:0]_t and DQS[3:0]_c is provided for each channel (A and B).
V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
V_{DDCA}	Supply	**Command/address power supply:** Command/address power supply.
V_{SSCA}	Supply	**Command/address ground:** Isolated on the die for improved noise immunity.
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{SS}	Supply	**Common ground.**
V_{REFCA}_B, V_{REFCA}_A V_{REFDQ}_B, V_{REFDQ}_A	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers. A separate V_{REFCA} and V_{REFDQ} provided for each channel (A and B).
ZQ_B, ZQ_A	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}. A separate ZQ is provided for each channel (A and B).

Table 4: Ball/Pad Descriptions (Continued)

Symbol	Type	Description
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.
(NC)	–	**No connect:** Balls indicated as (NC) are no connects; however, they could be connected together internally.

Package Block Diagrams

Figure 4: Dual-Die, Dual-Channel Package Block Diagram

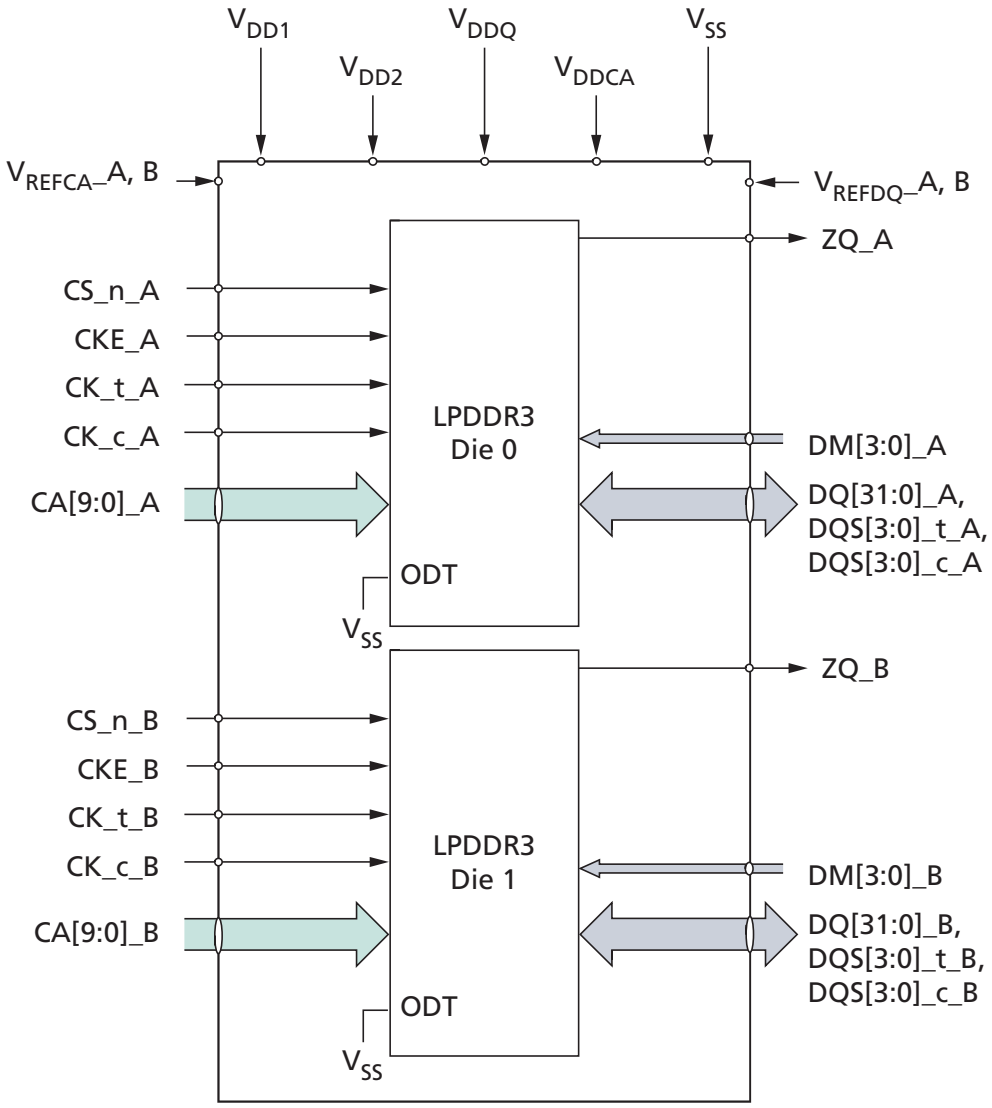
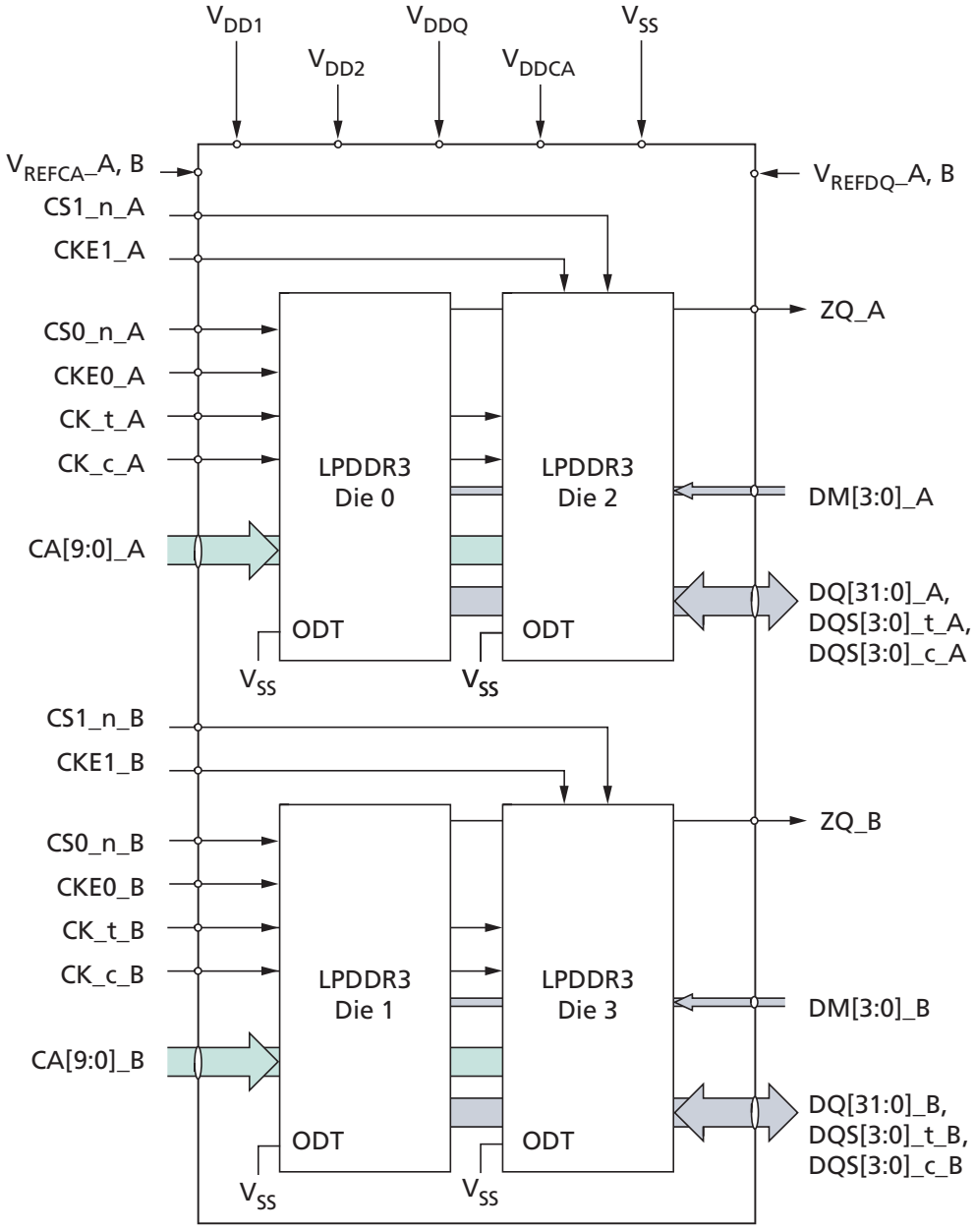


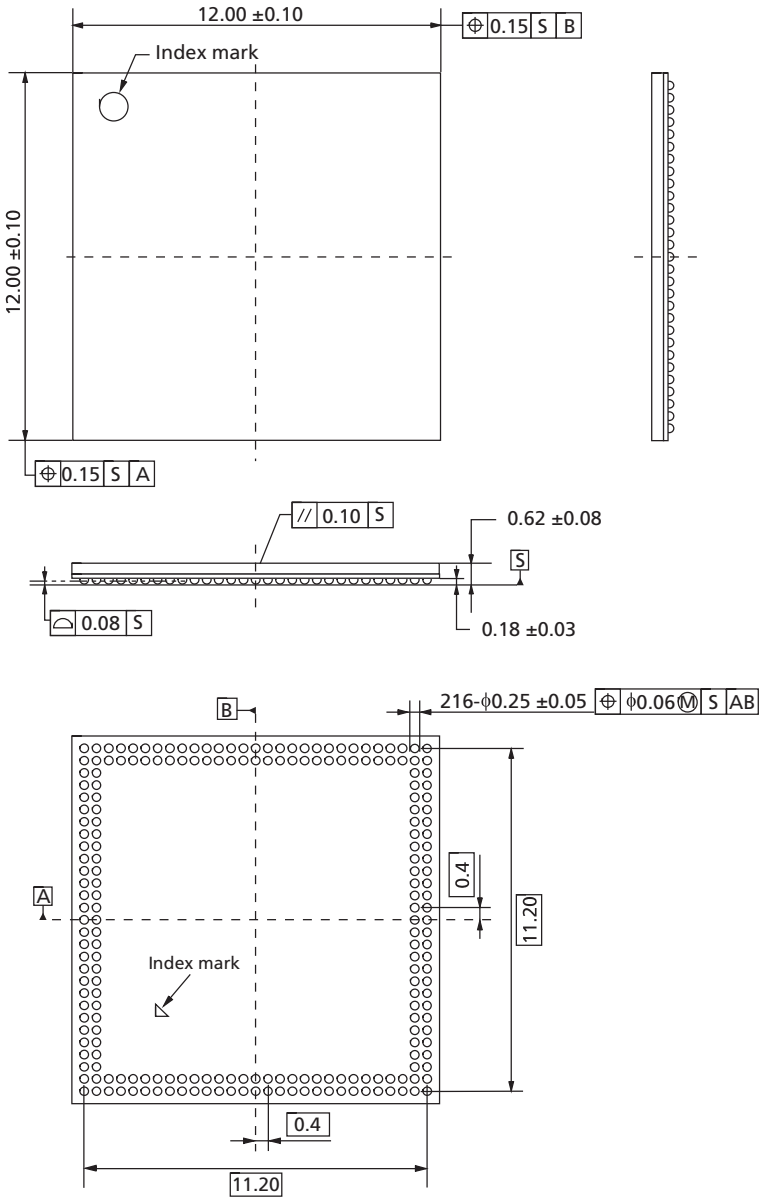
Figure 5: Quad-Die, Dual-Channel Package Block Diagram



Note: 1. The ODT input is connected to rank 0. The ODT input to rank 1 is connected to V_{SS} in the package.

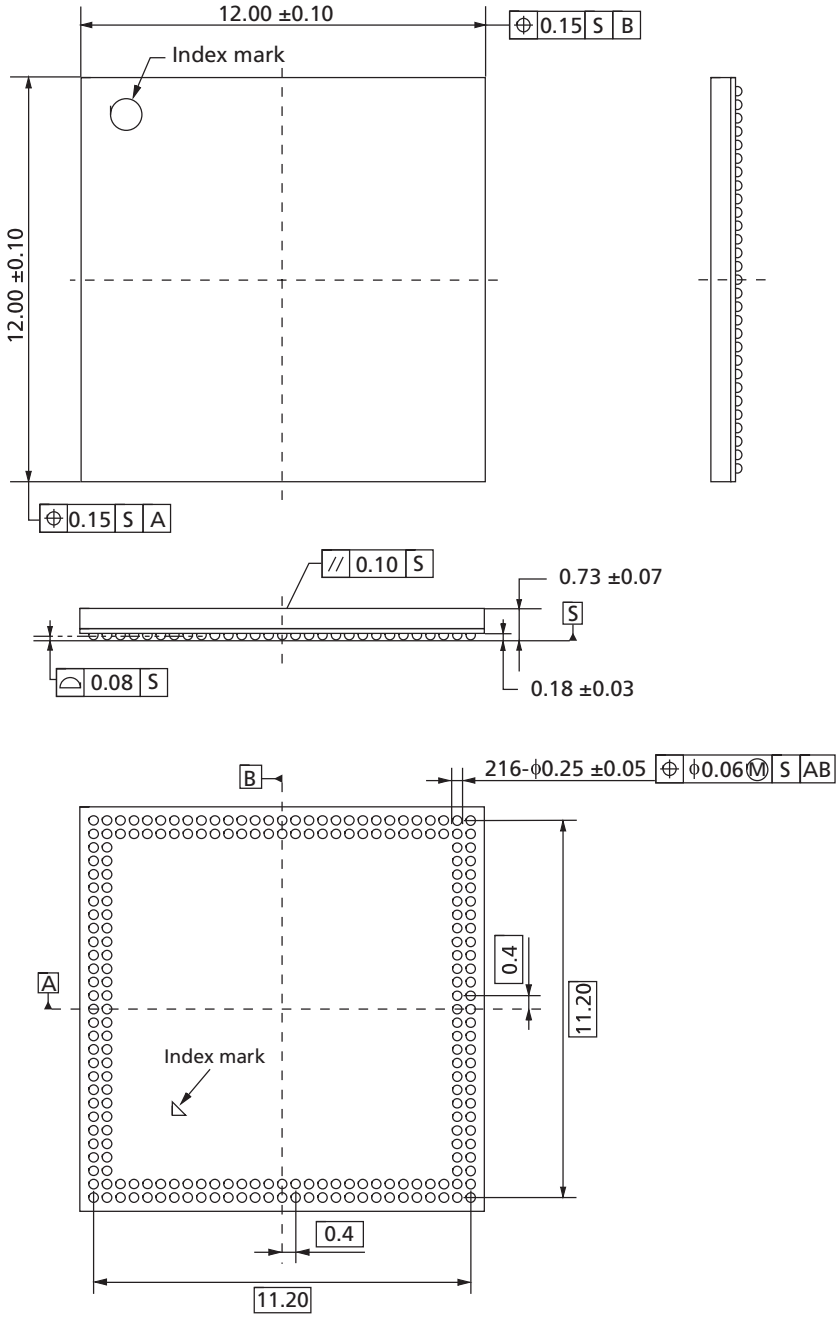
Package Dimensions

Figure 6: 216-Ball FBGA (12mm x 12mm) – EDF8164A3PK



Notes:
1. Package drawing: ECA-TS2-0498-01.
2. All dimensions are in millimeters.

Figure 7: 216-Ball FBGA (12mm x 12mm) – EDFA164A2PK



Notes: 1. Package drawing: ECA-TS2-0499-01.
2. All dimensions are in millimeters.

MR0, MR5–MR8 Readout

Table 5: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	OP6 = 1b indicates support for WL set B OP7 = 1b indicates that the option for RL3 is supported OP6 and OP7 =1b for this package							
MR5	Manufacturer ID = 0000 0011b							
MR6	Revision ID1 = 0000 0010b: Revision C							
MR7	Revision ID2 = (RFU)							
MR8	**I/O Width**		**Density**				**Type**	
	00b: x32		0110b: 4Gb				11b: S8	

Note: 1. The contents of MR0 and MR5–MR8 will reflect the manufacturer ID, die revision, and interface configurations for each die for each package.

I_{DD} Specifications – Dual Die, Dual Channel

Table 6: I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –30°C to +85°C

Symbol	Supply	Speed		Unit	Parameter/Condition
		1600	1333		
I_{DD01}	V_{DD1}	12	12	mA	All devices in operating one bank active-precharge ^tCK = ^tCK(avg) MIN; ^tRC = ^tRC (MIN); CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD02}	V_{DD2}	60	60		
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	12	12		
I_{DD2P1}	V_{DD1}	0.8	0.8	mA	All devices in idle power-down standby current ^tCK = ^tCK(avg) MIN; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD2P2}	V_{DD2}	1.8	1.8		
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	0.2	0.2		
I_{DD2PS1}	V_{DD1}	0.8	0.8	mA	All devices in idle power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD2PS2}	V_{DD2}	1.8	1.8		
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	0.2	0.2		
I_{DD2N1}	V_{DD1}	0.8	0.8	mA	All devices in idle non power-down standby current ^tCK = ^tCK(avg) MIN; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD2N2}	V_{DD2}	23	22		
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	12	12		
I_{DD2NS1}	V_{DD1}	0.8	0.8	mA	All devices in idle non power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD2NS2}	V_{DD2}	19	19		
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	12	12		
I_{DD3P1}	V_{DD1}	1.4	1.4	mA	All devices in active power-down standby current ^tCK = ^tCK(avg) MIN; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD3P2}	V_{DD2}	10	10		
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.2	0.2		
I_{DD3PS1}	V_{DD1}	1.4	1.4	mA	All devices in active power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD3PS2}	V_{DD2}	10	10		
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.2	0.2		
I_{DD3N1}	V_{DD1}	2.0	2.0	mA	All devices in active non power-down standby current ^tCK = ^tCK(avg) MIN; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD3N2}	V_{DD2}	25	24		
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	12	12		

Table 6: I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –30°C to +85°C

Symbol	Supply	Speed		Unit	Parameter/Condition
		1600	1333		
I_{DD3NS1}	V_{DD1}	2.0	2.0	mA	All devices in active non power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD3NS2}	V_{DD2}	21	21		
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	12	12		
I_{DD4R1}	V_{DD1}	4.0	4.0	mA	All devices in operating burst read ^tCK = ^tCK(avg) MIN; CS_n is HIGH between valid commands; One bank is active; BL = 8; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I_{DD4R2}	V_{DD2}	400	350		
$I_{DD4R,in}$	V_{DDCA}	12	12		
I_{DD4W1}	V_{DD1}	4.0	4.0	mA	All devices in operating burst write ^tCK = ^tCK(avg) MIN; CS_n is HIGH between valid commands; One bank is active; BL = 8; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I_{DD4W2}	V_{DD2}	380	330		
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	12	12		
I_{DD51}	V_{DD1}	40	40	mA	All devices in all bank auto-refresh ^tCK = ^tCK(avg) MIN; CKE is HIGH between valid commands; ^tRC = ^tRFCab (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD52}	V_{DD2}	200	200		
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	12	12		
I_{DD5AB1}	V_{DD1}	4.0	4.0	mA	All devices in all bank auto-refresh ^tCK = ^tCK(avg) MIN; CKE is HIGH between valid commands; ^tRC = ^tREFI; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD5AB2}	V_{DD2}	24	23		
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	12	12		
I_{DD5PB1}	V_{DD1}	4.0	4.0	mA	All devices in per bank auto-refresh ^tCK = ^tCK(avg) MIN; CKE is HIGH between valid commands; ^tRC = ^tREFIpb; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD5PB2}	V_{DD2}	24	23		
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	12	12		
I_{DD81}	V_{DD1}	32	32	µA	All devices in deep power-down CK_t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD82}	V_{DD2}	12	12		
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	24	24		

Notes:
1. Published I_{DD} values are the maximum of the distribution of the arithmetic mean.
2. I_{DD} current specifications are tested after the device is properly initialized.

Table 7: I_{DD6} Partial-Array Self Refresh Current at 45°C

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit	Parameter/Condition
Full array	V_{DD1}	400	µA	**All devices in self-refresh** CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V_{DD2}	1600		
	V_{DDCA} + V_{DDQ}	20		
1/2 array	V_{DD1}	320		
	V_{DD2}	1000		
	V_{DDCA} + V_{DDQ}	20		
1/4 array	V_{DD1}	260		
	V_{DD2}	600		
	V_{DDCA} + V_{DDQ}	20		
1/8 array	V_{DD1}	240		
	V_{DD2}	400		
	V_{DDCA} + V_{DDQ}	20		

Note: 1. I_{DD6} 45°C is typical of the distribution of the arithmetic mean.

Table 8: I_{DD6} Partial-Array Self Refresh Current at 85°C

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit	Parameter/Condition
Full array	V_{DD1}	1800	µA	**All devices in self refresh** CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V_{DD2}	6400		
	V_{DDCA} + V_{DDQ}	24		
1/2 array	V_{DD1}	1300		
	V_{DD2}	4400		
	V_{DDCA} + V_{DDQ}	24		
1/4 array	V_{DD1}	1100		
	V_{DD2}	3400		
	V_{DDCA} + V_{DDQ}	24		
1/8 array	V_{DD1}	1000		
	V_{DD2}	2800		
	V_{DDCA} + V_{DDQ}	24		

Note: 1. I_{DD6} 85°C is the maximum of the distribution of the arithmetic mean.

I_{DD} Specifications – Quad Die, Dual Channel

Table 9: I_{DD} Specifications

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –30°C to +85°C

Symbol	Supply	Speed			Unit	Parameter/Condition
		1866	1600	1333		
I_{DD01}	V_{DD1}	12	12	12	mA	2 devices in operating one bank active-precharge; 2 devices in deep power-down. Conditions for operating devices are: ^{t}CK = ^{t}CK(avg) MIN;^{t}RC = ^{t}RC (MIN); CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD02}	V_{DD2}	62	60	60		
$I_{DD0,in}$	V_{DDCA} + V_{DDQ}	12	12	12		
I_{DD2P1}	V_{DD1}	1.6	1.6	1.6	mA	All devices in idle power-down standby current ^{t}CK = ^{t}CK(avg) MIN; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD2P2}	V_{DD2}	3.6	3.6	3.6		
$I_{DD2P,in}$	V_{DDCA} + V_{DDQ}	0.4	0.4	0.4		
I_{DD2PS1}	V_{DD1}	1.6	1.6	1.6	mA	All devices in idle power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD2PS2}	V_{DD2}	3.6	3.6	3.6		
$I_{DD2PS,in}$	V_{DDCA} + V_{DDQ}	0.4	0.4	0.4		
I_{DD2N1}	V_{DD1}	1.6	1.6	1.6	mA	All devices in idle non power-down standby current ^{t}CK = ^{t}CK(avg) MIN; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD2N2}	V_{DD2}	48	46	44		
$I_{DD2N,in}$	V_{DDCA} + V_{DDQ}	24	24	24		
I_{DD2NS1}	V_{DD1}	1.6	1.6	1.6	mA	All devices in idle non power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD2NS2}	V_{DD2}	38	38	38		
$I_{DD2NS,in}$	V_{DDCA} + V_{DDQ}	24	24	24		
I_{DD3P1}	V_{DD1}	2.8	2.8	2.8	mA	All devices in active power-down standby current ^{t}CK = ^{t}CK(avg) MIN; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD3P2}	V_{DD2}	20	20	20		
$I_{DD3P,in}$	V_{DDCA} + V_{DDQ}	0.4	0.4	0.4		
I_{DD3PS1}	V_{DD1}	2.8	2.8	2.8	mA	All devices in active power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD3PS2}	V_{DD2}	20	20	20		
$I_{DD3PS,in}$	V_{DDCA} + V_{DDQ}	0.4	0.4	0.4		

Table 9: I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –30°C to +85°C

Symbol	Supply	Speed			Unit	Parameter/Condition
		1866	1600	1333		
I_{DD3N1}	V_{DD1}	4.0	4.0	4.0	mA	All devices in active non power-down standby current ^tCK = ^tCK(avg) MIN; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD3N2}	V_{DD2}	52	50	48		
$I_{DD3N,in}$	V_{DDCA} + V_{DDQ}	24	24	24		
I_{DD3NS1}	V_{DD1}	4.0	4.0	4.0	mA	All devices in active non power-down standby current with clock stop CK_t = LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD3NS2}	V_{DD2}	42	42	42		
$I_{DD3NS,in}$	V_{DDCA} + V_{DDQ}	24	24	24		
I_{DD4R1}	V_{DD1}	4.0	4.0	4.0	mA	2 devices in operating burst read; 2 devices in deep power-down. Conditions for operating devices are: ^tCK = ^tCK(avg) MIN; CS_n is HIGH between valid commands; One bank is active; BL = 8; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I_{DD4R2}	V_{DD2}	460	400	350		
$I_{DD4R,in}$	V_{DDCA}	12	12	12		
I_{DD4W1}	V_{DD1}	4.0	4.0	4.0	mA	2 devices in operating burst write; 2 devices in deep power-down Conditions for operating devices are: ^tCK = ^tCK(avg) MIN; CS_n is HIGH between valid commands; One bank is active; BL = 8; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I_{DD4W2}	V_{DD2}	440	380	330		
$I_{DD4W,in}$	V_{DDCA} + V_{DDQ}	12	12	12		
I_{DD51}	V_{DD1}	40	40	40	mA	2 devices in all bank auto-refresh; 2 devices in deep power-down. Conditions for operating devices are: ^tCK = ^tCK(avg) MIN; CKE is HIGH between valid commands; ^tRC = ^tRFCab (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD52}	V_{DD2}	200	200	200		
$I_{DD5,in}$	V_{DDCA} + V_{DDQ}	12	12	12		
I_{DD5AB1}	V_{DD1}	4.0	4.0	4.0	mA	2 devices in all bank auto-refresh; 2 devices in deep power-down. Conditions for operating devices are: ^tCK = ^tCK(avg) MIN; CKE is HIGH between valid commands; ^tRC = ^tREFI; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD5AB2}	V_{DD2}	25	24	23		
$I_{DD5AB,in}$	V_{DDCA} + V_{DDQ}	12	12	12		

Table 9: I_{DD} Specifications (Continued)

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V; T_C = –30°C to +85°C

Symbol	Supply	Speed			Unit	Parameter/Condition
		1866	1600	1333		
I_{DD5PB1}	V_{DD1}	4.0	4.0	4.0	mA	2 devices in per bank auto-refresh; 2 devices in deep power-down. Conditions for operating devices are: ^{t}CK = $^{t}CK(avg)$ MIN; CKE is HIGH between valid commands; ^{t}RC = $^{t}REFIpb$; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I_{DD5PB2}	V_{DD2}	25	24	23		
$I_{DD5PB,in}$	V_{DDCA} + V_{DDQ}	12	12	12		
I_{DD81}	V_{DD1}	64	64	64	µA	All devices in deep power-down CK_t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
I_{DD82}	V_{DD2}	24	24	24		
$I_{DD8,in}$	V_{DDCA} + V_{DDQ}	48	48	48		

Notes:
1. Published I_{DD} values are the maximum of the distribution of the arithmetic mean.
2. I_{DD} current specifications are tested after the device is properly initialized.

Table 10: I_{DD6} Partial-Array Self Refresh Current at 45°C

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V_{DD1}	800	µA	**All devices in self refresh** CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V_{DD2}	3200		
	V_{DDCA} + V_{DDQ}	40		
1/2 array	V_{DD1}	640		
	V_{DD2}	2000		
	V_{DDCA} + V_{DDQ}	40		
1/4 array	V_{DD1}	520		
	V_{DD2}	1200		
	V_{DDCA} + V_{DDQ}	40		
1/8 array	V_{DD1}	480		
	V_{DD2}	800		
	V_{DDCA} + V_{DDQ}	40		

Note:
1. I_{DD6} 45°C is typical of the distribution of the arithmetic mean.

Table 11: I_{DD6} Partial-Array Self Refresh Current at 85°C

V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14–1.30V; V_{DD1} = 1.70–1.95V

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V_{DD1}	3600	µA	**All devices in self refresh** CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V_{DD2}	12,800		
	V_{DDCA} + V_{DDQ}	48		
1/2 array	V_{DD1}	2600		
	V_{DD2}	8800		
	V_{DDCA} + V_{DDQ}	48		
1/4 array	V_{DD1}	2200		
	V_{DD2}	6800		
	V_{DDCA} + V_{DDQ}	48		
1/8 array	V_{DD1}	2000		
	V_{DD2}	5600		
	V_{DDCA} + V_{DDQ}	48		

Note: 1. I_{DD6} 85°C is the maximum of the distribution of the arithmetic mean.