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# Embedded LPDDR3 SDRAM

**EDF8164A3PK, EDFA164A2PK**

## Features

- Ultra-low-voltage core and I/O power supplies
- Frequency range
  - 800/933 MHz (data rate: 1600/1866 Mb/s/pin)
- 8n prefetch DDR architecture
- 8 internal banks for concurrent operation
- Multiplexed, double data rate, command/address inputs; commands entered on each CK\_t/CK\_c edge
- Bidirectional/differential data strobe per byte of data (DQS\_t/DQS\_c)
- Programmable READ and WRITE latencies (RL/WL)
- Burst length: 8
- Per-bank refresh for concurrent operation
- Auto temperature-compensated self refresh (ATCSR) by built-in temperature sensor
- Partial-array self refresh (PASR)
- Deep power-down mode (DPD)
- Selectable output drive strength (DS)
- Clock-stop capability
- Lead-free (RoHS-compliant) and halogen-free packaging

## Options

- $V_{DD1}/V_{DD2}/V_{DDCA}/V_{DDQ}$ : 1.8V/1.2V/1.2V/1.2V
- Array configuration
  - 128 Meg x 64 (DDP)
  - 256 Meg x 64 (QDP)
- Packaging
  - 12mm x 12mm, 216-ball PoP FBGA package
- Operating temperature range
  - From -30°C to +85°C

**Table 1: Configuration Addressing**

Architecture	128 Meg x 64	256 Meg x 64
Density per package	8Gb	16Gb
Die per package	2	4
Ranks (CS_n) per channel	1	2
Die per channel	1	2
Configuration	16 Meg x 32 x 8 banks x 2 channel	16 Meg x 32 x 8 banks x 2 rank x 2 channel
Row addressing	16K A[13:0]	16K A[13:0]
Column addressing (same for each die)	1K A[9:0]	1K A[9:0]



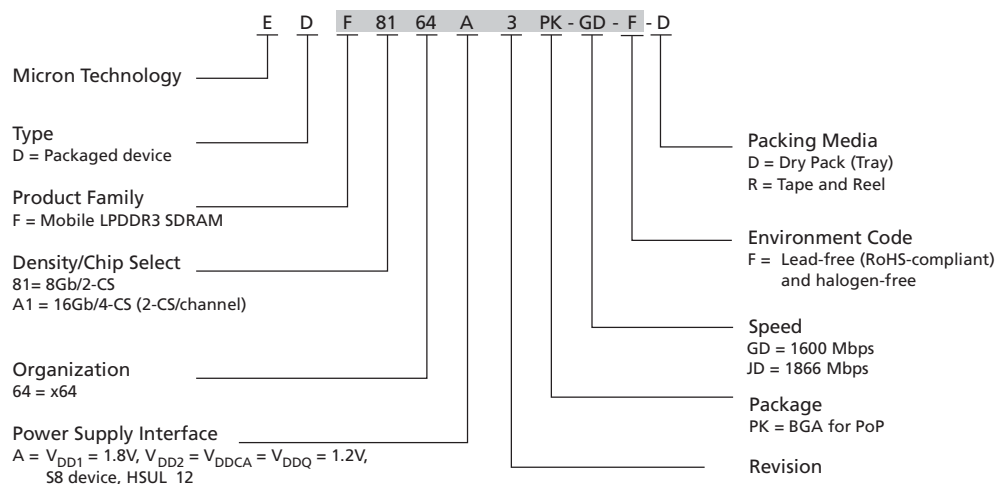
# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM Features

**Table 2: Key Timing Parameters**

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency (Set A/B)	READ Latency
GD	800	1600	6/9	12
JD	933	1866	8/11	14

**Table 3: Part Number Description**

Part Number	Total Density	Configuration	Ranks	Channels	Package Size	Ball Pitch
EDF8164A3PK-GD-F-D EDF8164A3PK-GD-F-R EDF8164A3PK-JD-F-D EDF8164A3PK-JD-F-R	8Gb	128 Meg x 64	1	2	12mm x 12mm (0.70mm MAX height)	0.40mm
EDFA164A2PK-GD-F-D EDFA164A2PK-GD-F-R EDFA164A2PK-JD-F-D EDFA164A2PK-JD-F-R	16Gb	256 Meg x 64	2	2	12mm x 12mm (0.80mm MAX height)	0.40mm

**Figure 1: Marketing Part Number Chart**


Note: 1. The characters highlighted in gray indicate the physical part marking found on the device.





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## Ball Assignments

Figure 2: 216-Ball FBGA – 2 x 4Gb Die

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	NC	V <sub>SS</sub>	V <sub>DD2</sub>	DQ30_A	DQ28_A	V <sub>SS</sub>	DQ26_A	DQ25_A	V <sub>SS</sub>	DQS15_A	V <sub>SS</sub>	DQ14_A	DQ13_A	V <sub>SS</sub>	NC	V <sub>DD2</sub>	DQ11_A	DQ10_A	DQ9_A	DQS1_A	DM1_A	V <sub>DD2</sub>	DQS0_A	DQ7_A	DQ6_A	DQ4_A	DQ3_A	V <sub>SS</sub>	NC
B	V <sub>SS</sub>	NC	DQ31_A	V <sub>DD2</sub>	DQ28_A	DQ27_A	V <sub>DD2</sub>	DQ24_A	V <sub>DD2</sub>	DQS1_A	DM3_A	DQ15_A	V <sub>DD2</sub>	V <sub>SS</sub>	V <sub>REFDQ_A</sub>	V <sub>DD2</sub>	DQ12_A	V <sub>DD2</sub>	DQ8_A	DQS1_A	V <sub>SS</sub>	DM0_A	DQS0_A	V <sub>SS</sub>	V <sub>DD2</sub>	DQ5_A	DQ2_A	NC	V <sub>SS</sub>
C	V <sub>DD1</sub>	DQ16_B																										V <sub>DD1</sub>	V <sub>DD2</sub>
D	DQ17_B	V <sub>DD2</sub>																										DQ1_A	V <sub>DD2</sub>
E	DQ18_B	DQ19_B																										V <sub>SS</sub>	DQ0_A
F	V <sub>SS</sub>	DQ20_B																										DM2_A	V <sub>DD2</sub>
G	DQ21_B	V <sub>DD2</sub>																										DQS2_A	DQS2_A
H	DQ22_B	DQ23_B																										V <sub>SS</sub>	DQ23_A
J	V <sub>SS</sub>	V <sub>DD2</sub>																										V <sub>DD2</sub>	DQ22_A
K	DQS2_A	DQS2_A																										DQ20_A	DQ21_A
L	DM2_B	DQ0_B																										DQ19_A	V <sub>SS</sub>
M	DQ1_A	V <sub>SS</sub>																										V <sub>DD2</sub>	DQ18_A
N	DQ2_B	V <sub>DD1</sub>																										DQ16_A	DQ17_A
P	V <sub>SS</sub>	V <sub>SS</sub>																										V <sub>DD2</sub>	NC
R	V <sub>DD1</sub>	V <sub>REFDQ_B</sub>																										V <sub>SS</sub>	CA0_B
T	V <sub>DD2</sub>	V <sub>DD2</sub>																										V <sub>DD2</sub>	CA1_B
U	V <sub>DD2</sub>	DQ3_B																										V <sub>REFDQ_B</sub>	CA2_B
V	DQ4_B	V <sub>SS</sub>																										V <sub>SS</sub>	CA3_B
W	DQ5_B	DQ5_B																										CA4_B	NC
Y	V <sub>DD2</sub>	DQ7_B																										CS1_B	NC
AA	DQS0_B	DQS0_B																										V <sub>SS</sub>	CKE_B
AB	DM0_B	V <sub>SS</sub>																										CK1_B	CK1_B
AC	V <sub>DD2</sub>	DM1_B																										V <sub>DD2</sub>	CA5_B
AD	DQS1_B	DQS1_B																										CA7_B	CA8_B
AE	DQ8_B	V <sub>SS</sub>																										CA8_B	V <sub>DD2</sub>
AF	DQ9_B	V <sub>DD2</sub>																										V <sub>SS</sub>	CA9_B
AG	DQ10_B	DQ11_B																										V <sub>DD2</sub>	ZQ_B
AH	V <sub>SS</sub>	V <sub>DD1</sub>	V <sub>DD2</sub>	DQ13_B	V <sub>SS</sub>	DQ15_B	DM3_B	DQS3_B	V <sub>DD2</sub>	DQ26_B	DQ27_B	V <sub>DD2</sub>	DQ30_B	V <sub>SS</sub>	V <sub>DD2</sub>	V <sub>REFDQ_B</sub>	CA9_A	V <sub>SS</sub>	CAT_A	CA6_A	CK1_A	V <sub>DD2</sub>	CKE_A	CS1_A	CA3_A	CA2_A	CA1_A	V <sub>DD1</sub>	V <sub>SS</sub>
AJ	NC	V <sub>SS</sub>	DQ12_B	V <sub>DD2</sub>	DQ14_B	V <sub>DD2</sub>	V <sub>SS</sub>	DQS4_B	DQ24_B	V <sub>SS</sub>	DQ28_B	DQ29_B	DQ31_B	NC	V <sub>SS</sub>	ZQ_A	CA8_A	V <sub>DD2</sub>	CA5_A	CK1_A	V <sub>SS</sub>	NC	NC	CA4_A	V <sub>DD2</sub>	CA0_A	V <sub>SS</sub>	NC	NC

Top View (ball down)

Channel a (A) Channel b (B) Supply Ground



## Ball Assignments

Figure 3: 216-Ball FBGA – 4 x 4Gb Die

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	NC	V <sub>SS</sub>	V <sub>DD2</sub>	DQ30_A	DQ29_A	V <sub>SS</sub>	DQ26_A	DQ25_A	V <sub>SS</sub>	DQS3_LA	V <sub>SS</sub>	DQ14_A	DQ13_A	V <sub>SS</sub>	NC	V <sub>DD2</sub>	DQ11_A	DQ10_A	DQ8_A	DQS1_LA	DM1_A	V <sub>DDQ</sub>	DQS0_LA	DQ7_A	DQ6_A	DQ4_A	DQ3_A	V <sub>SS</sub>	NC
B	V <sub>SS</sub>	NC	DQ31_A	V <sub>DDQ</sub>	DQ28_A	DQ27_A	V <sub>DDQ</sub>	DQ24_A	V <sub>DDQ</sub>	DQS3_LA	DM3_A	DQ15_A	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>REFDQ_A</sub>	V <sub>DD2</sub>	DQ12_A	V <sub>DDQ</sub>	DQ8_A	DQS1_LA	V <sub>SS</sub>	DM0_A	DQS0_LA	V <sub>SS</sub>	V <sub>DDQ</sub>	DQ5_A	DQ2_A	NC	V <sub>SS</sub>
C	V <sub>DD1</sub>	DQ16_B																										V <sub>DD1</sub>	V <sub>DD2</sub>
D	DQ17_B	V <sub>DDQ</sub>																										DQ1_A	V <sub>DDQ</sub>
E	DQ18_B	DQ19_B																										V <sub>SS</sub>	DQ0_A
F	V <sub>SS</sub>	DQ20_B																										DM2_A	V <sub>DDQ</sub>
G	DQ21_B	V <sub>DDQ</sub>																										DQS2_LA	DQS2_LA
H	DQ22_B	DQ23_B																										V <sub>SS</sub>	DQ23_A
J	V <sub>SS</sub>	V <sub>DDQ</sub>																										V <sub>DDQ</sub>	DQ22_A
K	DQS2_LA	DQS2_LA																										DQ20_A	DQ21_A
L	DM2_B	DQ0_B																										DQ19_A	V <sub>SS</sub>
M	DQ1_B	V <sub>SS</sub>																										V <sub>DDQ</sub>	DQ18_A
N	DQ2_B	V <sub>DD1</sub>																										DQ18_A	DQ17_A
P	V <sub>SS</sub>	V <sub>SS</sub>																										V <sub>DD2</sub>	NC
R	V <sub>DD1</sub>	V <sub>REFDQ_B</sub>																										V <sub>SS</sub>	CA0_B
T	V <sub>DD2</sub>	V <sub>DD2</sub>																										V <sub>DDCA</sub>	CA1_B
U	V <sub>DDQ</sub>	DQ3_B																										V <sub>REFCA_B</sub>	CA2_B
V	DQ4_B	V <sub>SS</sub>																										V <sub>SS</sub>	CA3_B
W	DQ6_B	DQ5_B																										CA4_B	CS1_LB
Y	V <sub>DDQ</sub>	DQ7_B																										CS0_LB	CKE1_B
AA	DQS0_LA	DQS0_LA																										V <sub>SS</sub>	CKE0_B
AB	DM0_B	V <sub>SS</sub>																										CK_LB	CK_LB
AC	V <sub>DDQ</sub>	DM1_B																										V <sub>DDCA</sub>	CA5_B
AD	DQS1_LA	DQS1_LA																										CA7_B	CA6_B
AE	DQ8_B	V <sub>SS</sub>																										CA8_B	V <sub>DDCA</sub>
AF	DQ9_B	V <sub>DDQ</sub>																										V <sub>SS</sub>	CA9_B
AG	DQ10_B	DQ11_B																										V <sub>DD2</sub>	ZQ_B
AH	V <sub>SS</sub>	V <sub>DD1</sub>	V <sub>DD2</sub>	DQ13_B	V <sub>SS</sub>	DQ15_B	DM3_B	DQS3_LB	V <sub>DDQ</sub>	DQ26_B	DQ27_B	V <sub>DDQ</sub>	DQ20_B	V <sub>SS</sub>	V <sub>DD2</sub>	V <sub>REFCA_A</sub>	CA8_A	V <sub>SS</sub>	CAT_A	CA6_A	CK_LA	V <sub>DDCA</sub>	CKE0_A	CS0_LA	CA3_A	CA2_A	CA1_A	V <sub>DD1</sub>	V <sub>SS</sub>
AJ	NC	V <sub>SS</sub>	DQ12_B	V <sub>DDQ</sub>	DQ14_B	V <sub>DDQ</sub>	V <sub>SS</sub>	DQS3_LB	DQ24_B	DQ25_B	V <sub>SS</sub>	DQ28_B	DQ29_B	DQ31_B	NC	V <sub>SS</sub>	ZQ_A	CA8_A	V <sub>DDCA</sub>	CA5_A	CK1_A	V <sub>SS</sub>	CKE1_A	CS1_LA	CA4_A	V <sub>DDCA</sub>	CA0_A	V <sub>SS</sub>	NC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29

Top View (ball down)

Channel a (L\_A) Channel b (L\_B) Supply Ground





# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM Ball Descriptions

## Ball Descriptions

The ball/pad description table below is a comprehensive list of signals for the device family. All signals listed may not be supported on this device. See ball assignments for information specific to this device.

**Table 4: Ball/Pad Descriptions**

Symbol	Type	Description
CA[9:0]_A, CA[9:0]_B	Input	<b>Command/address inputs:</b> Provide the command and address inputs according to the command truth table. A separate CA[9:0] is provided for each channel (A and B).
CK_t_B, CK_t_A CK_c_B, CK_c_A	Input	<b>Clock:</b> Differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock. A separate CK_t/CK_c is provided for each channel (A and B).
CKE[1:0]_A, CKE[1:0]_B	Input	<b>Clock enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled on the rising edge of CK. A separate CKE is provided for each channel (A and B).
CS[1:0]_n_A, CS[1:0]_n_B	Input	<b>Chip select:</b> Considered part of the command code and is sampled on the rising edge of CK. A separate CS_n is provided for each channel (A and B).
DM[3:0]_B, DM[3:0]_A	Input	<b>Input data mask:</b> Input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM[3:0] is DM for each of the four data bytes, respectively. A separate DM[3:0] is provided for each channel (A and B).
ODT_B, ODT_A	Input	<b>On-die termination:</b> Enables and disables termination on the DRAM DQ bus according to the specified mode register settings. For packages that do not support ODT, the ODT signal may be grounded internally. A separate ODT provided for each channel (A and B).
DQ[31:0]_B, DQ[31:0]_A	I/O	<b>Data input/output:</b> Bidirectional data bus. A separate DQ[11:0] is provided for each channel (A and B).
DQS[3:0]_t_B, DQS[3:0]_t_A, DQS[3:0]_c_B, DQS[3:0]_c_A	I/O	<b>Data strobe:</b> Bidirectional (used for read and write data) and complementary (DQS_t and DQS_c). It is edge-aligned output with read data and centered input with write data. DQS[3:0]_t/DQS[3:0]_c is DQS for each of the four data bytes, respectively. A separate DQS[3:0]_t and DQS[3:0]_c is provided for each channel (A and B).
V <sub>DDQ</sub>	Supply	<b>DQ power supply:</b> Isolated on the die for improved noise immunity.
V <sub>SSQ</sub>	Supply	<b>DQ ground:</b> Isolated on the die for improved noise immunity.
V <sub>DDCA</sub>	Supply	<b>Command/address power supply:</b> Command/address power supply.
V <sub>SSCA</sub>	Supply	<b>Command/address ground:</b> Isolated on the die for improved noise immunity.
V <sub>DD1</sub>	Supply	<b>Core power:</b> Supply 1.
V <sub>DD2</sub>	Supply	<b>Core power:</b> Supply 2.
V <sub>SS</sub>	Supply	<b>Common ground.</b>
V <sub>REFCA</sub> _B, V <sub>REFCA</sub> _A V <sub>REFDQ</sub> _B, V <sub>REFDQ</sub> _A	Supply	<b>Reference voltage:</b> V <sub>REFCA</sub> is reference for command/address input buffers, V <sub>REFDQ</sub> is reference for DQ input buffers. A separate V <sub>REFCA</sub> and V <sub>REFDQ</sub> provided for each channel (A and B).
ZQ_B, ZQ_A	Reference	<b>External reference ball for output drive calibration:</b> This ball is tied to an external 240Ω resistor (RZQ), which is tied to V <sub>SSQ</sub> . A separate ZQ is provided for each channel (A and B).



# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM Ball Descriptions

**Table 4: Ball/Pad Descriptions (Continued)**

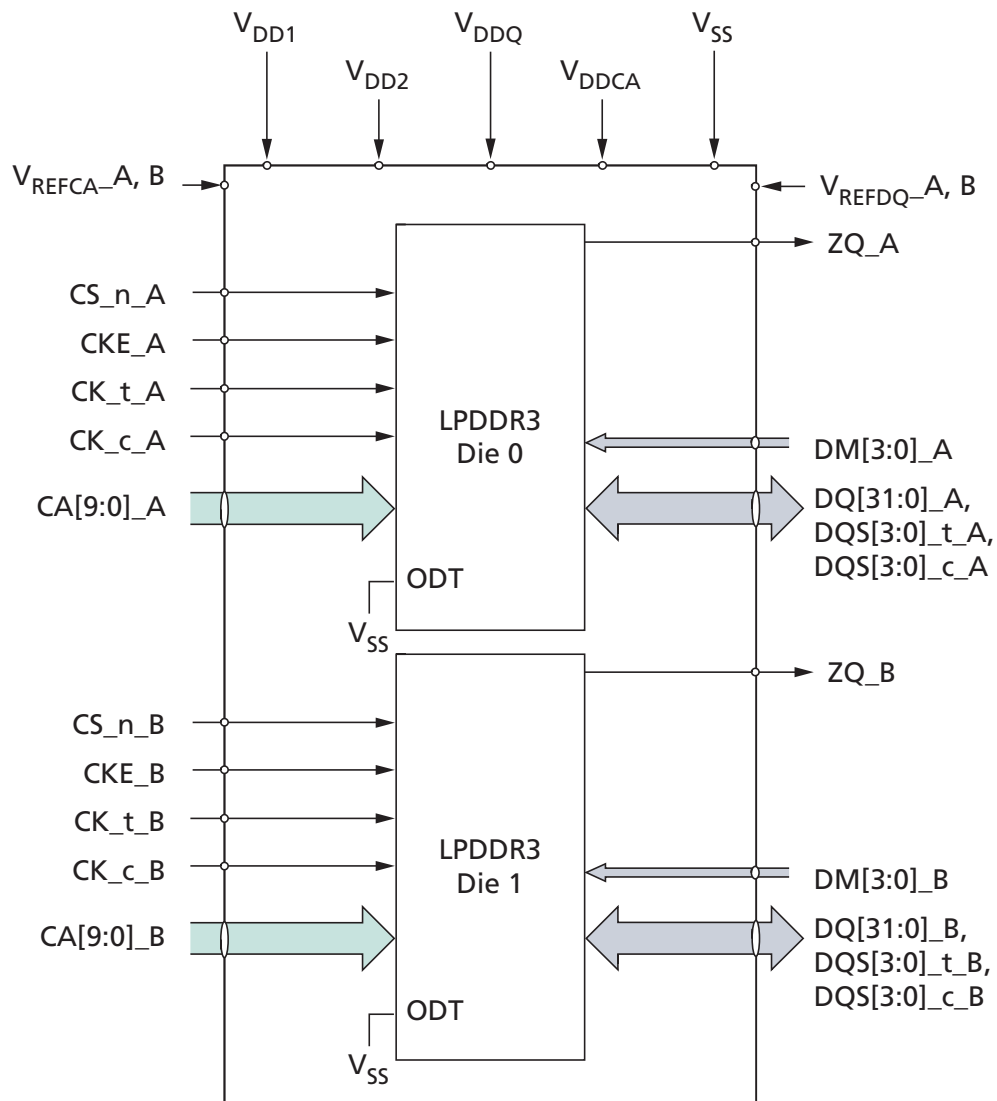
Symbol	Type	Description
DNU	–	<b>Do not use:</b> Must be grounded or left floating.
NC	–	<b>No connect:</b> Not internally connected.
(NC)	–	<b>No connect:</b> Balls indicated as (NC) are no connects; however, they could be connected together internally.



# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM Package Block Diagrams

## Package Block Diagrams

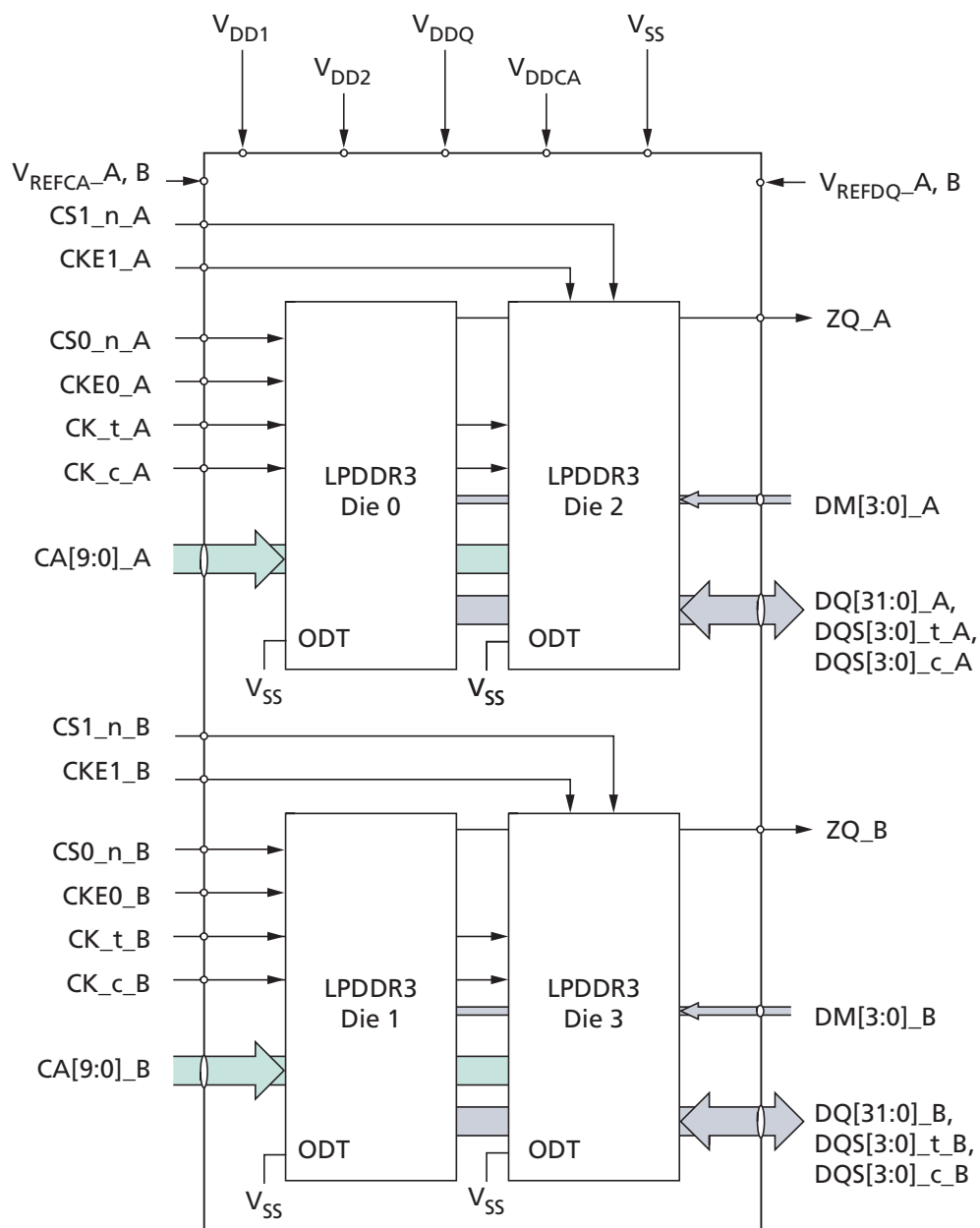
**Figure 4: Dual-Die, Dual-Channel Package Block Diagram**





# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM Package Block Diagrams

**Figure 5: Quad-Die, Dual-Channel Package Block Diagram**



Note: 1. The ODT input is connected to rank 0. The ODT input to rank 1 is connected to  $V_{SS}$  in the package.

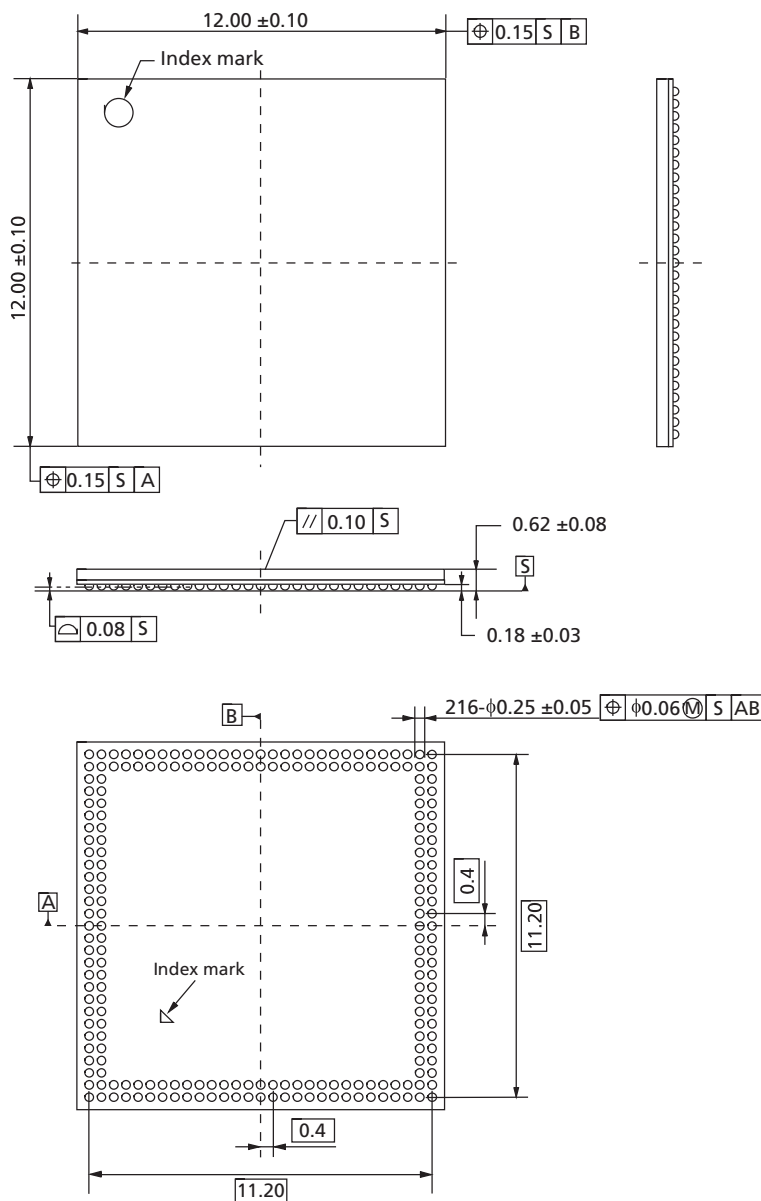




# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM Package Dimensions

## Package Dimensions

Figure 6: 216-Ball FBGA (12mm x 12mm) – EDF8164A3PK

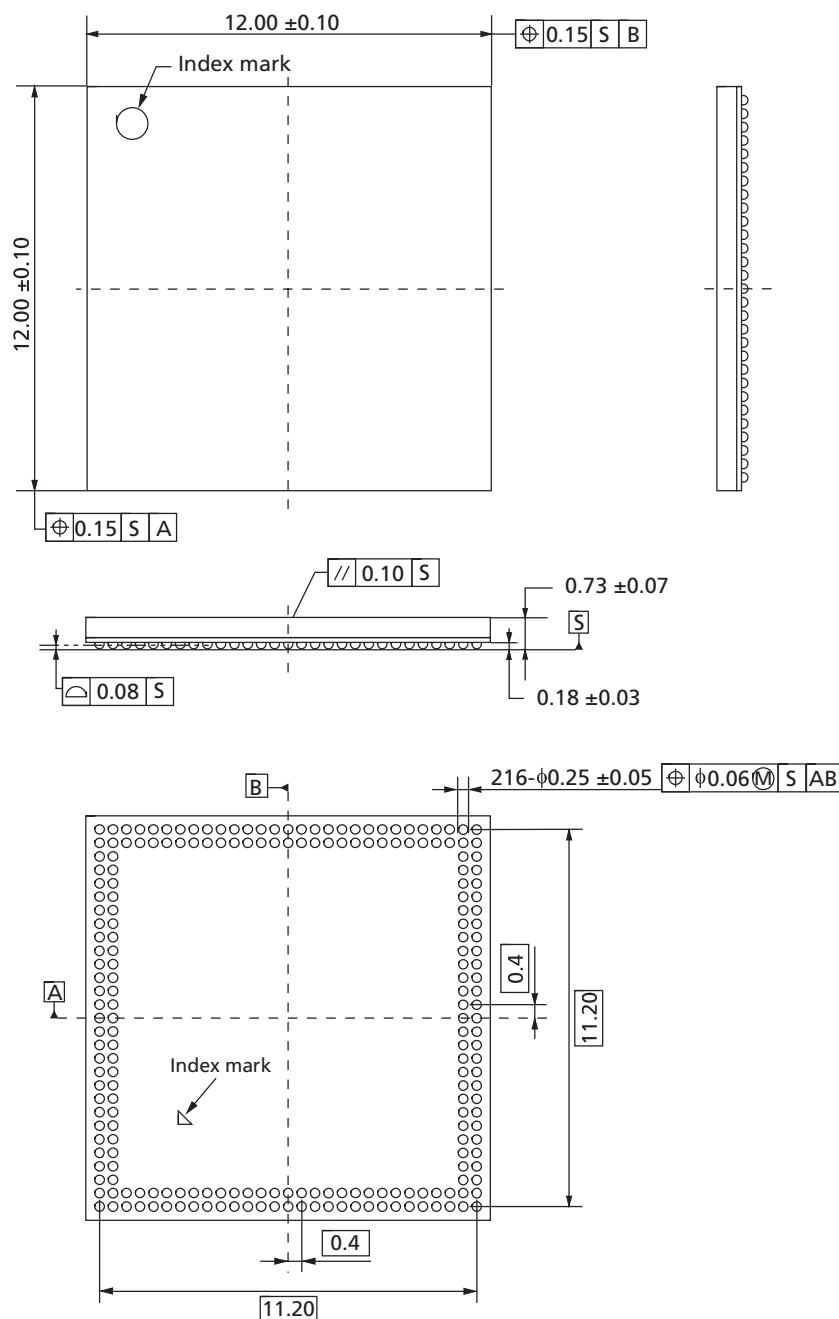


- Notes: 1. Package drawing: ECA-TS2-0498-01.  
2. All dimensions are in millimeters.



# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM Package Dimensions

**Figure 7: 216-Ball FBGA (12mm x 12mm) – EDFA164A2PK**



- Notes: 1. Package drawing: ECA-TS2-0499-01.  
2. All dimensions are in millimeters.



# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM MR0, MR5–MR8 Readout

## MR0, MR5–MR8 Readout

**Table 5: Mode Register Contents**

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	OP6 = 1b indicates support for WL set B OP7 = 1b indicates that the option for RL3 is supported OP6 and OP7 = 1b for this package							
MR5	Manufacturer ID = 0000 0011b							
MR6	Revision ID1 = 0000 0010b: Revision C							
MR7	Revision ID2 = (RFU)							
MR8	<b>I/O Width</b>		<b>Density</b>				<b>Type</b>	
	00b: x32		0110b: 4Gb				11b: S8	

Note: 1. The contents of MR0 and MR5–MR8 will reflect the manufacturer ID, die revision, and interface configurations for each die for each package.



# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM I<sub>DD</sub> Specifications – Dual Die, Dual Channel

## I<sub>DD</sub> Specifications – Dual Die, Dual Channel

**Table 6: I<sub>DD</sub> Specifications**

V<sub>DD2</sub>, V<sub>DDQ</sub>, V<sub>DDCA</sub> = 1.14–1.30V; V<sub>DD1</sub> = 1.70–1.95V; T<sub>C</sub> = –30°C to +85°C

Symbol	Supply	Speed		Unit	Parameter/Condition
		1600	1333		
I <sub>DD01</sub>	V <sub>DD1</sub>	12	12	mA	All devices in operating one bank active-precharge t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; t <sub>RC</sub> = t <sub>RC</sub> (MIN); CKE is HIGH; CS <sub>n</sub> is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD02</sub>	V <sub>DD2</sub>	60	60		
I <sub>DD0,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12		
I <sub>DD2P1</sub>	V <sub>DD1</sub>	0.8	0.8	mA	All devices in idle power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is LOW; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD2P2</sub>	V <sub>DD2</sub>	1.8	1.8		
I <sub>DD2P,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.2	0.2		
I <sub>DD2PS1</sub>	V <sub>DD1</sub>	0.8	0.8	mA	All devices in idle power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD2PS2</sub>	V <sub>DD2</sub>	1.8	1.8		
I <sub>DD2PS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.2	0.2		
I <sub>DD2N1</sub>	V <sub>DD1</sub>	0.8	0.8	mA	All devices in idle non power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD2N2</sub>	V <sub>DD2</sub>	23	22		
I <sub>DD2N,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12		
I <sub>DD2NS1</sub>	V <sub>DD1</sub>	0.8	0.8	mA	All devices in idle non power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is HIGH; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD2NS2</sub>	V <sub>DD2</sub>	19	19		
I <sub>DD2NS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12		
I <sub>DD3P1</sub>	V <sub>DD1</sub>	1.4	1.4	mA	All devices in active power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is LOW; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD3P2</sub>	V <sub>DD2</sub>	10	10		
I <sub>DD3P,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.2	0.2		
I <sub>DD3PS1</sub>	V <sub>DD1</sub>	1.4	1.4	mA	All devices in active power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD3PS2</sub>	V <sub>DD2</sub>	10	10		
I <sub>DD3PS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.2	0.2		
I <sub>DD3N1</sub>	V <sub>DD1</sub>	2.0	2.0	mA	All devices in active non power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD3N2</sub>	V <sub>DD2</sub>	25	24		
I <sub>DD3N,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12		





# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM I<sub>DD</sub> Specifications – Dual Die, Dual Channel

**Table 6: I<sub>DD</sub> Specifications (Continued)**
 $V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}; T_C = -30^\circ\text{C to } +85^\circ\text{C}$ 

Symbol	Supply	Speed		Unit	Parameter/Condition
		1600	1333		
I <sub>DD3NS1</sub>	V <sub>DD1</sub>	2.0	2.0	mA	All devices in active non power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is HIGH; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD3NS2</sub>	V <sub>DD2</sub>	21	21		
I <sub>DD3NS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12		
I <sub>DD4R1</sub>	V <sub>DD1</sub>	4.0	4.0	mA	All devices in operating burst read t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CS <sub>n</sub> is HIGH between valid commands; One bank is active; BL = 8; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I <sub>DD4R2</sub>	V <sub>DD2</sub>	400	350		
I <sub>DD4R,in</sub>	V <sub>DDCA</sub>	12	12		
I <sub>DD4W1</sub>	V <sub>DD1</sub>	4.0	4.0	mA	All devices in operating burst write t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CS <sub>n</sub> is HIGH between valid commands; One bank is active; BL = 8; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I <sub>DD4W2</sub>	V <sub>DD2</sub>	380	330		
I <sub>DD4W,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12		
I <sub>DD51</sub>	V <sub>DD1</sub>	40	40	mA	All devices in all bank auto-refresh t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH between valid commands; t <sub>RC</sub> = t <sub>RFCab</sub> (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD52</sub>	V <sub>DD2</sub>	200	200		
I <sub>DD5,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12		
I <sub>DD5AB1</sub>	V <sub>DD1</sub>	4.0	4.0	mA	All devices in all bank auto-refresh t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH between valid commands; t <sub>RC</sub> = t <sub>REFI</sub> ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD5AB2</sub>	V <sub>DD2</sub>	24	23		
I <sub>DD5AB,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12		
I <sub>DD5PB1</sub>	V <sub>DD1</sub>	4.0	4.0	mA	All devices in per bank auto-refresh t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH between valid commands; t <sub>RC</sub> = t <sub>REFIpb</sub> ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD5PB2</sub>	V <sub>DD2</sub>	24	23		
I <sub>DD5PB,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12		
I <sub>DD81</sub>	V <sub>DD1</sub>	32	32	μA	All devices in deep power-down CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD82</sub>	V <sub>DD2</sub>	12	12		
I <sub>DD8,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	24	24		

- Notes: 1. Published I<sub>DD</sub> values are the maximum of the distribution of the arithmetic mean.  
2. I<sub>DD</sub> current specifications are tested after the device is properly initialized.



# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM I<sub>DD</sub> Specifications – Dual Die, Dual Channel

**Table 7: I<sub>DD6</sub> Partial-Array Self Refresh Current at 45°C**
 $V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

PASR	Supply	Value	Unit	Parameter/Condition
Full array	V <sub>DD1</sub>	400	μA	<b>All devices in self-refresh</b> CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V <sub>DD2</sub>	1600		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	20		
1/2 array	V <sub>DD1</sub>	320		
	V <sub>DD2</sub>	1000		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	20		
1/4 array	V <sub>DD1</sub>	260		
	V <sub>DD2</sub>	600		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	20		
1/8 array	V <sub>DD1</sub>	240		
	V <sub>DD2</sub>	400		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	20		

Note: 1. I<sub>DD6</sub> 45°C is typical of the distribution of the arithmetic mean.

**Table 8: I<sub>DD6</sub> Partial-Array Self Refresh Current at 85°C**
 $V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

PASR	Supply	Value	Unit	Parameter/Condition
Full array	V <sub>DD1</sub>	1800	μA	<b>All devices in self refresh</b> CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V <sub>DD2</sub>	6400		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	24		
1/2 array	V <sub>DD1</sub>	1300		
	V <sub>DD2</sub>	4400		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	24		
1/4 array	V <sub>DD1</sub>	1100		
	V <sub>DD2</sub>	3400		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	24		
1/8 array	V <sub>DD1</sub>	1000		
	V <sub>DD2</sub>	2800		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	24		

Note: 1. I<sub>DD6</sub> 85°C is the maximum of the distribution of the arithmetic mean.



# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM I<sub>DD</sub> Specifications – Quad Die, Dual Channel

## I<sub>DD</sub> Specifications – Quad Die, Dual Channel

**Table 9: I<sub>DD</sub> Specifications**

V<sub>DD2</sub>, V<sub>DDQ</sub>, V<sub>DDCA</sub> = 1.14–1.30V; V<sub>DD1</sub> = 1.70–1.95V; T<sub>C</sub> = –30°C to +85°C

Symbol	Supply	Speed			Unit	Parameter/Condition
		1866	1600	1333		
I <sub>DD01</sub>	V <sub>DD1</sub>	12	12	12	mA	2 devices in operating one bank active-precharge; 2 devices in deep power-down. Conditions for operating devices are: t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; t <sub>RC</sub> = t <sub>RC</sub> (MIN); CKE is HIGH; CS <sub>n</sub> is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD02</sub>	V <sub>DD2</sub>	62	60	60		
I <sub>DD0,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12	12		
I <sub>DD2P1</sub>	V <sub>DD1</sub>	1.6	1.6	1.6	mA	All devices in idle power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is LOW; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD2P2</sub>	V <sub>DD2</sub>	3.6	3.6	3.6		
I <sub>DD2P,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.4	0.4	0.4		
I <sub>DD2PS1</sub>	V <sub>DD1</sub>	1.6	1.6	1.6	mA	All devices in idle power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD2PS2</sub>	V <sub>DD2</sub>	3.6	3.6	3.6		
I <sub>DD2PS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.4	0.4	0.4		
I <sub>DD2N1</sub>	V <sub>DD1</sub>	1.6	1.6	1.6	mA	All devices in idle non power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is HIGH; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD2N2</sub>	V <sub>DD2</sub>	48	46	44		
I <sub>DD2N,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	24	24	24		
I <sub>DD2NS1</sub>	V <sub>DD1</sub>	1.6	1.6	1.6	mA	All devices in idle non power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is HIGH; CS <sub>n</sub> is HIGH; All banks are idle; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD2NS2</sub>	V <sub>DD2</sub>	38	38	38		
I <sub>DD2NS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	24	24	24		
I <sub>DD3P1</sub>	V <sub>DD1</sub>	2.8	2.8	2.8	mA	All devices in active power-down standby current t <sub>CK</sub> = t <sub>CK</sub> (avg) MIN; CKE is LOW; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD3P2</sub>	V <sub>DD2</sub>	20	20	20		
I <sub>DD3P,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.4	0.4	0.4		
I <sub>DD3PS1</sub>	V <sub>DD1</sub>	2.8	2.8	2.8	mA	All devices in active power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD3PS2</sub>	V <sub>DD2</sub>	20	20	20		
I <sub>DD3PS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	0.4	0.4	0.4		



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## I<sub>DD</sub> Specifications – Quad Die, Dual Channel

**Table 9: I<sub>DD</sub> Specifications (Continued)**
 $V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}; T_C = -30^\circ\text{C to } +85^\circ\text{C}$ 

Symbol	Supply	Speed			Unit	Parameter/Condition
		1866	1600	1333		
I <sub>DD3N1</sub>	V <sub>DD1</sub>	4.0	4.0	4.0	mA	All devices in active non power-down standby current t <sub>CK</sub> = t <sub>CK(avg)</sub> MIN; CKE is HIGH; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD3N2</sub>	V <sub>DD2</sub>	52	50	48		
I <sub>DD3N,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	24	24	24		
I <sub>DD3NS1</sub>	V <sub>DD1</sub>	4.0	4.0	4.0	mA	All devices in active non power-down standby current with clock stop CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is HIGH; CS <sub>n</sub> is HIGH; One bank is active; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD3NS2</sub>	V <sub>DD2</sub>	42	42	42		
I <sub>DD3NS,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	24	24	24		
I <sub>DD4R1</sub>	V <sub>DD1</sub>	4.0	4.0	4.0	mA	2 devices in operating burst read; 2 devices in deep power-down. Conditions for operating devices are: t <sub>CK</sub> = t <sub>CK(avg)</sub> MIN; CS <sub>n</sub> is HIGH between valid commands; One bank is active; BL = 8; RL = RL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I <sub>DD4R2</sub>	V <sub>DD2</sub>	460	400	350		
I <sub>DD4R,in</sub>	V <sub>DDCA</sub>	12	12	12		
I <sub>DD4W1</sub>	V <sub>DD1</sub>	4.0	4.0	4.0	mA	2 devices in operating burst write; 2 devices in deep power-down Conditions for operating devices are: t <sub>CK</sub> = t <sub>CK(avg)</sub> MIN; CS <sub>n</sub> is HIGH between valid commands; One bank is active; BL = 8; WL = WL (MIN); CA bus inputs are SWITCHING; 50% data change occurs at each burst transfer
I <sub>DD4W2</sub>	V <sub>DD2</sub>	440	380	330		
I <sub>DD4W,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12	12		
I <sub>DD51</sub>	V <sub>DD1</sub>	40	40	40	mA	2 devices in all bank auto-refresh; 2 devices in deep power-down. Conditions for operating devices are: t <sub>CK</sub> = t <sub>CK(avg)</sub> MIN; CKE is HIGH between valid commands; t <sub>RC</sub> = t <sub>RFCab</sub> (MIN); Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD52</sub>	V <sub>DD2</sub>	200	200	200		
I <sub>DD5,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12	12		
I <sub>DD5AB1</sub>	V <sub>DD1</sub>	4.0	4.0	4.0	mA	2 devices in all bank auto-refresh; 2 devices in deep power-down. Conditions for operating devices are: t <sub>CK</sub> = t <sub>CK(avg)</sub> MIN; CKE is HIGH between valid commands; t <sub>RC</sub> = t <sub>REFI</sub> ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD5AB2</sub>	V <sub>DD2</sub>	25	24	23		
I <sub>DD5AB,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12	12		



# 8Gb, 16Gb: 216-Ball, Dual-Channel Embedded LPDDR3 SDRAM I<sub>DD</sub> Specifications – Quad Die, Dual Channel

**Table 9: I<sub>DD</sub> Specifications (Continued)**
 $V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}; T_C = -30^\circ\text{C to } +85^\circ\text{C}$ 

Symbol	Supply	Speed			Unit	Parameter/Condition
		1866	1600	1333		
I <sub>DD5PB1</sub>	V <sub>DD1</sub>	4.0	4.0	4.0	mA	2 devices in per bank auto-refresh; 2 devices in deep power-down. Conditions for operating devices are: t <sub>CK</sub> = t <sub>CK(avg)</sub> MIN; CKE is HIGH between valid commands; t <sub>RC</sub> = t <sub>REFIpb</sub> ; CA bus inputs are SWITCHING; Data bus inputs are STABLE
I <sub>DD5PB2</sub>	V <sub>DD2</sub>	25	24	23		
I <sub>DD5PB,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	12	12	12		
I <sub>DD81</sub>	V <sub>DD1</sub>	64	64	64	μA	All devices in deep power-down CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
I <sub>DD82</sub>	V <sub>DD2</sub>	24	24	24		
I <sub>DD8,in</sub>	V <sub>DDCA</sub> + V <sub>DDQ</sub>	48	48	48		

- Notes: 1. Published I<sub>DD</sub> values are the maximum of the distribution of the arithmetic mean.  
2. I<sub>DD</sub> current specifications are tested after the device is properly initialized.

**Table 10: I<sub>DD6</sub> Partial-Array Self Refresh Current at 45°C**
 $V_{DD2}, V_{DDQ}, V_{DDCA} = 1.14\text{--}1.30\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$ 

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V <sub>DD1</sub>	800	μA	<b>All devices in self refresh</b> CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V <sub>DD2</sub>	3200		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	40		
1/2 array	V <sub>DD1</sub>	640		
	V <sub>DD2</sub>	2000		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	40		
1/4 array	V <sub>DD1</sub>	520		
	V <sub>DD2</sub>	1200		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	40		
1/8 array	V <sub>DD1</sub>	480		
	V <sub>DD2</sub>	800		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	40		

- Note: 1. I<sub>DD6</sub> 45°C is typical of the distribution of the arithmetic mean.





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**Table 11: I<sub>DD6</sub> Partial-Array Self Refresh Current at 85°C**

V<sub>DD2</sub>, V<sub>DDQ</sub>, V<sub>DDCA</sub> = 1.14–1.30V; V<sub>DD1</sub> = 1.70–1.95V

PASR	Supply	Value	Unit	Parameters/Conditions
Full array	V <sub>DD1</sub>	3600	μA	<b>All devices in self refresh</b> CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
	V <sub>DD2</sub>	12,800		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	48		
1/2 array	V <sub>DD1</sub>	2600		
	V <sub>DD2</sub>	8800		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	48		
1/4 array	V <sub>DD1</sub>	2200		
	V <sub>DD2</sub>	6800		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	48		
1/8 array	V <sub>DD1</sub>	2000		
	V <sub>DD2</sub>	5600		
	V <sub>DDCA</sub> + V <sub>DDQ</sub>	48		

Note: 1. I<sub>DD6</sub> 85°C is the maximum of the distribution of the arithmetic mean.