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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

DDR4 SDRAM

EDY4016A - 256Mb x 16

Features

- $V_{DD} = V_{DDQ} = 1.2V \pm 60mV$
- $V_{PP} = 2.5V, -125mV/+250mV$
- On-die, internal, adjustable V_{REFDQ} generation
- 1.2V pseudo open-drain I/O
- T_C of 0°C to 95°C
 - 64ms, 8192-cycle refresh at 0°C to 85°C
 - 32ms at 85°C to 95°C
- 8 internal banks: 2 groups of 4 banks each
- 8n-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity

- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test
- JEDEC JESD-79-4 compliant

Options¹

- | Options¹ | Marking |
|---|----------------|
| • Revision | A |
| • FBGA package size | |
| – 96-ball (7.5mm x 13.5mm) | BG |
| • Timing – cycle time | |
| – 0.625ns @ CL = 24 (DDR4-3200) | -JD |
| – 0.750ns @ CL = 19 (DDR4-2666) | -GX |
| – 0.833ns @ CL = 16 (DDR4-2400) | -DR |
| • Packaging | |
| – Lead-free (RoHS-compliant) and halogen-free | - F |

Notes:

1. Not all options listed can be combined to define an offered product. Use the part catalog search on <http://www.micron.com> for available offerings.
2. Restricted and limited availability.

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target tRCD-tRP-CL	tRCD (ns)	tRP (ns)	CL (ns)
-JD ¹	3200	24-24-24	15.0	15.0	15.0
-GX ²	2666	19-19-19	14.25	14.25	14.25
-DR ³	2400	16-16-16	13.32	13.32	13.32

Notes:

1. Backward compatible to 2666 CL = 20, 2400 CL = 18), 2133 CL = 16, 1866 CL = 14, 1600 CL = 12.
2. Backward compatible to 2400 CL = 17, 2133 CL = 15, 1866 CL = 13, 1600 CL = 11.
3. Backward compatible to 2133 CL = 15, 1866 CL = 13, 1600 CL = 11.

Table 2: Addressing

Parameter	256 Meg x 16
Number of bank groups	2
Bank group address	BG0

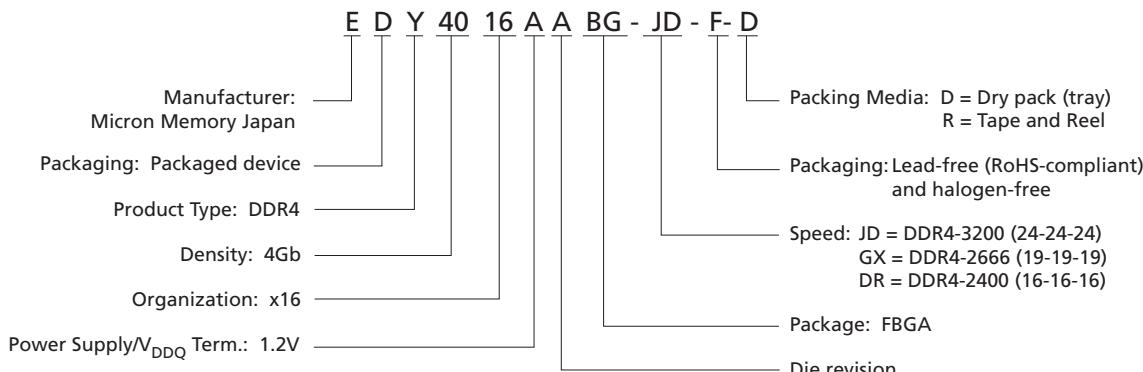
Table 2: Addressing (Continued)

Parameter	256 Meg x 16
Bank count per group	4
Bank address in bank group	BA[1:0]
Row addressing	32K (A[14:0])
Column addressing	1K (A[9:0])
Page size ¹	2KB

Note: 1. Page size is per bank, calculated as follows:

Page size = $2^{\text{COLBITS}} \times \text{ORG}/8$, where COLBIT = the number of column address bits and ORG = the number of DQ bits.

Micron Memory Japan DDR4 Part Numbering

Figure 1: 4Gb DDR4 Part Numbers


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General Notes and Description

Description

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM for the x16 configuration and as a 16-bank DRAM for the x4 and x8 configurations. The DDR4 SDRAM uses an $8n$ -prefetch architecture to achieve high-speed operation. The $8n$ -prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins.

A single READ or WRITE operation for the DDR4 SDRAM consists of a single $8n$ -bit wide, four-clock data transfer at the internal DRAM core and two corresponding n -bit wide, one-half-clock-cycle data transfers at the I/O pins.

Industrial Temperature

An industrial temperature (IT) device option requires that the case temperature not exceed below -40°C or above 95°C . JEDEC specifications require the refresh rate to double when T_C exceeds 85°C ; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when operating outside of the commercial temperature range, when T_C is between -40°C and 0°C .

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enable mode of operation (normal operation), unless specifically stated otherwise.
- Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms " $_t$ " and " $_c$ " are used to represent the true and complement of a differential signal pair. These terms replace the previously used notation of "#" and/or overbar characters. For example, differential data strobe pair DQS, DQS# is now referred to as DQS $_t$, DQS $_c$.
- The term " $_n$ " is used to represent a signal that is active LOW and replaces the previously used "#" and/or overbar characters. For example: CS# is now referred to as CS $_n$.
- The terms "DQS" and "CK" found throughout the data sheet are to be interpreted as DQS $_t$, DQS $_c$ and CK $_t$, CK $_c$ respectively, unless specifically stated otherwise.
- Complete functionality may be described throughout the entire document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.
- Any functionality not specifically stated here within is considered undefined, illegal, and not supported, and can result in unknown operation.
- Addressing is denoted as BG[n] for bank group, BA[n] for bank address, and A[n] for row/col address.
- The NOP command is not allowed, except when exiting maximum power savings mode or when entering gear-down mode, and only a DES command should be used.

- Not all features described within this document may be available on the Rev. A (first) version.
- Not all specifications listed are finalized industry standards; best conservative estimates have been provided when an industry standard has not been finalized.
- Although it is implied throughout the specification, the DRAM must be used after V_{DD} has reached the stable power-on level, which is achieved by toggling CKE at least once every $8192 \times t_{REFI}$. However, in the event CKE is fixed HIGH, toggling CS_n at least once every $8192 \times t_{REFI}$ is an acceptable alternative. Placing the DRAM into self refresh mode also alleviates the need to toggle CKE.
- Not all features designated in the data sheet may be supported by earlier die revisions due to late definition by JEDEC.

Definitions of the Device-Pin Signal Level

- HIGH: A device pin is driving the logic 1 state.
- LOW: A device pin is driving the logic 0 state.
- High-Z: A device pin is tri-state.
- ODT: A device pin terminates with the ODT setting, which could be terminating or tri-state depending on the mode register setting.

Definitions of the Bus Signal Level

- HIGH: One device on the bus is HIGH, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally V_{DDQ}.
- LOW: One device on the bus is LOW, and all other devices on the bus are either ODT or High-Z. The voltage level on the bus is nominally V_{OL(DC)} if ODT was enabled, or V_{SSQ} if High-Z.
- High-Z: All devices on the bus are High-Z. The voltage level on the bus is undefined as the bus is floating.
- ODT: At least one device on the bus is ODT, and all others are High-Z. The voltage level on the bus is nominally V_{DDQ}.

Ball Assignments

Figure 2: 96-Ball x16 Ball Assignments

	1	2	3	4	5	6	7	8	9	
A			DQ8				UDQS_c	VSSQ	VDDQ	A
B	VDDQ	VSSQ					UDQS_t	DQ9	VDD	B
C	VPP	VSS	VDD							C
D	VDDQ	DQ12	DQ10				DQ11	DQ13	VSSQ	D
E	VDD	VSSQ	DQ14				DQ15	VSSQ	VDDQ	E
F	VSS	NF/LDM_n/ UDBL_n	VSSQ				NF/LDM_n/ LDBL_n	VSSQ	VSS	F
G	VSSQ	VDDQ	LDQS_c				DQ1	VDDQ	ZQ	G
H	VDDQ	DQ0	LDQS_t				VDD	VSS	VDDQ	H
J	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	J
K	VDD	VDDQ	DQ6				DQ7	VDDQ	VDD	K
L	VSS	CKE	ODT				CK_t	CK_c	VSS	L
M	VDD	WE_n/A14	ACT_n				CS_n	RAS_n/A16	VDD	M
N	VREFCA	BG0	A10/AP				A12/BC_n	CAS-n/A15	VSS	N
P	VSS	BA0	A4				A3	BA1	TEN	P
R	RESET_n	A6	A0				A1	A5	ALERT_n	R
T	VDD	A8	A2				A9	A7	VPP	T
	VSS	A11	PAR				NC	A13	VDD	

- Notes:
1. See Ball Descriptions.
 2. A slash "/" defines a selectable function. For example: Ball E7 = NF/LDM_n. If data mask is enabled via the MRS, ball E7 = LDM_n. If data mask is disabled in the MRS, E7 = NF (no function).
 3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).

Ball Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 devices. All pins listed may not be supported on the device defined in this data sheet. See the Ball Assignments section to review all pins used on this device.

Table 3: Ball Descriptions

Symbol	Type	Description
A[17:0]	Input	Address inputs: Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, RAS_n/A16 have additional functions, see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts, and A17 is only used on some 16Gb parts.
A10/AP	Input	Auto precharge: A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	Burst chop: A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst chop-ped). See the Command Truth Table.
ACT_n	Input	Command input: ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
BA[1:0]	Input	Bank address inputs: Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
BG[1:0]	Input	Bank group address inputs: Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. BG1 is not used in the x16 configuration.
C0/CKE1, C1/CS1_n, C2/ODT1	Input	Stack address inputs: These inputs are used only when devices are stacked; that is, they are used in 2H, 4H, and 8H stacks for x4 and x8 configurations (these pins are not used in the x16 configuration). DDR4 will support a traditional DDP package, which uses these three signals for control of the second die (CS1_n, CKE1, ODT1). DDR4 is not expected to support a traditional QDP package. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave) type of configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT signal.
CK_t, CK_c	Input	Clock: Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.

Table 3: Ball Descriptions (Continued)

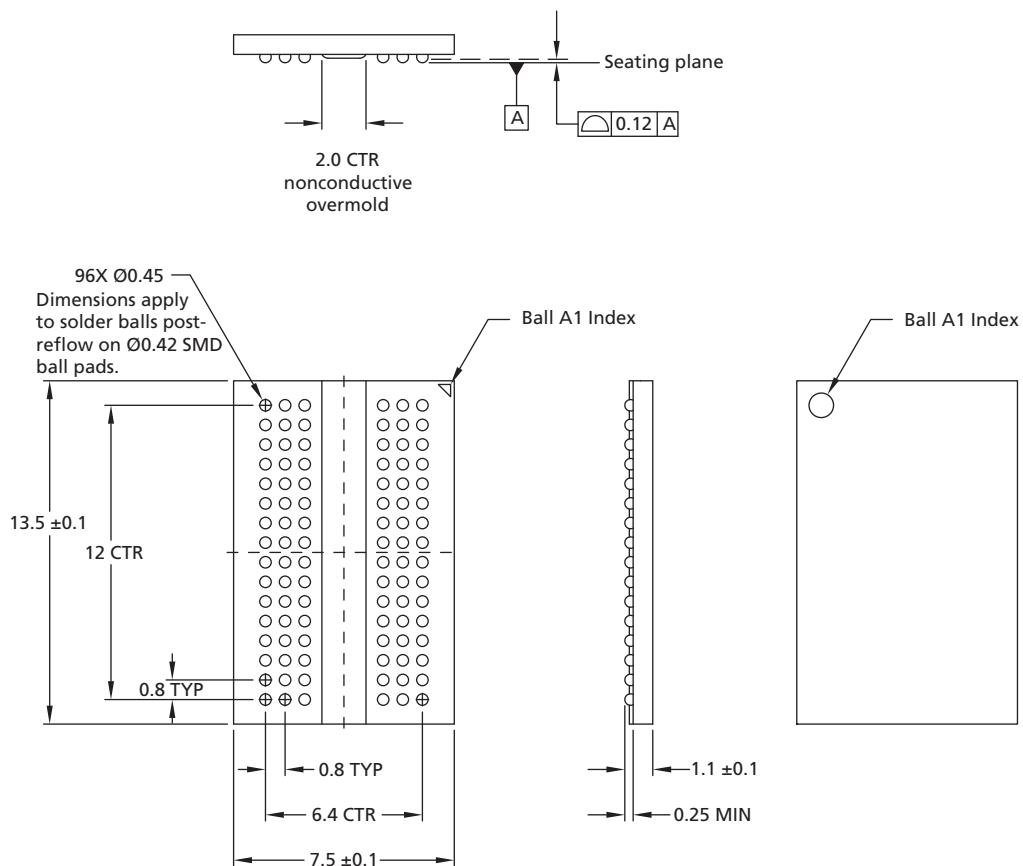
Symbol	Type	Description
CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CS_n	Input	Chip select: All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
DM_n, UDM_n LDM_n	Input	Input data mask: DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS. DM is not supported on x4 configurations. The UDM_n and LDM_n pins are used in the x16 configuration: UDM_n is associated with DQ[15:8]; LDM_n is associated with DQ[7:0]. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Mask section.
ODT	Input	On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for the x4 and x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQL_t, DQL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT} .
PAR	Input	Parity for command and address: This function can be enabled or disabled via the mode register. When enabled, the parity signal covers all command and address inputs, including ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, A[17:0], A10/AP, A12/BC_n, BA[1:0], and BG[1:0] with C0, C1, and C2 on 3DS only devices. Control pins NOT covered by the parity signal are CS_n, CKE, and ODT. Unused address pins that are density- and configuration-specific should be treated internally as 0s by the DRAM parity logic. Command and address inputs will have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n and ACT_n) define the command and/or address being entered. See the ACT_n description in this table.
RESET_n	Input	Active LOW asynchronous reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD} (960 mV for DC HIGH and 240 mV for DC LOW).
TEN	Input	Connectivity test mode: TEN is active when HIGH and inactive when LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DD} (960mV for DC HIGH and 240mV for DC LOW).

Table 3: Ball Descriptions (Continued)

Symbol	Type	Description
DQ	I/O	Data input/output: Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If write CRC is enabled via mode register, the write CRC code is added at the end of data burst. Any one or all of DQ0, DQ1, DQ2, and DQ3 may be used to monitor the internal V _{REF} level during test via mode register setting MR[4] A[4] = HIGH, training times change when enabled. During this mode, the R _{TT} value should be set to High-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DBI_n, UDBI_n, LDBI_n	I/O	DBI input/output: Data bus inversion. DBI_n is an input/output signal used for data bus inversion in the x8 configuration. UDBI_n and LDBI_n are used in the x16 configuration; UDBI_n is associated with DQ[15:8], and LDBI_n is associated with DQ[7:0]. The DBI feature is not supported on the x4 configuration. DBI can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Bus Inversion section.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	I/O	Data strobe: Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, DQSL corresponds to the data on DQ[7:0]; DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	Alert output: This signal allows the DRAM to indicate to the system's memory controller that a specific alert or event has occurred. Alerts will include the command/address parity error and the CRC data error when either of these functions is enabled in the mode register.
TDQS_t, TDQS_c	Output	Termination data strobe: TDQS_t and TDQS_c are used by x8 DRAMs only. When enabled via the mode register, the DRAM will enable the same R _{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin will provide the DATA MASK (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations.
V _{DD}	Supply	Power supply: 1.2V ±0.060V.
V _{DDQ}	Supply	DQ power supply: 1.2V ±0.060V.
V _{PP}	Supply	DRAM activating power supply: 2.5V –0.125V/+0.250V.
V _{REFCA}	Supply	Reference voltage for control, command, and address pins.
V _{SS}	Supply	Ground.
V _{SSQ}	Supply	DQ ground.
ZQ	Reference	Reference ball for ZQ calibration: This ball is tied to an external 240Ω resistor (RZQ), which is tied to V _{SSQ} .
RFU	–	Reserved for future use.
NC	–	No connect: No internal electrical connection is present.
NF	–	No function: May have internal connection present but has no function.

Package Dimensions

Figure 3: 96-Ball FBGA – x16



- Notes:
1. All dimensions are in millimeters.
 2. Solder ball material: SAC302 (Pb-free 96.8% Sn, 3% Ag, 0.2% Cu).

State Diagram

This simplified state diagram provides an overview of the possible state transitions and the commands to control them. Situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

Figure 4: Simplified State Diagram



Table 4: State Diagram Command Definitions

Command	Description
ACT	Active
MPR	Multipurpose register
MRS	Mode register set
PDE	Enter power-down
PDX	Exit power-down
PRE	Precharge
PREA	Precharge all
READ	RD, RDS4, RDS8
READ A	RDA, RDAS4, RDAS8
REF	Refresh, fine granularity refresh
RESET	Start reset procedure
SRE	Self refresh entry
SRX	Self refresh exit
TEN	Boundary scan mode enable
WRITE	WR, WRS4, WRS8 with/without CRC
WRITE A	WRA, WRAS4, WRAS8 with/without CRC
ZQCL	ZQ calibration long
ZQCS	ZQ calibration short

Note: 1. See the Command Truth Table for more details.