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LogiCORE IP 10-Gigabit Ethernet PCS/PMA v2.3

DS739 April 24, 2012 **Product Specification**

Introduction

The LogiCORE™ IP 10-Gigabit Ethernet Physical Coding Sublayer/Physical Medium Attachment (PCS/PMA) core forms a seamless interface between the Xilinx® 10-Gigabit Ethernet Media Access Controller (MAC) and a 10 Gb/s-capable PHY, enabling the design of high-speed Ethernet systems and subsystems.

10GBASE-KR and 10GBASE-R are supported on Virtex®-7 and Kintex™-7 devices on GTH and GTX transceivers. Xilinx also supports an integrated 10GBASE-R IP on Virtex-6 HXT devices.

Features

- Designed to 10-Gigabit Ethernet specification *IEEE 802.3-2008 clause 49, 72, 73, 74*
- Optional Management Data Interface (MDIO) interface to manage PCS/PMA registers according to specification *IEEE 802.3-2008 clause 45*
- Delivered through the Xilinx CORE Generator™ tool
- Supports 10GBASE-SR, -LR and -ER optical links in Virtex-7, Kintex-7 and Virtex-6 devices (LAN mode only)
- Supports 10GBASE-KR backplane links in Kintex-7/Virtex-7, including Auto-Negotiation (AN), Training and Forward Error Correction (FEC).
- SDR 10-Gigabit Ethernet Media Independent Interface (XGMII) connects seamlessly to the Xilinx 10G Ethernet MAC

LogiCORE IP Facts			
Core Specifics			
Supported Device Family (1)	Virtex-7/Kintex-7(2) Virtex-6 HXT		
Supported User Interfaces	XGMII		
Resources Used			
Device	**LUTs**	**FFs**	**Block RAMs**
Virtex-7/Kintex-7	3318-8191	3494-6200	3
Virtex-6	687-877	770-1019	0
Provided with Core			
Design Files	Native Generic Circuit (NGC) netlist		
Example Design	VHDL, Verilog		
Test Bench	VHDL, Verilog		
Constraints File	User Constraints File (UCF)		
Verification	VHDL, Verilog Test Bench		
Instantiation Template	VHDL, Verilog Wrapper		
Simulation Model	Verilog or VHDL Structural Model		
Supported S/W Drivers	N/A		
Tested Design Tools			
Design Entry Tools	Integrated Software Environment (ISE) Design Suite v14.1		
Simulation(3)	Mentor Graphics ModelSim Cadence Incisive Enterprise Simulator (IES) Synopsys VCS and VCS MX		
Synthesis Tools	XST v14.1		
Support			
Provided by Xilinx, Inc.			

1. 10GBASE-R is pre-production status for Virtex-7/Kintex-7 and Production for Virtex-6 FPGAs. This IP was verified in software using pre-production speed files. For the complete list of supported devices, see the 14.1 release notes for this core.
2. -2 or -3 speed grades
3. For the supported versions of the tools, see the ISE Design Suite 14: Release Notes Guide.

Applications

Figure 1 shows a typical Ethernet system architecture and the 10-Gigabit Ethernet PCS/PMA core within it. The MAC and all the blocks to the right are defined in Ethernet IEEE specifications [Ref 1][Ref 2].

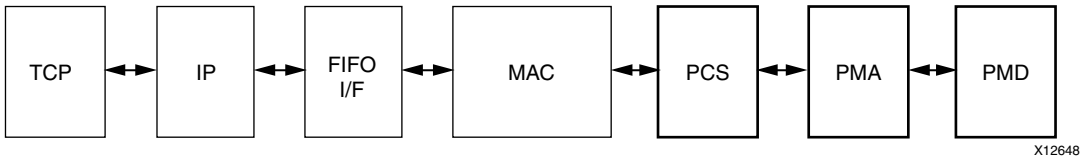

Figure 1: **Typical Ethernet System Architecture**

Figure 2 shows the 10-Gigabit Ethernet PCS/PMA core connected on one side to a 10-Gigabit MAC and on the other to an optical module (BASE-R) or backplane (BASE-KR) using a serial interface. The optional WAN Interface Sublayer (WIS) part of the 10GBASE-R standard is not implemented in this core.

The 10-Gigabit Ethernet PCS/PMA core is designed to be attached to the Xilinx IP 10-Gigabit Ethernet MAC core over XGMII.

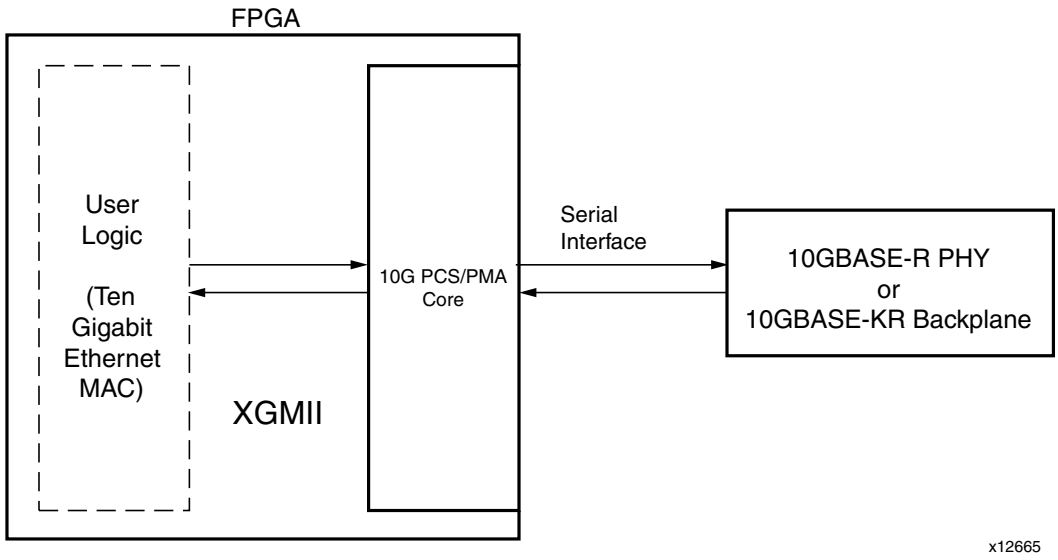

Figure 2: **Core Connected to MAC Core Using XGMII Interface**

Functional Overview

10GBASE-R

Figure 3 illustrates a block diagram of the 10-Gigabit Ethernet PCS/PMA (BASE-R) core implementation on Virtex-6 devices. As you can see, in Virtex-6 devices, most of the functionality is contained within the GTH transceiver.

For Virtex-7/Kintex-7 devices, all of the PCS and Management blocks illustrated are implemented in logic, except for part of the Gearbox and SERDES.

The major functional blocks of the core include the following:

- XGMII interface, designed for simple attachment of 10-Gigabit Ethernet MAC
- Transmit path, including Scrambler, 64B/66b Encoder and Gearbox
- Receive path, including Block Synchronization, Descrambler, Decoder and BER (Bit Error Rate) monitor
- Test Pattern Generation and Checking
- Serial interface to optics
- Management registers (PCS/PMA) with optional MDIO interface

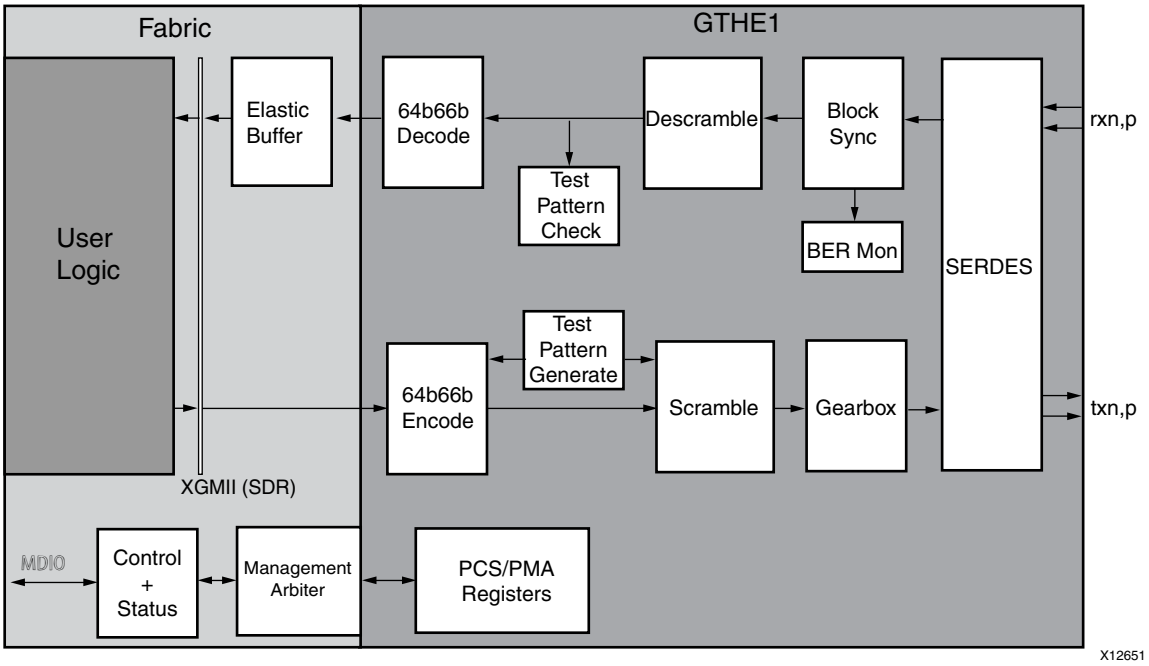

Figure 3: **Virtex-6 Implementation of the BASE-R Core**

10GBASE-KR

Figure 4 illustrates a block diagram of the 10-Gigabit Ethernet PCS/PMA (BASE-KR) core implementation. The major functional blocks of the core include the following:

- XGMII interface, designed for simple attachment of 10-Gigabit Ethernet MAC
- Transmit path, including Scrambler, 64B/66B Encoder, FEC, AN and Training
- Receive path, including Block Synchronization, Descrambler, Decoder and BER (Bit Error Rate) monitor, FEC, AN and Training
- Test Pattern Generation and Checking
- Serial interface to backplane connector
- Management registers (PCS/PMA) with optional MDIO interface

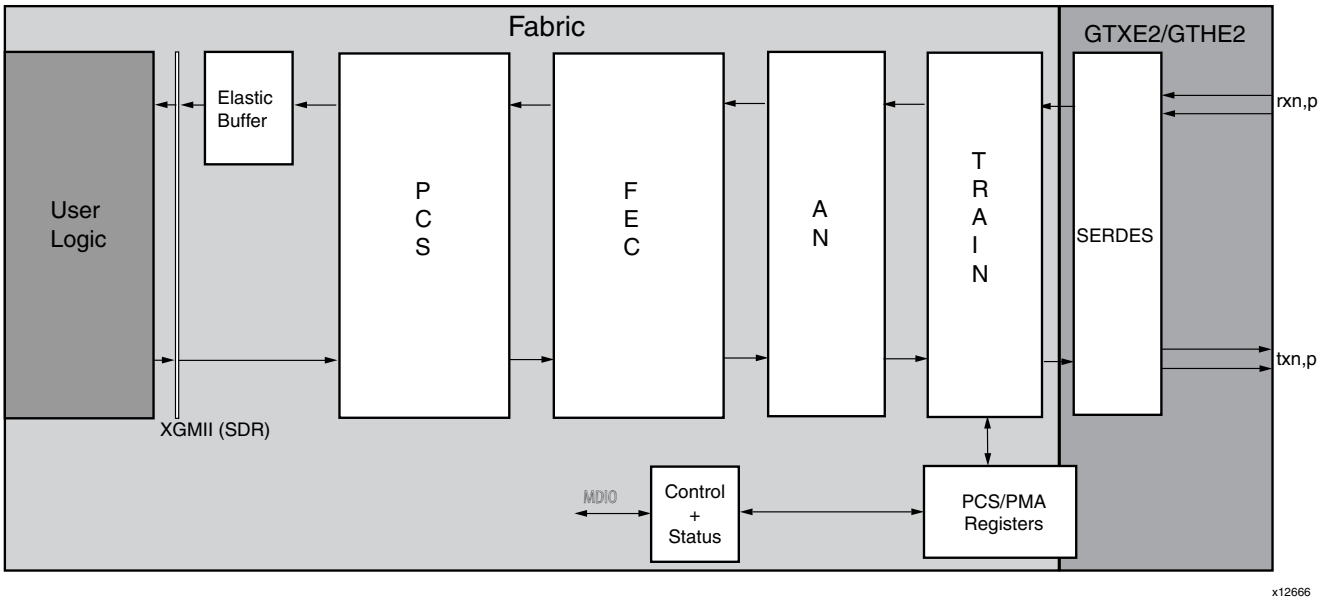

Figure 4: **Virtex-7/Kintex-7 Implementation of the BASE-KR Core**

Core Interfaces

MAC-Side Interface: XGMII

The MAC (or client) side of the core has a 64-bit datapath plus 8 control bits implementing an XGMII interface. Table 1 defines the signals, which are all synchronous to the 156.25 MHz core clock. It is designed to be connected to either user logic within the FPGA or, by using SelectIO™ technology Double Data Rate (DDR) registers in the user's own design top-level, to provide an external 32-bit 312 Mb/s DDR XGMII, defined in clause 46 of *IEEE 802.3-2008*.

Table 1: **MAC-Side Interface Ports**

Signal Name	Direction	Description
xgmii_txd[63:0]	In	64-bit transmit data word
xgmii_txc[7:0]	In	8-bit transmit control word
xgmii_rxd[63:0]	Out	64-bit receive data word
xgmii_rxc[7:0]	Out	8-bit receive control word

Figure 5 illustrates transmitting a frame through the client-side interface.

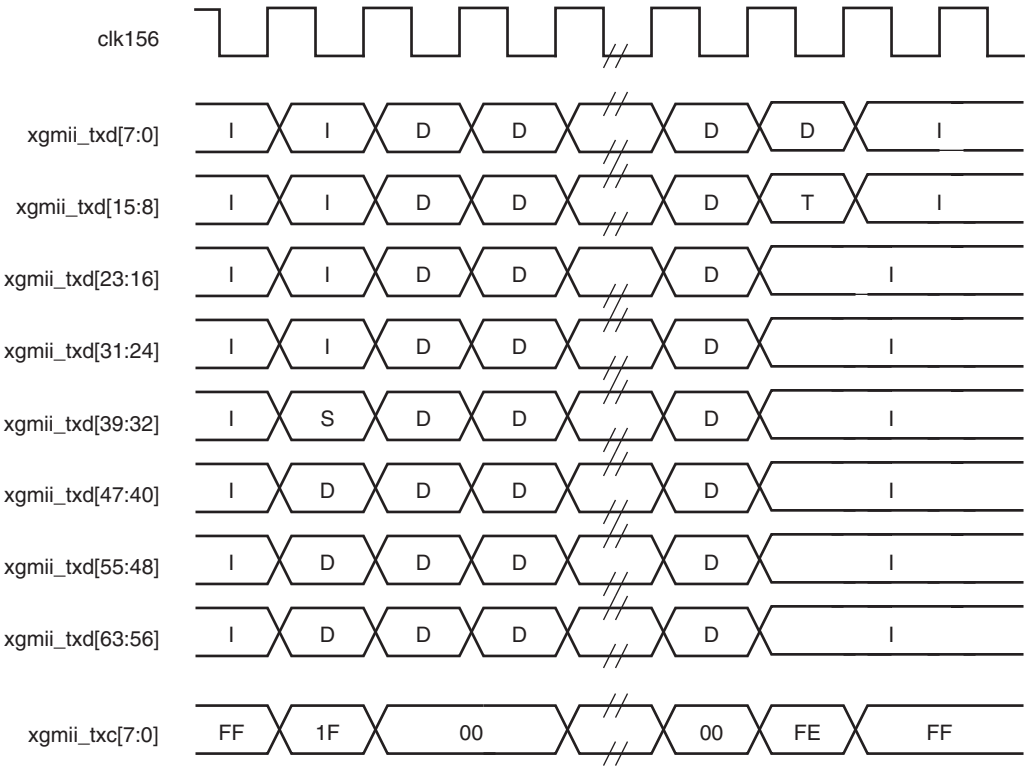

Figure 5: **Transmitting a Frame Through the Client-Side Interface**

Figure 6 illustrates receiving a frame through the client-side interface.

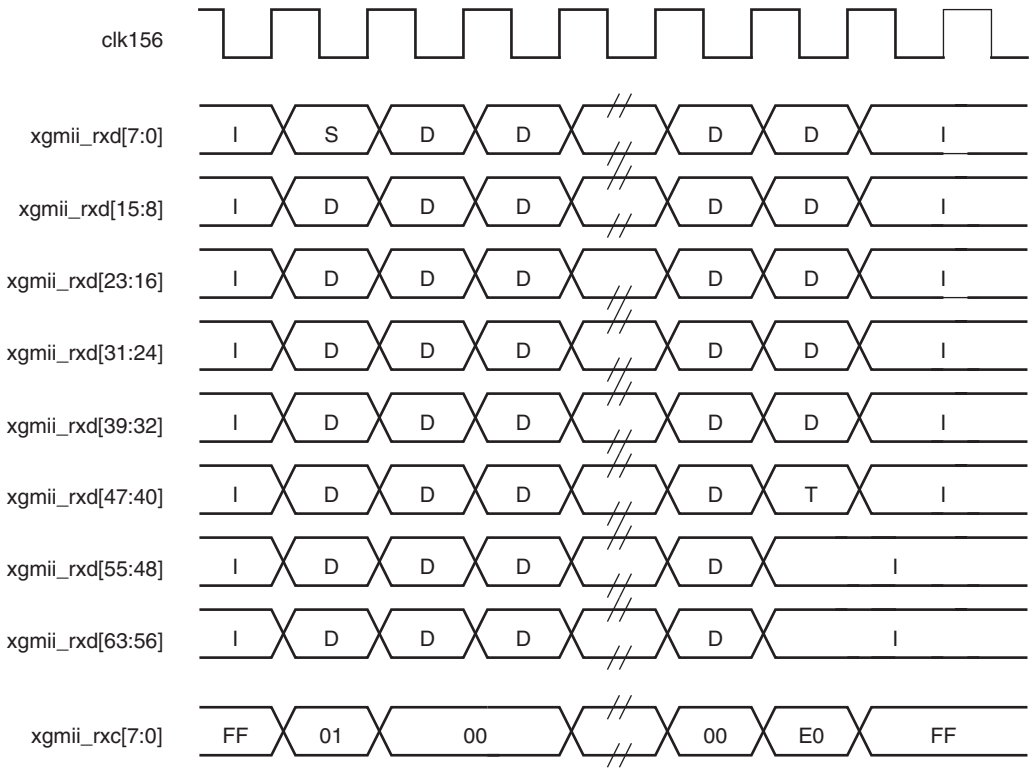

Figure 6: **Receiving a Frame Through the Client-Side Interface**

Transceiver Interface

The following tables describe the signals which connect the core to the transceiver. For Virtex-7/Kintex-7 FPGAs, the mapping of transceiver signals is not one-to-one.

Table 2: **Transceiver-Side Interface Port Description - Virtex-6 10GBASE-R**

Signal Name	Direction	Description
gt_txd[63:0]	Out	64-bit transmit data word
gt_txc[7:0]	Out	8-bit transmit control word
gt_rxd[63:0]	In	64-bit receive data word
gt_rxc[7:0]	In	8-bit receive control word

Table 3: **Transceiver-Side Interface Port Description - Virtex-7/Kintex-7**

Signal Name	Direction	Description
gt_txd[31:0]	Out	32-bit transmit data word
gt_txc[1:0]	Out	2-bit transmit sync header
gt_txc[7:2]	Out	6-bit txsequence count (0..32)
gt_rxd[31:0]	In	32-bit receive data word
gt_rxc[1:0]	In	2-bit receive sync header
gt_rxc[2]	In	RXDATAVALID (high for 64 in 66 rxusrclk2 cycles)
gt_rxc[3]	In	RXHEADERVALID (high on alternate cycles of rxusrclk2, while RXDATAVALID is high)
gt_rxc[7:4]	In	Not Used
gt_slip	Out	Slip control for serial transceiver gearbox

Management Interface (MDIO)

The optional MDIO interface is a simple low-speed two-wire interface for management of the 10-Gigabit Ethernet PCS/PMA core, consisting of a clock signal and a bidirectional data signal. The interface is defined in clause 45 of the *IEEE 802.3-2008* standard.

In this core, the MDIO interface is an optional block. If implemented, the bidirectional data signal MDIO is implemented as three unidirectional signals. These can be used to drive a 3-state buffer either in the FPGA IOB or in a separate device.

For the BASE-R core in Virtex-6 FPGAs, the register in the GTHE1 is pre-read as soon as the address phase of the MDIO transfer is complete and this data is provided back to the MDIO interface on completion of the READ phase of the MDIO transfer.

Table 4: **MDIO Management Interface Ports**

Signal Name	Direction	Description
mdc	In	Management clock
mdio_in	In	MDIO Input
mdio_out	Out	MDIO Output
mdio_tri	Out	MDIO 3-state control. "1" disconnects the output driver from the MDIO bus.
prtad[4:0]	In	MDIO port address. When multiple MDIO-managed ports appear on the same bus, this address can be used to address each port individually.

GTHE1 Management Interface Ports

There is a management interface on the GTHE1 transceiver which connects to the associated ports on the core, through an arbiter block provided with the core.

Table 5: **GTHE1 Management Interface Ports**

Signal Name	Direction	Description
mgmt_req	Out	Request access to the MGMT interface on the GTHE1
mgmt_gnt	In	Access granted to the MGMT interface on the GTHE1
mgmt_rd_out	Out	Read enable
mgmt_wr_out	Out	Write enable
mgmt_addr_out[20:0]	Out	Address
mgmt_rdack_in	In	Read Acknowledge
mgmt_rddata_in[15:0]	In	Read data
mgmt_wrdata_out[15:0]	In	Write data

GTXE2/GTHE2 DRP Interface Ports

There is a DRP interface on the GTXE2/GTHE2 transceivers which connect to the associated ports on the core, perhaps through an arbiter block (not provided with the core).

Table 6: **GTXE2/GTHE2 DRP Interface Ports**

Signal Name	Direction	Description
drp_req(1)	Out	Request access to the DRP interface on the GTXE2/GTHE2
drp_gnt	In	Access granted to the DRP interface on the GTXE2/GTHE2
drp_den	Out	DRP enable
drp_dwe	Out	Write enable
drp_daddr[15:0]	Out	Address
drp_di[15:0]	In	Write data
drp_drdy	In	Read data ready/Write complete
drp_drpdo[15:0]	In	Read data

1. Can be wired directly to drp_gnt if this is the only block requiring access to the DRP interface.

Configuration and Status Signals

As an alternative to the MDIO interface, vector-based interfaces can be provided to allow control and status to flow to and from the core. Table 7 describes these two vectors. Neither vector is completely populated so the actual number of pins required is much lower than the maximum widths of the vectors. For the status vector, correct default values are provided for all bits in the associated IEEE registers.

Table 7: **Configuration and Status Vectors**

Signal Name	Direction	Description
configuration_vector[535:0]	In	Configures the PCS/PMA registers
status_vector[447:0]	Out	Reflects *recent* status of PCS/PMA registers

Clock, Reset and Miscellaneous Signals

The various clocks, resets and other ports on the core are described in Table 8.

Table 8: **Clock, Reset and Miscellaneous Signals**

Signal Name	Direction	Description
dclk_reset	In	Sync reset in dclk domain (1)
reset	In	Synchronous reset signal in clk156 domain
txreset322	In	Sync reset in txusrclk2 domain (1)
rxreset322	In	Sync reset in rxusrclk2 domain (1)
dclk	In	Management clock
clk156	In	Core clock - User should use this in their own logic
rxclk156	In	Receive path clock - Derived from recovered clock (4)
rxusrclk2	In	Receive path clock - Derived from recovered clock (1)
txusrclk2	In	Transmit path clock - Derived from TXCLKOUT (1)
signal_detect	In	Signal Detect indication from Optics (2) (3)
tx_fault	In	Tx Fault indication from Optics (2) (3)
tx_disable	Out	Disable the laser in Optics (3)
core_status[7:0]	Out	PCS Block lock in bit 0. (1) BASE-KR cores: FEC signal OK in bit 1, pmd_signal_detect (Training Done) in bit 2, AN Complete in bit 3. Other bits are reserved.
pma_pmd_type[2:0]	In	Set the PMA/PMD type for the core (1) (3)
is_eval	Out	Active-High signal which indicates if the core is a HW Eval core (5)
tx_prbs31_en	Out	Enable PRBS31 transmission in GTXE2/GTHE2 (1)
rx_prbs31_en	Out	Enable PRBS31 checking in GTXE2/GTHE2 (1)
clear_rx_prbs_err_count	Out	Clear PRBS error count in GTXE2/GTHE2 (1)
loopback_ctrl[2:0]	Out	Loopback control to GTXE2/GTHE2 (1)
resetdone	In	Reset Done indication from GTXE2/GTHE2 (1)

Table 8: **Clock, Reset and Miscellaneous Signals *(Cont'd)***

Signal Name	Direction	Description
an_enable	In	Enable Auto-Negotiation - Can be used to disable AN during simulation (5)
training_*	In	Training Algorithm Interface - see UG692 (5)

1. Not connected in Virtex-6 devices
2. These signals are not connected inside the core; the user should employ these signals where applicable, to reset the core. An example is given in the core example design.
3. BASE-R core only.
4. Virtex-6 devices only
5. BASE-KR only

Verification

The 10-Gigabit Ethernet PCS/PMA core has been verified using simulation. Check the core product page for more information.

Simulation

A highly parameterizable transaction-based simulation test suite was used to verify the core. Verification tests include:

- Register access over MDIO
- Loss and regain of synchronization
- Frame transmission
- Frame reception
- Clock compensation
- Recovery from error conditions
- BASE-KR-specific:
  - Auto-Negotiation
  - Training
  - FEC

Device Utilization

Virtex-7/Kintex-7 FPGAs

Table 9 provides approximate slice counts for the BASE-R options on Virtex-7/Kintex-7 FPGAs.

Table 9: **Device Utilization - BASE-R on Virtex-7/Kintex-7 FPGAs**

Parameter Values	Device Resources		
MDIO Interface	Slices	LUTs	FFs
No	952	2160	2281
Yes	1171	2736	2708

Table 10 provides the approximate slice counts for the BASE-KR options on Virtex-7/Kintex-7 FPGAs.

Table 10: **Device Utilization on Virtex-7/Kintex-7 FPGAs**

Parameter Values			Device Resources		
FEC	Auto-Negotiation	MDIO Interface	Slices	LUTs	FFs
No	No	No	1549	3318	3494
No	No	Yes	1709	3745	3734
No	Yes	No	1797	3815	4100
No	Yes	Yes	1972	4504	4517
Yes	No	No	2854	6899	5176
Yes	No	Yes	2886	7372	5446
Yes	Yes	No	3343	7465	5806
Yes	Yes	Yes	3443	8191	6200

Virtex-6 HXT FPGAs

Table 11 provides approximate slice counts for the two BASE-R core options on Virtex-6 HXT FPGAs.

Table 11: **Device Utilization - Virtex-6 HXT FPGAs**

Parameter Values	Device Resources		
MDIO Interface	Slices	LUTs	FFs
No	446	877	1019
Yes	296	687	770

References

1. *IEEE Std. 802.3-2008*, Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications
2. *IEEE Std. 802.3-2008*, Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10-Gb/s Operation

Support

Visit www.xilinx.com/support for technical support. Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation.

Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not listed in the documentation or if customized beyond that allowed in the product documentation, or if any changes are made in sections of the design marked *DO NOT MODIFY*.

Ordering Information

The core is provided under the Xilinx End User License Agreement and can be generated using CORE Generator tool v13.3 and higher. The CORE Generator tool is shipped with Xilinx ISE® Design Suite software.

The 10GBASE-KR IP with the optional FEC and Auto-Negotiation is provided under the Xilinx Core Project License Agreement. Included is a no-charge simulation only license for evaluation with the CORE Generator system. If you require a hardware timeout evaluation license, contact your Xilinx sales representative.

For full access to the 10GBASE-KR IP, both in simulation and hardware, you must purchase the 10GBASE-KR IP. After purchasing, go to the 10GBASE-KR product page for more information on generating the relevant license key for use with the Xilinx CORE Generator System v14.1.

The 10GBASE-R IP without FEC or Auto-Negotiation is available at no charge under the Xilinx End User License Agreement and can be generated using the Core Generator v14.1 tool and higher.

Contact your local Xilinx sales representative for pricing and availability of Xilinx LogiCORE IP modules and software. Information on additional LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

Date	Version	Revision
12/02/09	1.1	Initial Xilinx release.
04/19/10	1.2	Updated to core version 1.2; updated to Xilinx tools 12.1.
03/01/11	2.1	Updated to core version 2.1; updated to Xilinx tools 13.1.
10/19/11	2.2	Updated to core version 2.2 and Xilinx tools 13.3. Revised resources in the IP Facts table and slice counts in Table 7 and Table 8. Changed transmit and receive data widths to 32 bits for Virtex-7 and Kintex-7 devices.
04/24/12	2.3	Updated to core version 2.3; updated to Xilinx tools 14.1. Initial Release of 10GBASE-R/10GBASE-KR version. Added support for Virtex-7 GTHE2 transceivers

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