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EFM32 Tiny Gecko Series 1 Family
EFM32TG11 Family Data Sheet

The EFM32 Tiny Gecko Series 1 MCUs are the world's most energy-friendly microcontrollers, featuring new connectivity interfaces and rich analog features.

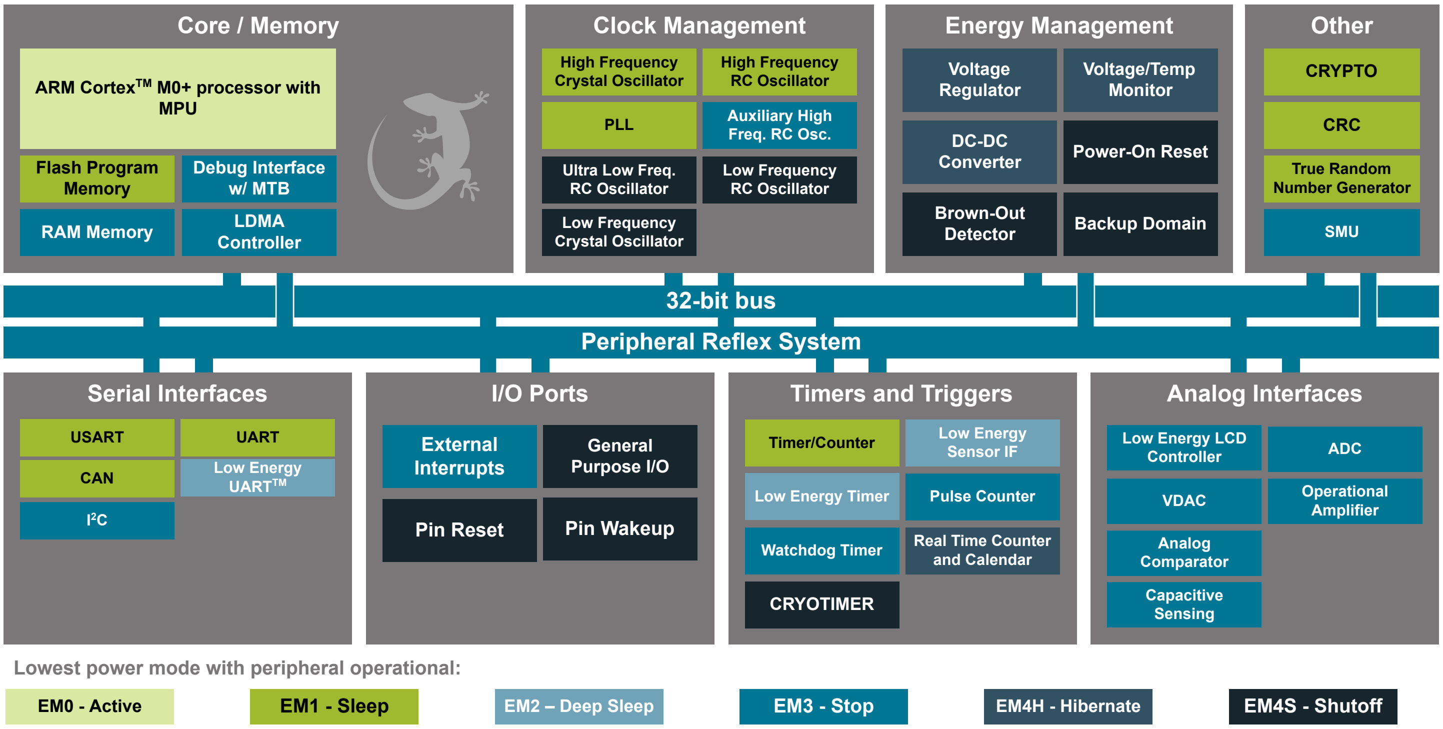
EFM32TG11 includes a powerful and efficient 32-bit ARM® Cortex®-M0+ and provides robust security via a unique cryptographic hardware engine supporting AES, ECC, SHA, and True Random Number Generator (TRNG). New features include a CAN bus controller, highly robust capacitive sensing, and LESENSE/PCNT enhancements for smart energy meters. These features, combined with ultra-low current active mode and short wake-up time from energy-saving modes, make EFM32TG11 microcontrollers well suited for any battery-powered application, as well as other systems requiring high performance and low-energy consumption.

Example applications:

- Smart energy meters
- Industrial and factory automation
- Home automation and security
- Entry-level wearables
- Personal medical devices
- IoT devices

ENERGY FRIENDLY FEATURES

- ARM Cortex-M0+ at 48 MHz
- Ultra low energy operation:
  - 37 µA/MHz in Energy Mode 0 (EM0)
  - 1.30 µA EM2 Deep Sleep current
- CAN 2.0 Bus Controller
- Low energy analog peripherals: ADC, DAC, OPAMP, Comparator, Segment LCD
- Hardware cryptographic engine supports AES, ECC, SHA, and TRNG
- Robust capacitive touch sense
- Footprint compatible with select EFM32 packages
- 5 V tolerant I/O



1. Feature List

The EFM32TG11 highlighted features are listed below.

- **ARM Cortex-M0+ CPU platform**
  - High performance 32-bit processor @ up to 48 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 37 μA/MHz in Active Mode (EM0)
  - 1.30 μA EM2 Deep Sleep current (8 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC buck converter**
- **Backup Power Domain**
  - RTCC and retention registers in a separate power domain, available in all energy modes
  - Operation from backup battery when main power absent/ insufficient
- **Up to 128 kB flash program memory**
- **Up to 32 kB RAM data memory**
- **Communication Interfaces**
  - CAN Bus Controller
    - Version 2.0A and 2.0B up to 1 Mbps
  - 4 × Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
    - Triple buffered full/half-duplex operation with flow control
    - Ultra high speed (24 MHz) operation on one instance
  - 1 × Universal Asynchronous Receiver/ Transmitter
  - 1 × Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 2 × I^2C Interface with SMBus support
    - Address recognition in EM3 Stop Mode
- **Up to 67 General Purpose I/O Pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 5 V tolerance on select pins
  - Asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **Up to 8 Channel DMA Controller**
- **Up to 8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Hardware Cryptography**
  - AES 128/256-bit keys
  - ECC B/K163, B/K233, P192, P224, P256
  - SHA-1 and SHA-2 (SHA-224 and SHA-256)
  - True Random Number Generator (TRNG)
- **Hardware CRC engine**
  - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
  - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8 × 32 segments**
  - Voltage boost, contrast and autonomous animation
  - Patented low-energy LCD driver
- **Ultra Low-Power Precision Analog Peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
    - On-chip temperature sensor
  - 2 × 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
  - Up to 2 × Analog Comparator (ACMP)
  - Up to 4 × Operational Amplifier (OPAMP)
  - Robust current-based capacitive sensing with up to 38 inputs and wake-on-touch (CSEN)
  - Up to 62 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
  - Supply Voltage Monitor

- **Timers/Counters**
  - 2 × 16-bit Timer/Counter
    - 3 or 4 Compare/Capture/PWM channels (4 + 4 on one timer instance)
    - Dead-Time Insertion on one timer instance
  - 2 × 32-bit Timer/Counter
  - 32-bit Real Time Counter and Calendar (RTCC)
  - 32-bit Ultra Low Energy CRYOTIMER for periodic wakeup from any Energy Mode
  - 16-bit Low Energy Timer for waveform generation
  - 16-bit Pulse Counter with asynchronous operation
  - Watchdog Timer with dedicated RC oscillator
- **Low Energy Sensor Interface (LESENSE)**
  - Autonomous sensor monitoring in Deep Sleep Mode
  - Wide range of sensors supported, including LC sensors and capacitive buttons
  - Up to 16 inputs
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
  - 2-pin Serial Wire Debug interface
  - 4-pin JTAG interface
  - Micro Trace Buffer (MTB)
- **Pre-Programmed UART Bootloader**
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - Standard (-40 °C to 85 °C T_A) and Extended (-40 °C to 125 °C T_J) temperature grades available
- **Packages**
  - QFN32 (5x5 mm)
  - TQFP48 (7x7 mm)
  - QFN64 (9x9 mm)
  - TQFP64 (10x10 mm)
  - QFN80 (9x9 mm)
  - TQFP80 (12x12 mm)

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con-verter	LCD	GPIO	Package	Temp Range
EFM32TG11B520F128GM80-A	128	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B520F128GQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B520F128IM80-A	128	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B520F128IQ80-A	128	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B540F64GM80-A	64	32	Yes	Yes	67	QFN80	-40 to +85°C
EFM32TG11B540F64GQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +85°C
EFM32TG11B540F64IM80-A	64	32	Yes	Yes	67	QFN80	-40 to +125°C
EFM32TG11B540F64IQ80-A	64	32	Yes	Yes	63	QFP80	-40 to +125°C
EFM32TG11B520F128GM64-A	128	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B520F128GQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B520F128IM64-A	128	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B520F128IQ64-A	128	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B540F64GM64-A	64	32	Yes	Yes	53	QFN64	-40 to +85°C
EFM32TG11B540F64GQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +85°C
EFM32TG11B540F64IM64-A	64	32	Yes	Yes	53	QFN64	-40 to +125°C
EFM32TG11B540F64IQ64-A	64	32	Yes	Yes	50	QFP64	-40 to +125°C
EFM32TG11B520F128GQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B520F128IQ48-A	128	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B540F64GQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +85°C
EFM32TG11B540F64IQ48-A	64	32	Yes	Yes	34	QFP48	-40 to +125°C
EFM32TG11B520F128GM32-A	128	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B520F128IM32-A	128	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B540F64GM32-A	64	32	Yes	Yes	22	QFN32	-40 to +85°C
EFM32TG11B540F64IM32-A	64	32	Yes	Yes	22	QFN32	-40 to +125°C
EFM32TG11B320F128GM64-A	128	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B320F128GQ64-A	128	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B320F128IM64-A	128	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B320F128IQ64-A	128	32	No	Yes	53	QFP64	-40 to +125°C
EFM32TG11B340F64GM64-A	64	32	No	Yes	56	QFN64	-40 to +85°C
EFM32TG11B340F64GQ64-A	64	32	No	Yes	53	QFP64	-40 to +85°C
EFM32TG11B340F64IM64-A	64	32	No	Yes	56	QFN64	-40 to +125°C
EFM32TG11B340F64IQ64-A	64	32	No	Yes	53	QFP64	-40 to +125°C

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con-verter	LCD	GPIO	Package	Temp Range
EFM32TG11B320F128GQ48-A	128	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B320F128IQ48-A	128	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B340F64GQ48-A	64	32	No	Yes	37	QFP48	-40 to +85°C
EFM32TG11B340F64IQ48-A	64	32	No	Yes	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM64-A	128	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B120F128GQ64-A	128	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B120F128IM64-A	128	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B120F128IQ64-A	128	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B140F64GM64-A	64	32	No	No	56	QFN64	-40 to +85°C
EFM32TG11B140F64GQ64-A	64	32	No	No	53	QFP64	-40 to +85°C
EFM32TG11B140F64IM64-A	64	32	No	No	56	QFN64	-40 to +125°C
EFM32TG11B140F64IQ64-A	64	32	No	No	53	QFP64	-40 to +125°C
EFM32TG11B120F128GQ48-A	128	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B120F128IQ48-A	128	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B140F64GQ48-A	64	32	No	No	37	QFP48	-40 to +85°C
EFM32TG11B140F64IQ48-A	64	32	No	No	37	QFP48	-40 to +125°C
EFM32TG11B120F128GM32-A	128	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B120F128IM32-A	128	32	No	No	24	QFN32	-40 to +125°C
EFM32TG11B140F64GM32-A	64	32	No	No	24	QFN32	-40 to +85°C
EFM32TG11B140F64IM32-A	64	32	No	No	24	QFN32	-40 to +125°C

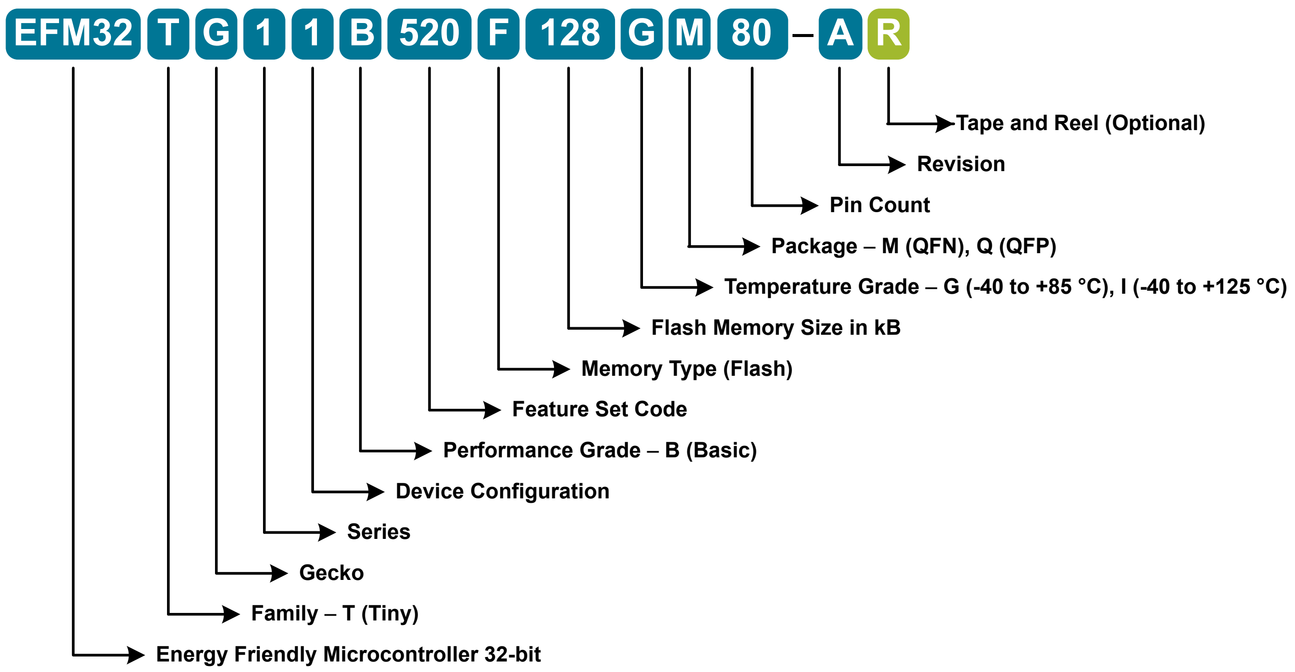


Figure 2.1. Ordering Code Key

Table of Contents

3. System Overview

3.1 Introduction

The Tiny Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Tiny Gecko Series 1 Reference Manual. Any behavior that does not conform to the specifications in this data sheet or the functional descriptions in the Tiny Gecko Series 1 Reference Manual are detailed in the EFM32TG11 Errata document.

A block diagram of the Tiny Gecko Series 1 family is shown in Figure 3.1 Detailed EFM32TG11 Block Diagram on page 10. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

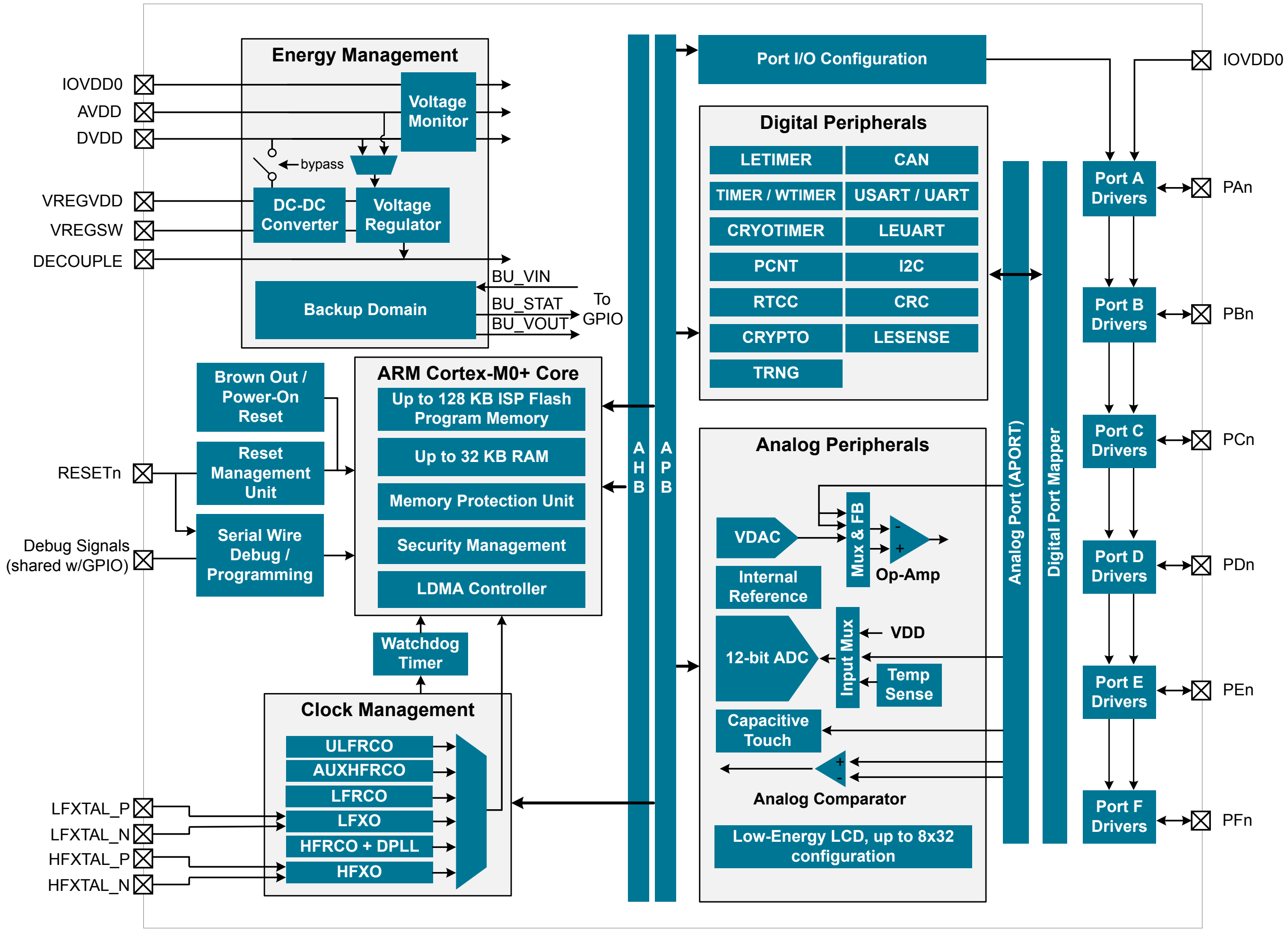


Figure 3.1. Detailed EFM32TG11 Block Diagram

3.2 Power

The EFM32TG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32TG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 EM2 and EM3 Power Domains

The EFM32TG11 has three independent peripheral power domains for use in EM2 and EM3. Two of these domains are dynamic and can be shut down to save energy. Peripherals associated with the two dynamic power domains are listed in Table 3.1 EM2 and EM3 Peripheral Power Subdomains on page 11. If all of the peripherals in a peripheral power domain are unused, the power domain for that group will be powered off in EM2 and EM3, reducing the overall current consumption of the device. Other EM2, EM3, and EM4-capable peripherals and functions not listed in the table below reside on the primary power domain, which is always on in EM2 and EM3.

Table 3.1. EM2 and EM3 Peripheral Power Subdomains

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	CSEN
ADC0	VDAC0
LETIMER0	LEUART0
LESENSE	I2C0
APORT	I2C1
-	IDAC
-	LCD

3.3 General Purpose Input/Output (GPIO)

EFM32TG11 has up to 67 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32TG11. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32TG11 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 48 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.5.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.5.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.6.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter is a subset of the USART module, supporting full duplex asynchronous UART communication with hardware flow control and RS-485.

3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART^{TM} provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.6.4 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.6.5 Controller Area Network (CAN)

The CAN peripheral provides support for communication at up to 1 Mbps over CAN protocol version 2.0 part A and B. It includes 32 message objects with independent identifier masks and retains message RAM in EM2. Automatic retransmittion may be disabled in order to support Time Triggered CAN applications.

3.6.6 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.6.7 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE^{TM} is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. Tiny Gecko Series 1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.6 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.7 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x32 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32TG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M0+ RISC processor
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Micro-Trace Buffer (MTB)
- Up to 128 kB flash program memory
- Up to 32 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.10.4 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed. More information about the bootloader protocol and usage can be found in *AN0003: UART Bootloader*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or within Simplicity Studio in the [**Documentation**] area.

3.11 Memory Map

The EFM32TG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

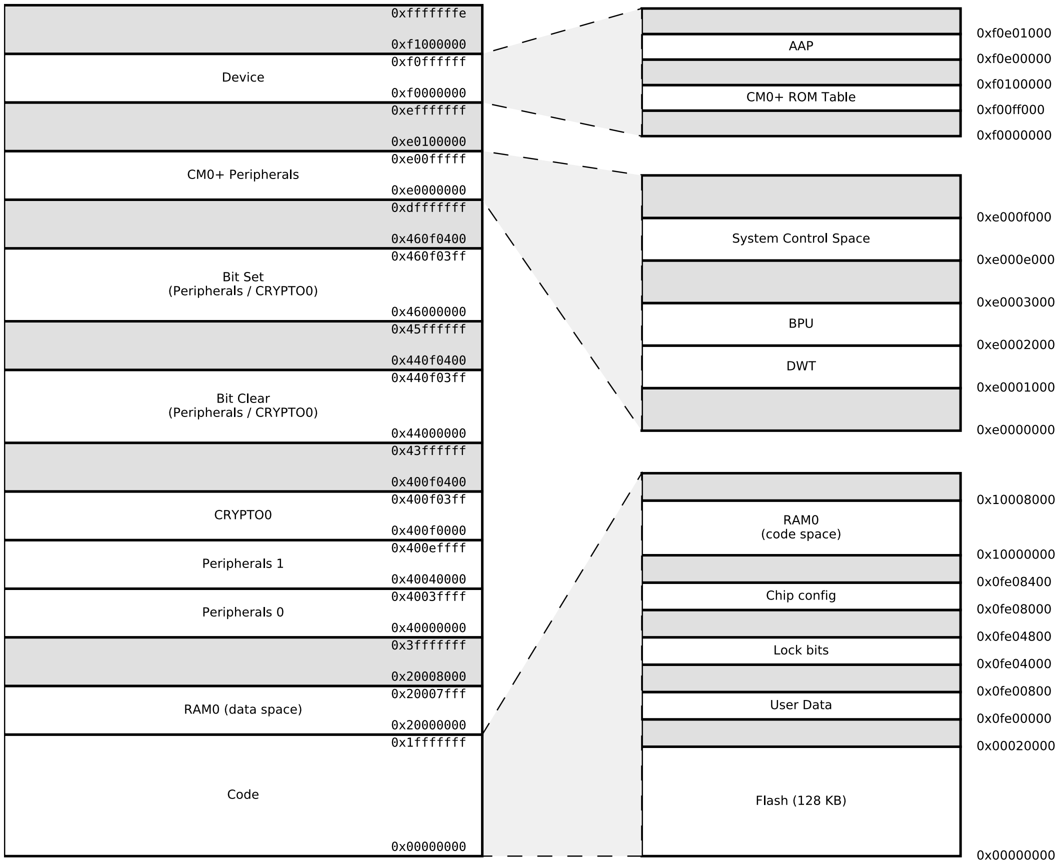


Figure 3.2. EFM32TG11 Memory Map — Core Peripherals and Code Space

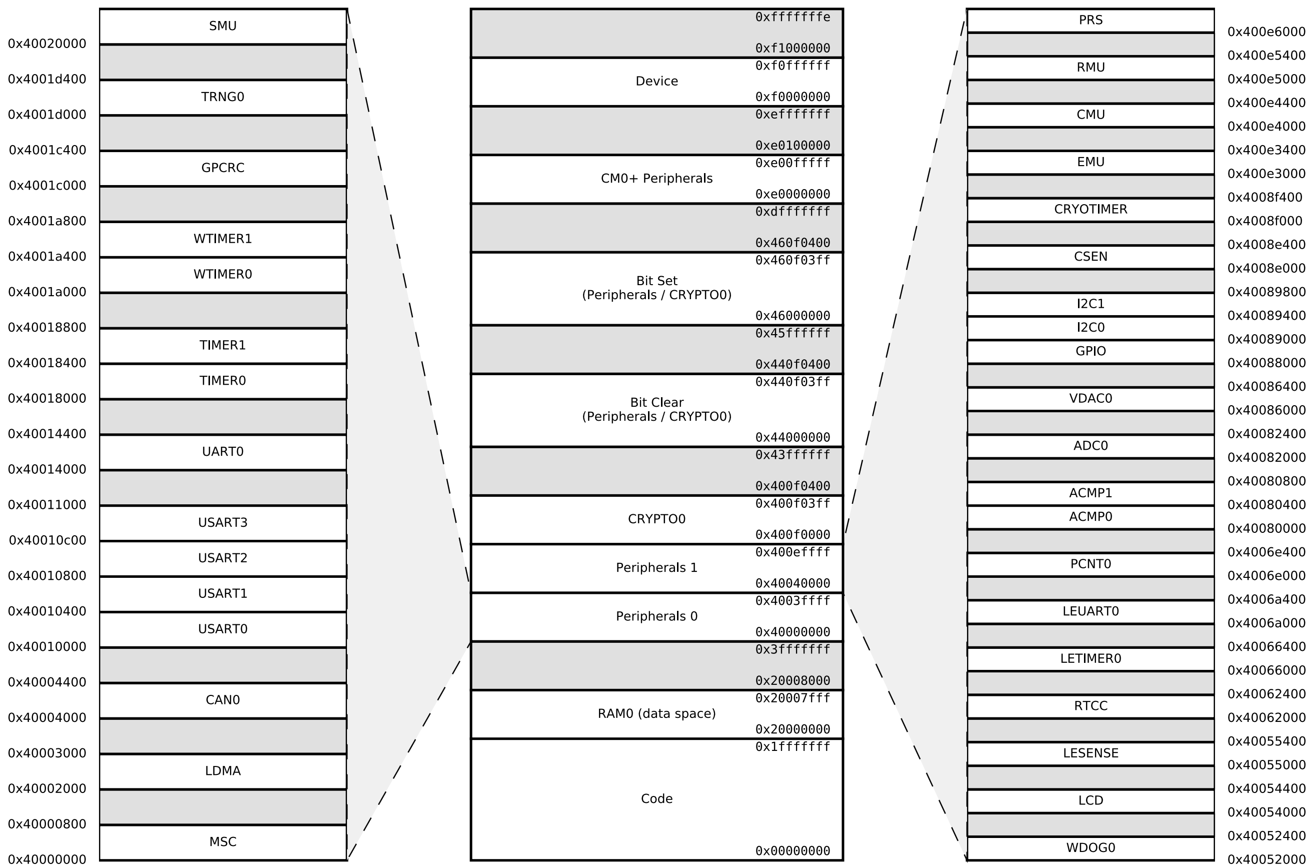


Figure 3.3. EFM32TG11 Memory Map — Peripherals

3.12 Configuration Summary

The features of the EFM32TG11 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA, SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	I^2S, SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	IrDA, SmartCard, High-Speed	US2_TX, US2_RX, US2_CLK, US2_CS
USART3	I^2S, SmartCard	US3_TX, US3_RX, US3_CLK, US3_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	-	TIM1_CC[3:0]
WTIMER0	with DTI	WTIM0_CC[2:0], WTIM0_CDTI[2:0]
WTIMER1	-	WTIM1_CC[3:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to 4.1.2.1 General Operating Conditions for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1	V / µs
DC voltage on any GPIO pin	V_{DIGPIN}	5V tolerant GPIO pins[1 2 3]	-0.3	—	Min of 5.25 and IOVDD +2	V
		LCD pins[3]	-0.3	—	Min of 3.8 and IOVDD +2	V
		Standard GPIO pins	-0.3	—	IOVDD+0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA
Junction temperature	T_J	-G grade devices	-40	—	105	°C
		-I grade devices	-40	—	125	°C

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.
2. Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.
3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range[6]	T_A	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage[2]	V_{AVDD}		1.8	3.3	3.8	V
VREGVDD operating supply voltage[2 1]	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	$I_{VREGVDD}$	DCDC in bypass, T ≤ 85 °C	—	—	200	mA
		DCDC in bypass, T > 85 °C	—	—	100	mA
DVDD operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage	V_{IOVDD}	All IOVDD pins[5]	1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor[3 4]	$C_{DECOUPLE}$		0.75	1.0	2.75	µF
HFCORECLK frequency	f_{CORE}	VSCALE2, MODE = WS1	—	—	48	MHz
		VSCALE2, MODE = WS0	—	—	25	MHz
		VSCALE0, MODE = WS1	—	—	20	MHz
		VSCALE0, MODE = WS0	—	—	10	MHz
HFCLK frequency	f_{HFCLK}	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFSRCCLK frequency	$f_{HFSRCCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFBUSCLK frequency	$f_{HFBUSCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERCLK frequency	$f_{HFPERCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERBCLK frequency	$f_{HFPERBCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz
HFPERCCLK frequency	$f_{HFPERCCLK}$	VSCALE2	—	—	48	MHz
		VSCALE0	—	—	20	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$. 2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate. 3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias. 4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor). 5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD. 6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and $THETA_{JA}$.						

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN32 Package	$THETA_{JA\_QFN32}$	4-Layer PCB, Air velocity = 0 m/s	—	25.7	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	23.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	21.3	—	°C/W
Thermal resistance, TQFP48 Package	$THETA_{JA\_TQFP48}$	4-Layer PCB, Air velocity = 0 m/s	—	44.1	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	43.5	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.3	—	°C/W
Thermal resistance, QFN64 Package	$THETA_{JA\_QFN64}$	4-Layer PCB, Air velocity = 0 m/s	—	20.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	18.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	—	°C/W
Thermal resistance, TQFP64 Package	$THETA_{JA\_TQFP64}$	4-Layer PCB, Air velocity = 0 m/s	—	37.3	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	35.6	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	33.8	—	°C/W
Thermal resistance, QFN80 Package	$THETA_{JA\_QFN80}$	4-Layer PCB, Air velocity = 0 m/s	—	20.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	18.2	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	16.4	—	°C/W
Thermal resistance, TQFP80 Package	$THETA_{JA\_TQFP80}$	4-Layer PCB, Air velocity = 0 m/s	—	49.3	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	44.5	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	42.6	—	°C/W

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 μH (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 μF (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.8	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC accuracy	ACC_{DC}	Low Noise (LN) mode, 1.8 V target output	TBD	—	TBD	V
Regulation window[4]	WIN_{REG}	Low Power (LP) mode, LPCMPBIASEMxx[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 μA	TBD	—	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	TBD	—	TBD	V
Steady-state output ripple	V_R		—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	25	TBD	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive[2], T ≤ 85 °C	—	—	200	mA
		Low noise (LN) mode, Heavy Drive[2], T > 85 °C	—	—	100	mA
		Low noise (LN) mode, Medium Drive[2]	—	—	100	mA
		Low noise (LN) mode, Light Drive[2]	—	—	50	mA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 0	—	—	75	μA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 3	—	—	10	mA
DCDC nominal output capacitor[5]	C_{DCDC}	25% tolerance	1	4.7	4.7	μF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	μH
Resistance in Bypass mode	R_{BYP}		—	1.2	TBD	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 μF. Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 μF. See Application Note AN0948 for details.

4.1.5 Backup Supply Domain

Table 4.5. Backup Supply Domain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Backup supply voltage range	V_{BU_VIN}		TBD	—	3.8	V
PWRRES resistor	R_{PWRRES}	EMU_BUCTRL_PWRRES = RES0	TBD	3900	TBD	Ω
		EMU_BUCTRL_PWRRES = RES1	TBD	1800	TBD	Ω
		EMU_BUCTRL_PWRRES = RES2	TBD	1330	TBD	Ω
		EMU_BUCTRL_PWRRES = RES3	TBD	815	TBD	Ω
Output impedance between BU_VIN and BU_VOUT [2]	R_{BU_VOUT}	EMU_BUCTRL_VOUTRES = STRONG	TBD	110	TBD	Ω
		EMU_BUCTRL_VOUTRES = MED	TBD	775	TBD	Ω
		EMU_BUCTRL_VOUTRES = WEAK	TBD	6500	TBD	Ω
Supply current	I_{BU_VIN}	BU_VIN not powering backup domain	—	10	TBD	nA
		BU_VIN powering backup domain[1]	—	450	TBD	nA

Note:
1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.
2. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.