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EFM[®]32

... the world's most energy friendly microcontrollers

EFM32TG825 DATASHEET

F32/F16/F8

- **ARM Cortex-M3 CPU platform**
 - High Performance 32-bit processor @ up to 32 MHz
 - Wake-up Interrupt Controller
- **Flexible Energy Management System**
 - 20 nA @ 3 V Shutoff Mode
 - 0.6 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
 - 1.0 µA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
 - 51 µA/MHz @ 3 V Sleep Mode
 - 150 µA/MHz @ 3 V Run Mode, with code executed from flash
- **32/16/8 KB Flash**
- **4/4/2 KB RAM**
- **37 General Purpose I/O pins**
 - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
 - Configurable peripheral I/O locations
 - 16 asynchronous external interrupts
 - Output state retention and wake-up from Shutoff Mode
- **8 Channel DMA Controller**
- **8 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Hardware AES with 128/256-bit keys in 54/75 cycles**
- **Timers/Counters**
 - 2× 16-bit Timer/Counter
 - 2×3 Compare/Capture/PWM channels
 - 16-bit Low Energy Timer
 - 1× 24-bit Real-Time Counter
 - 1× 16-bit Pulse Counter
 - Watchdog Timer with dedicated RC oscillator @ 50 nA
- **Integrated LCD Controller for up to 8×11 segments**
 - Voltage boost, adjustable contrast and autonomous animation
- **Communication interfaces**
 - 2× Universal Synchronous/Asynchronous Receiver/Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
 - Triple buffered full/half-duplex operation
 - Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - I²C Interface with SMBus support
 - Address recognition in Stop Mode
- **Ultra low power precision analog peripherals**
 - 12-bit 1 Msamples/s Analog to Digital Converter
 - 4 single ended channels/2 differential channels
 - On-chip temperature sensor
 - 12-bit 500 ksamples/s Digital to Analog Converter
 - 2× Analog Comparator
 - Capacitive sensing with up to 4 inputs
 - 3× Operational Amplifier
 - 6.1 MHz GBW, Rail-to-rail, Programmable Gain
 - Supply Voltage Comparator
- **Low Energy Sensor Interface (LESENSE)**
 - Autonomous sensor monitoring in Deep Sleep Mode
 - Wide range of sensors supported, including LC sensors and capacitive buttons
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **2-pin Serial Wire Debug interface**
 - 1-pin Serial Wire Viewer
- **Pre-Programmed UART Bootloader**
- **Temperature range -40 to 85 °C**
- **Single power supply 1.98 to 3.8 V**
- **BGA48 package**

32-bit ARM Cortex-M0+, Cortex-M3 and Cortex-M4 microcontrollers for:

- Energy, gas, water and smart metering
- Health and fitness applications
- Smart accessories
- Alarm and security systems
- Industrial and home automation



1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32TG825 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32TG825F8-BGA48	8	2	32	1.98 - 3.8	-40 - 85	BGA48
EFM32TG825F16-BGA48	16	4	32	1.98 - 3.8	-40 - 85	BGA48
EFM32TG825F32-BGA48	32	4	32	1.98 - 3.8	-40 - 85	BGA48

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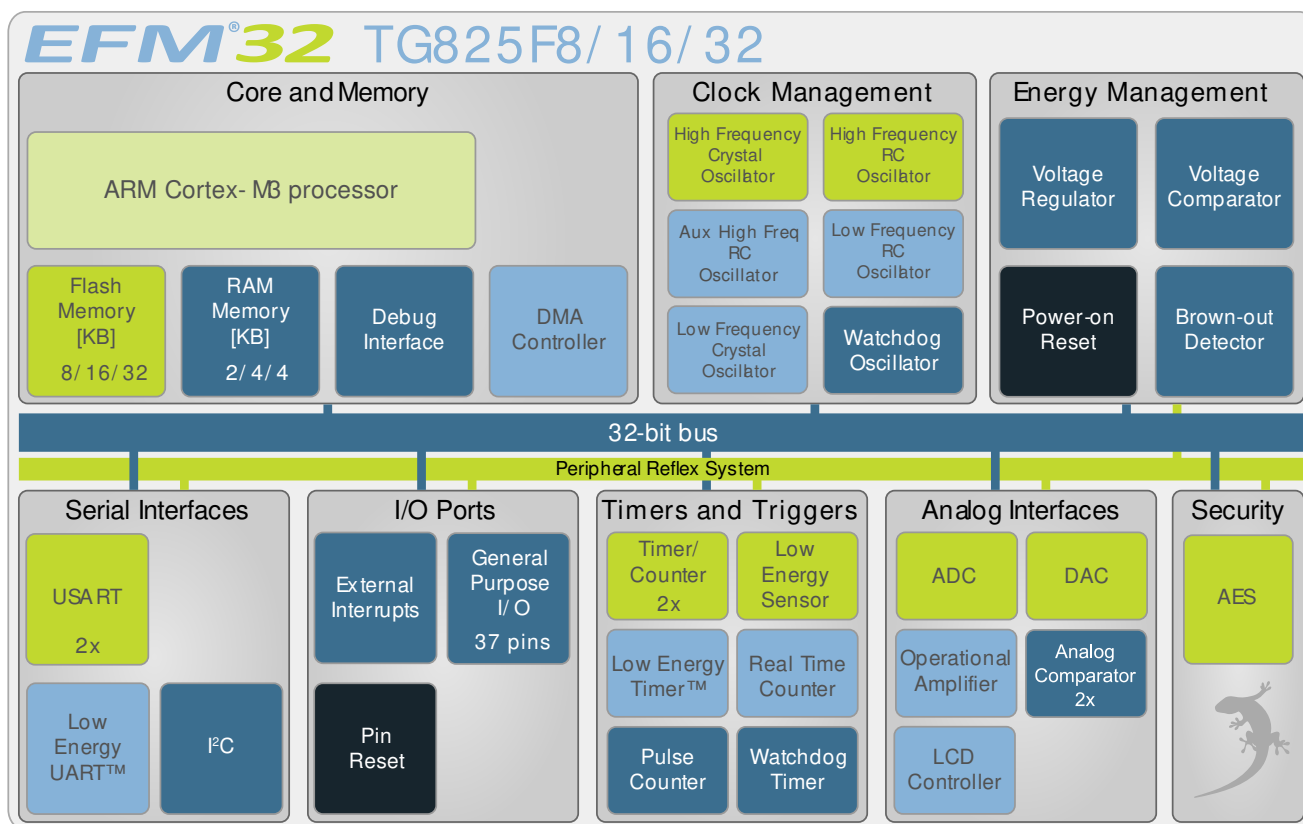
2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32TG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32TG825 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32TG Reference Manual*.

A block diagram of the EFM32TG825 is shown in Figure 2.1 (p. 3) .

Figure 2.1. Block Diagram



2.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M3 is described in detail in *EFM32 Cortex-M3 Reference Manual*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32TG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is

divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 μ DMA controller licensed from ARM.

2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32TG.

2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32TG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32TG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

2.1.10 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART[™], the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output.

2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.16 Low Energy Timer (LETIMER)

The unique LETIMER[™], the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

2.1.17 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACTK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

2.1.18 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.19 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.20 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 4 external pins and 6 internal signals.

2.1.21 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has one single ended output buffer connected to channel 0. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

2.1.22 Operational Amplifier (OPAMP)

The EFM32TG825 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

2.1.23 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE[™]), is a highly configurable sensor interface with support for up to 4 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

2.1.24 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

2.1.25 General Purpose Input/Output (GPIO)

In the EFM32TG825, there are 37 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

2.1.26 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x11 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

2.2 Configuration Summary

The features of the EFM32TG825 is a subset of the feature set described in the EFM32TG Reference Manual. Table 2.1 (p. 7) describes device specific implementation of the features.

Table 2.1. Configuration Summary

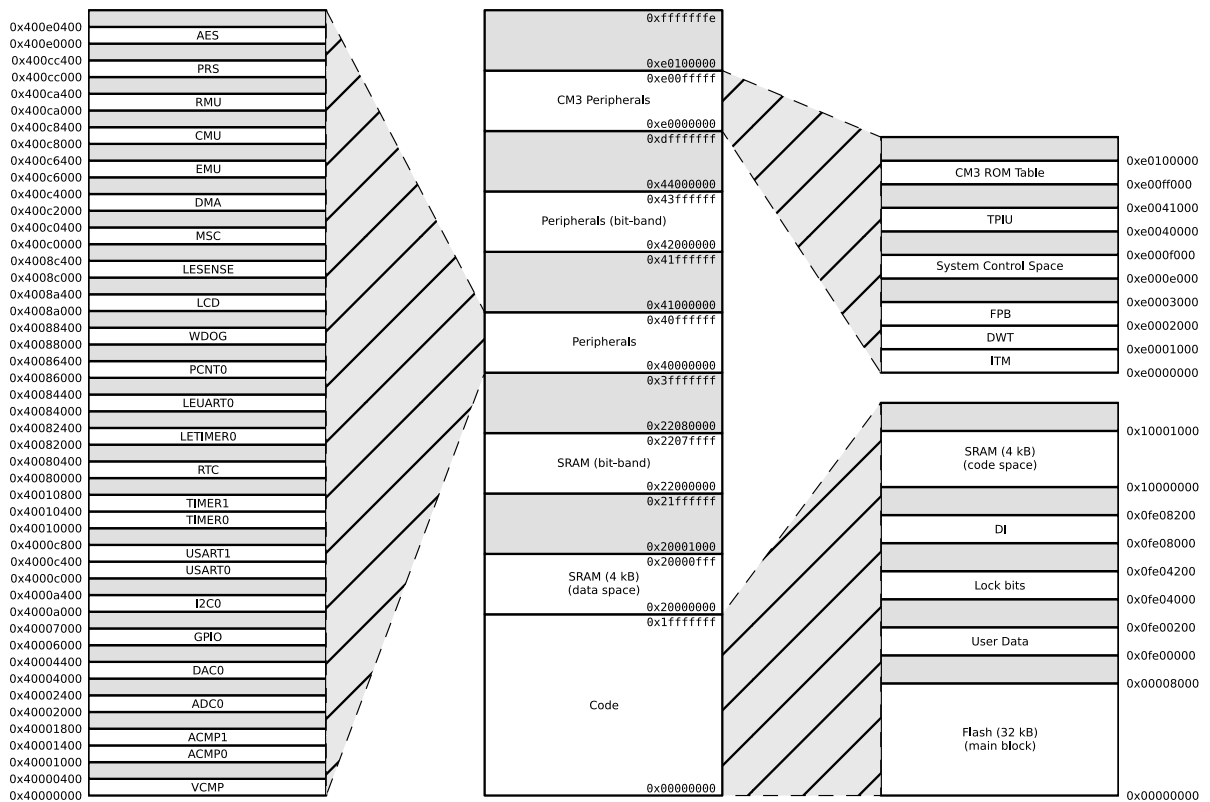
Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[4], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:5], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:4]
DAC0	Full configuration	DAC0_OUT[0], DAC0_OUTxALT
OPAMP		
AES	Full configuration	NA
GPIO	37 pins	Available pins are shown in Table 4.3 (p. 52)

Module	Configuration	Pin Connections
LCD	Full configuration	LCD_SEG[10:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

2.3 Memory Map

The EFM32TG825 memory map is shown in Figure 2.2 (p. 8), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32TG825 Memory Map with largest RAM and Flash sizes



3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}\text{C}$ and $V_{DD}=3.0\text{ V}$, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 9) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 9).

Table 3.1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{STG}	Storage temperature range		-40		150 ¹	$^{\circ}\text{C}$
T_S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	$^{\circ}\text{C}$
V_{DDMAX}	External main supply voltage		0		3.8	V
V_{IOPIN}	Voltage on any I/O pin		-0.3		$V_{DD}+0.3$	V

¹Based on programmed devices tested for 10000 hours at 150 $^{\circ}\text{C}$. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{AMB}	Ambient temperature range	-40		85	$^{\circ}\text{C}$
V_{DDOP}	Operating supply voltage	1.98		3.8	V
f_{APB}	Internal APB clock frequency			32	MHz
f_{AHB}	Internal AHB clock frequency			32	MHz

3.4 Current Consumption

Table 3.3. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	32 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V		157		μA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		150	170	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		153	172	μA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		155	175	μA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		157	178	μA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		162	183	μA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		200	240	μA/MHz
I _{EM1}	EM1 current (Production test condition = 14 MHz)	32 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V		53		μA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		51	57	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		55	59	μA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		56	61	μA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		58	63	μA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V		63	68	μA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V		100	122	μA/MHz
I _{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =25°C		1.0	1.2	μA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =85°C		2.4	5.0	μA
I _{EM3}	EM3 current	V _{DD} = 3.0 V, T _{AMB} =25°C		0.59	1.0	μA
		V _{DD} = 3.0 V, T _{AMB} =85°C		2.0	4.5	μA
I _{EM4}	EM4 current	V _{DD} = 3.0 V, T _{AMB} =25°C		0.02	0.055	μA
		V _{DD} = 3.0 V, T _{AMB} =85°C		0.25	0.70	μA

Figure 3.1. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.

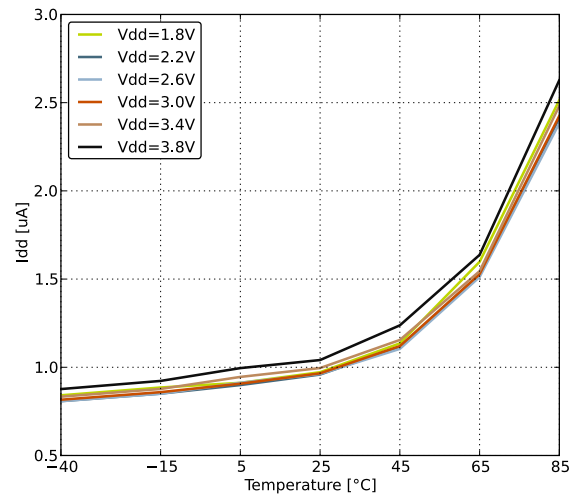
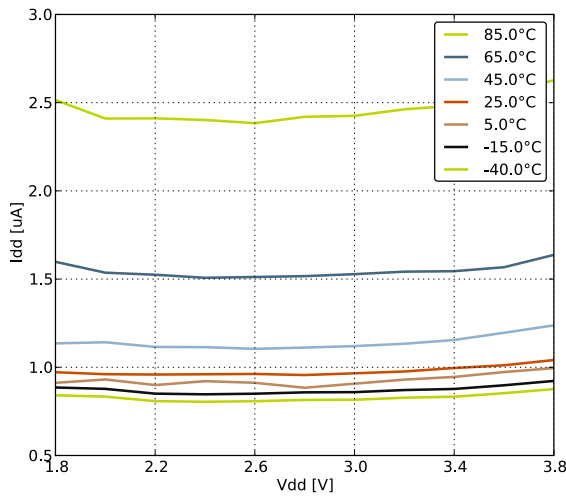


Figure 3.2. EM3 current consumption.

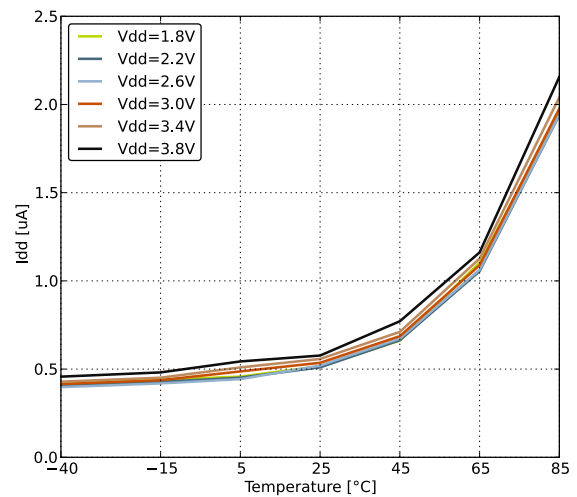
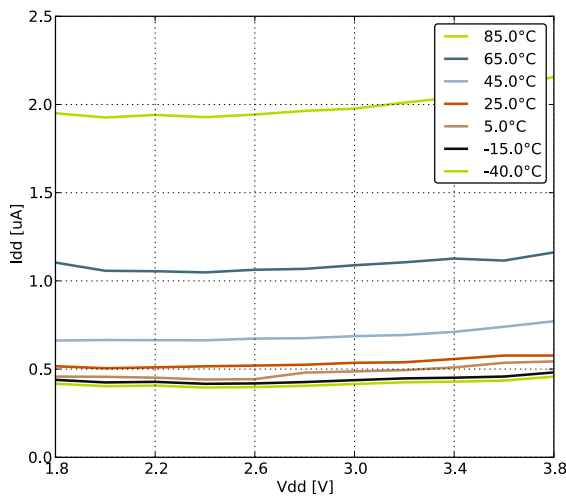
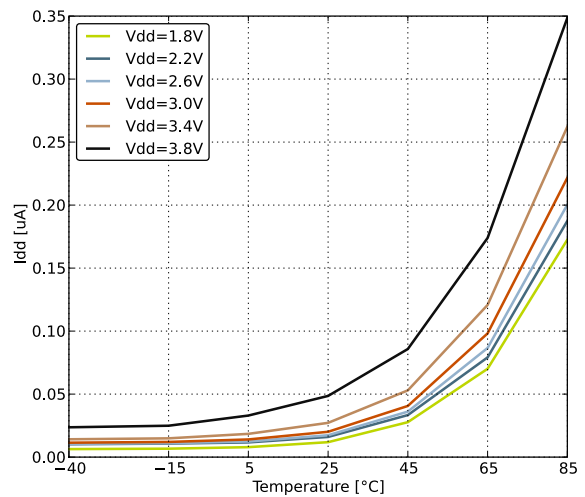
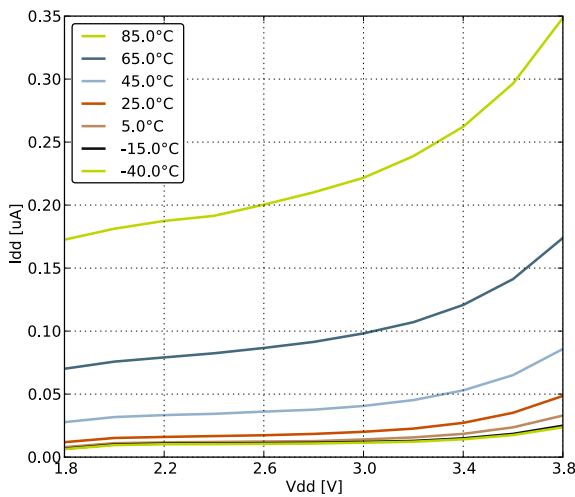


Figure 3.3. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
t_{EM10}	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
t_{EM20}	Transition time from EM2 to EM0		2		μ s
t_{EM30}	Transition time from EM3 to EM0		2		μ s
t_{EM40}	Transition time from EM4 to EM0		163		μ s

3.6 Power Management

The EFM32TG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.5. Power Management

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{BODextthr-}$	BOD threshold on falling external supply voltage		1.74		1.96	V
$V_{BODextthr+}$	BOD threshold on rising external supply voltage			1.85	1.98	V
$V_{PORthr+}$	Power-on Reset (POR) threshold on rising external supply voltage				1.98	V
t_{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μ s
$C_{DECOUPLE}$	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μ F

3.7 Flash

Table 3.6. Flash

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
RET _{FLASH}	Flash data retention	T _{AMB} <150°C	10000			h
		T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) programming time		20			µs
t _{P_ERASE}	Page erase time		20	20.4	20.8	ms
t _{D_ERASE}	Device erase time		40	40.8	41.6	ms
I _{ERASE}	Erase current				7 ¹	mA
I _{WRITE}	Write current				7 ¹	mA
V _{FLASH}	Supply voltage during flash erase and write		1.98		3.8	V

¹Measured at 25°C

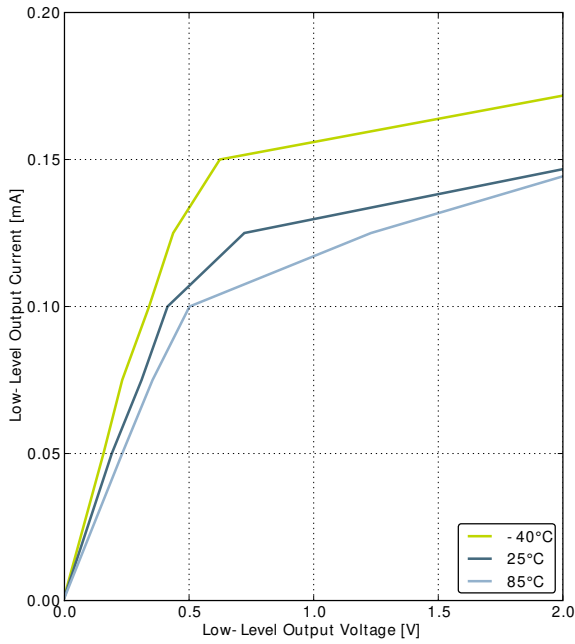
3.8 General Purpose Input Output

Table 3.7. GPIO

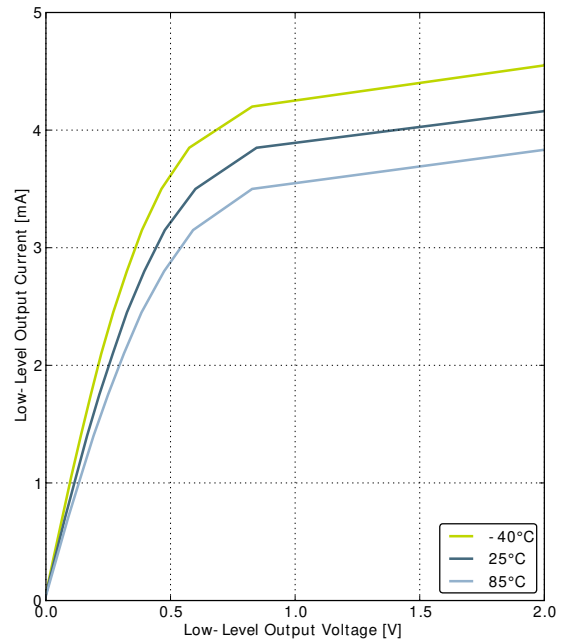
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IOIL}	Input low voltage				0.30V _{DD}	V
V _{IOIH}	Input high voltage		0.70V _{DD}			V
V _{IOOH}	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V _{DD}		V
		Sourcing 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V _{DD}		V
		Sourcing 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V _{DD}		V
		Sourcing 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V _{DD}		V
		Sourcing 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V _{DD}			V
		Sourcing 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V _{DD}			V
		Sourcing 20 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60V _{DD}			V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80V _{DD}			V
V _{IOOL}	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.20V _{DD}		V
		Sinking 0.1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.10V _{DD}		V
		Sinking 1 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.10V _{DD}		V
		Sinking 1 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.05V _{DD}		V
		Sinking 6 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.30V _{DD}	V
		Sinking 6 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.20V _{DD}	V
		Sinking 20 mA, V _{DD} =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.35V _{DD}	V
		Sinking 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.20V _{DD}	V
I _{IOLEAK}	Input leakage current	High Impedance IO connected to GROUND or V _{DD}		±0.1	±100	nA
R _{PU}	I/O pin pull-up resistor			40		kOhm
R _{PD}	I/O pin pull-down resistor			40		kOhm
R _{IOESD}	Internal ESD series resistor			200		Ohm
t _{IOGLITCH}	Pulse width of pulses to be removed by the glitch suppression filter		10		50	ns
t _{IOOF}	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C _L =12.5-25pF.	20+0.1C _L		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C _L =350-600pF	20+0.1C _L		250	ns
V _{IOHYST}	I/O pin hysteresis (V _{IOTHR+} - V _{IOTHR-})	V _{DD} = 1.98 - 3.8 V	0.1V _{DD}			V

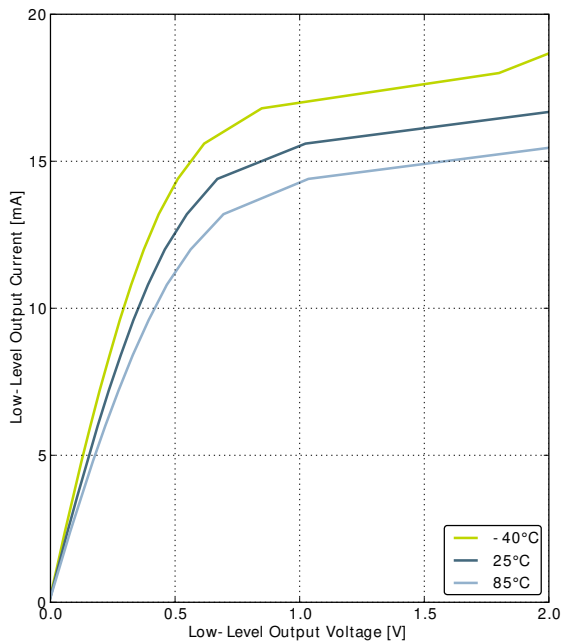
Figure 3.4. Typical Low-Level Output Current, 2V Supply Voltage



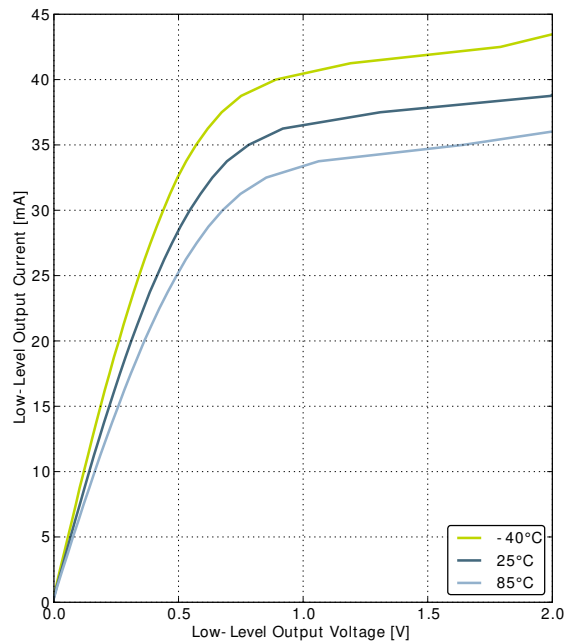
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

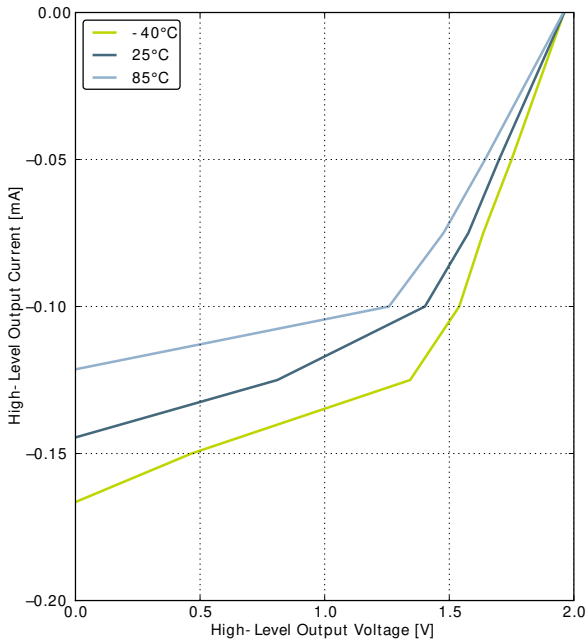


GPIO_Px_CTRL DRIVEMODE = STANDARD

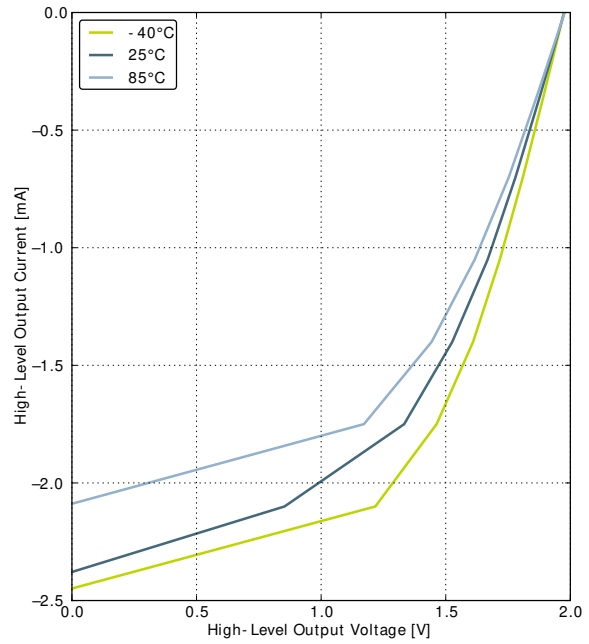


GPIO_Px_CTRL DRIVEMODE = HIGH

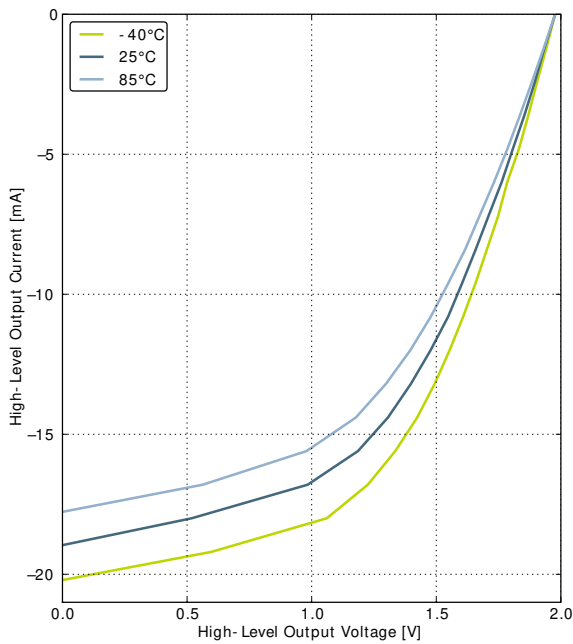
Figure 3.5. Typical High-Level Output Current, 2V Supply Voltage



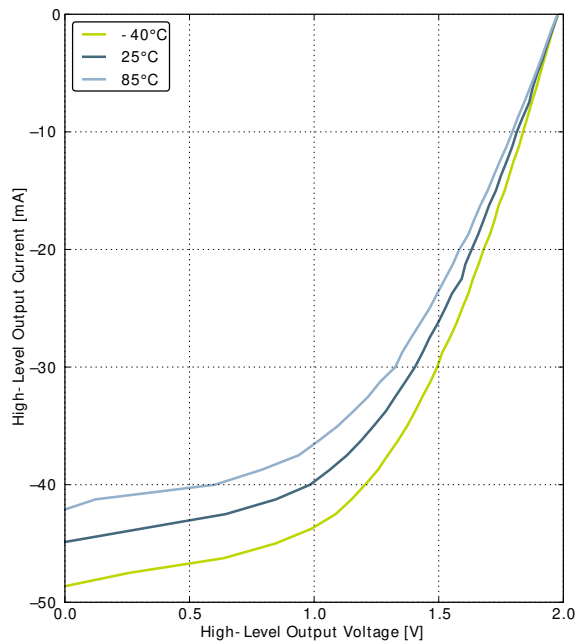
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

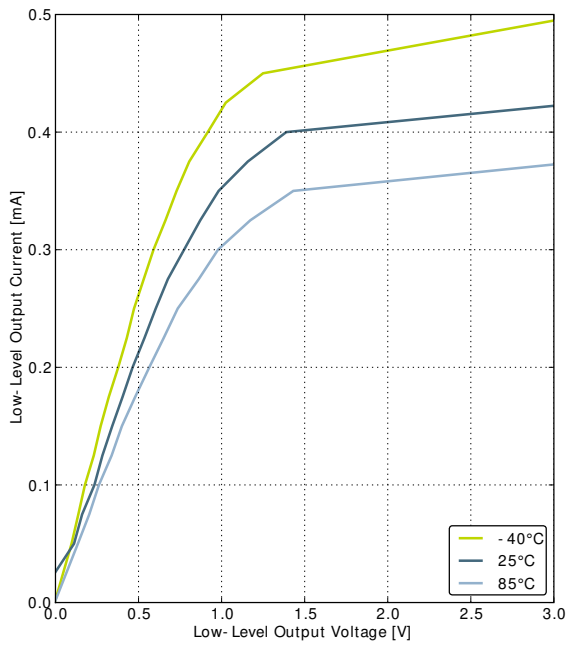


GPIO_Px_CTRL DRIVEMODE = STANDARD

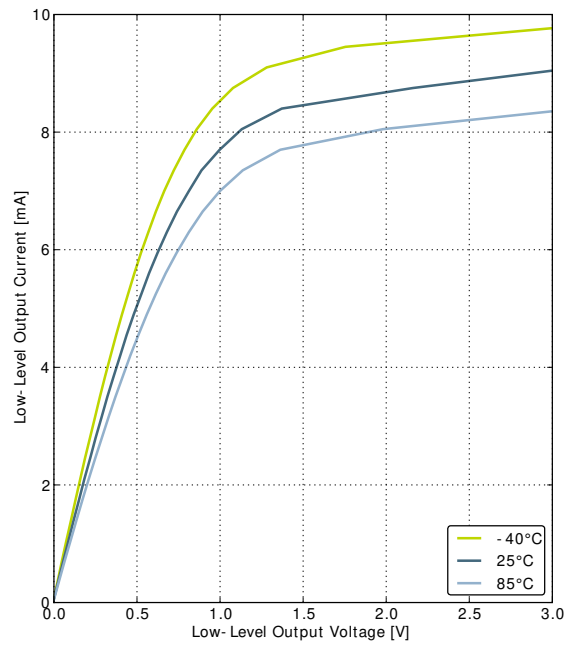


GPIO_Px_CTRL DRIVEMODE = HIGH

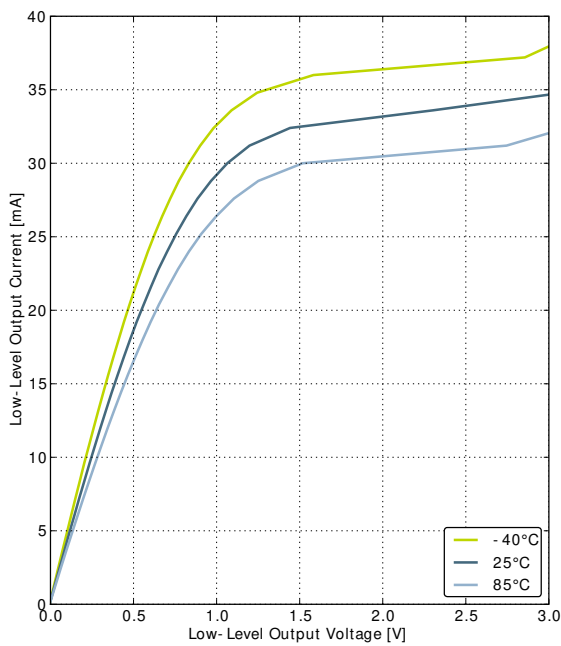
Figure 3.6. Typical Low-Level Output Current, 3V Supply Voltage



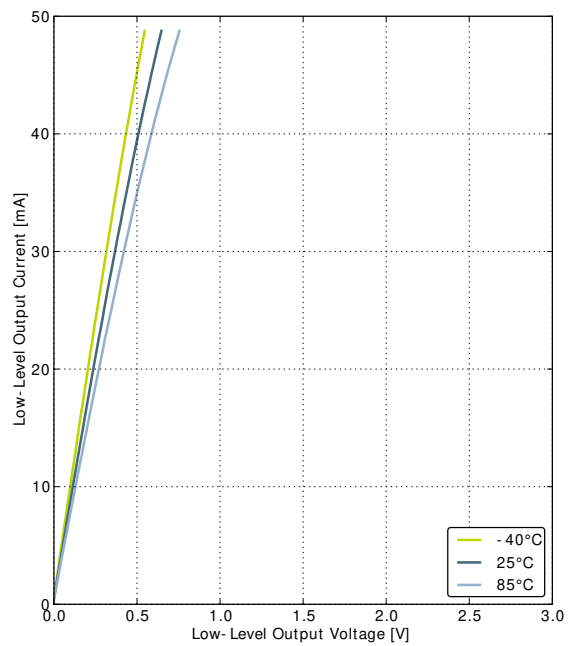
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

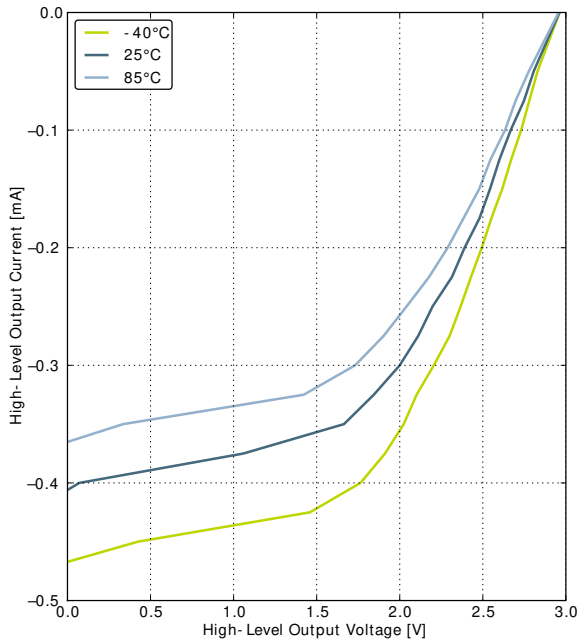


GPIO_Px_CTRL DRIVEMODE = STANDARD

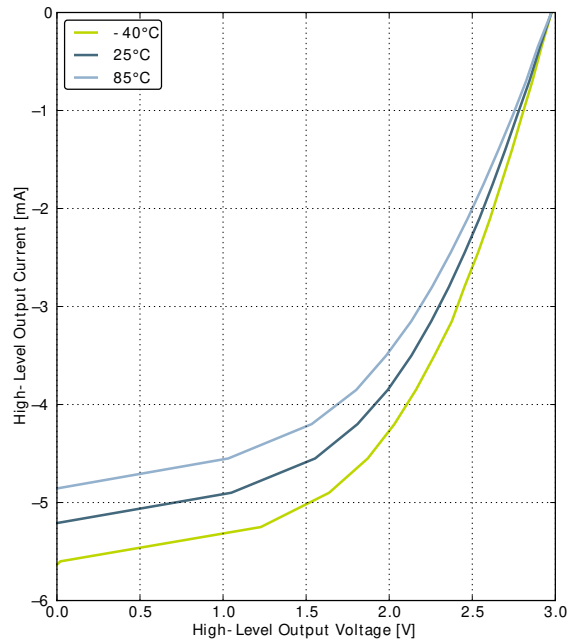


GPIO_Px_CTRL DRIVEMODE = HIGH

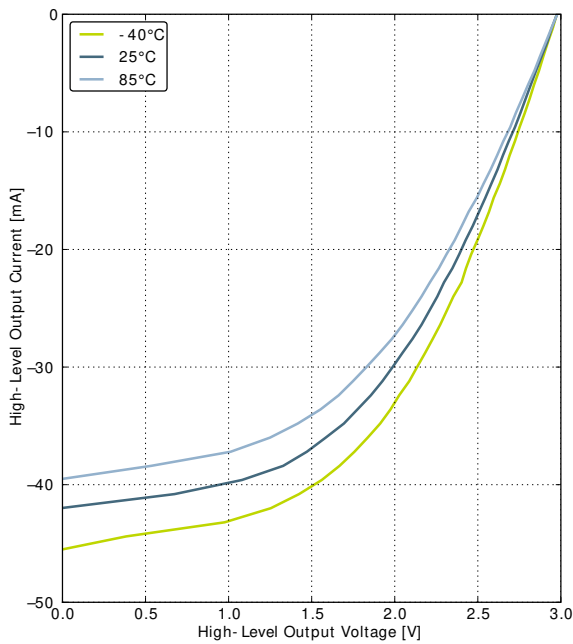
Figure 3.7. Typical High-Level Output Current, 3V Supply Voltage



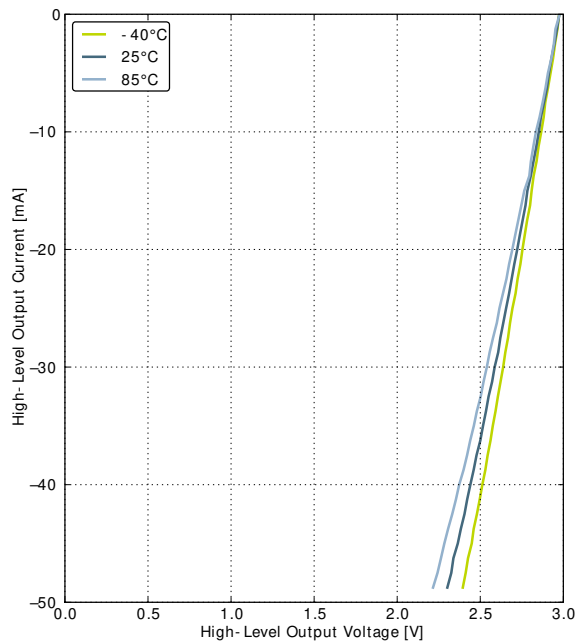
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

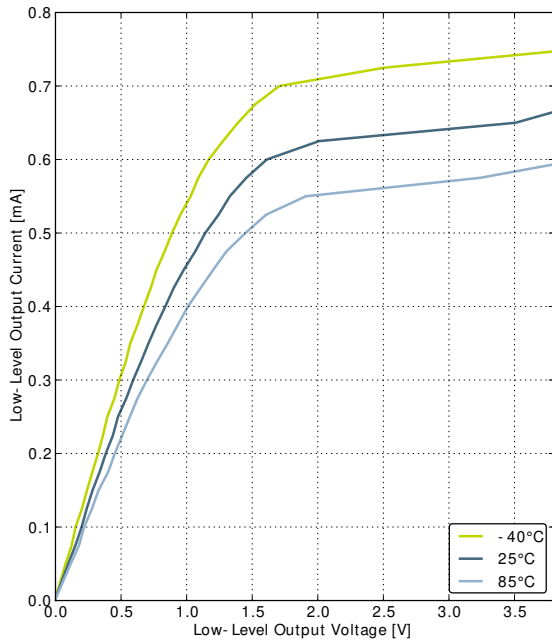


GPIO_Px_CTRL DRIVEMODE = STANDARD

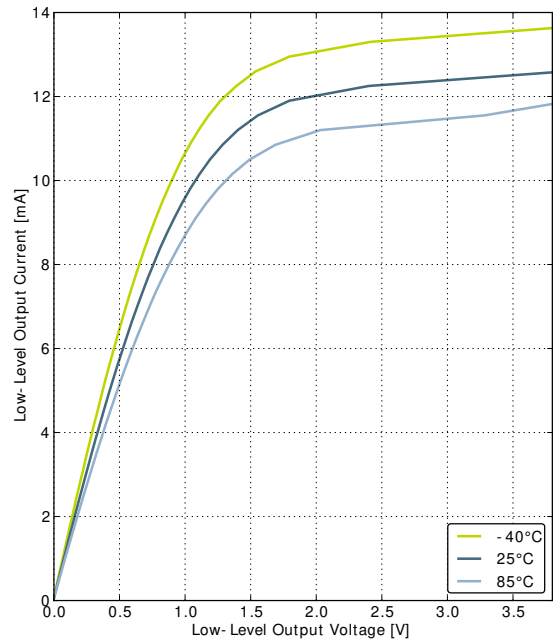


GPIO_Px_CTRL DRIVEMODE = HIGH

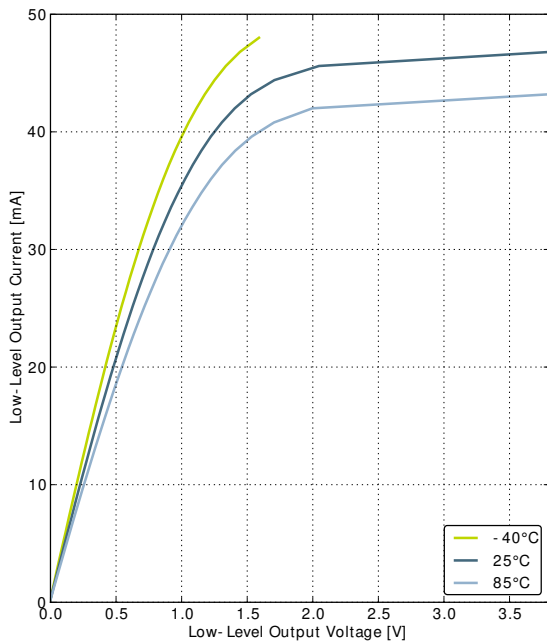
Figure 3.8. Typical Low-Level Output Current, 3.8V Supply Voltage



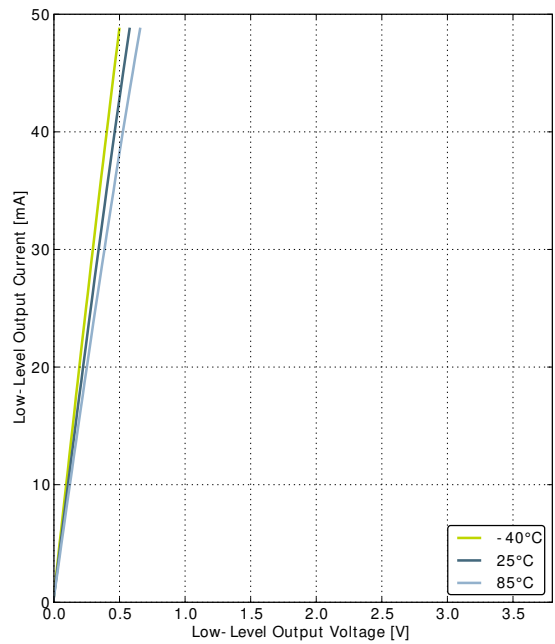
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

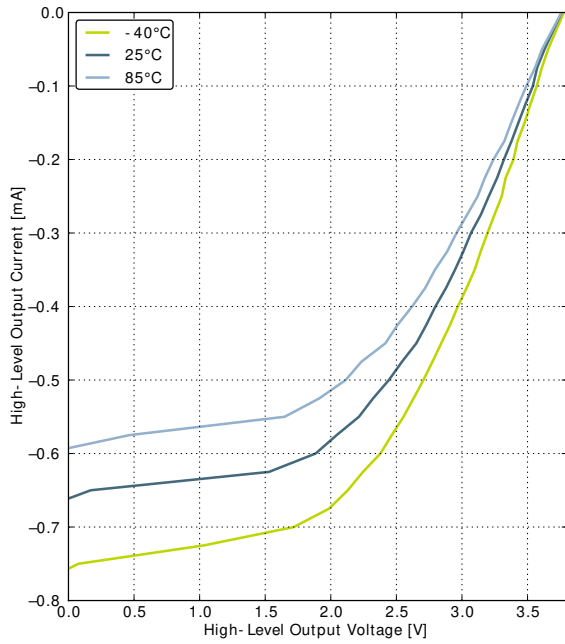


GPIO_Px_CTRL DRIVEMODE = STANDARD

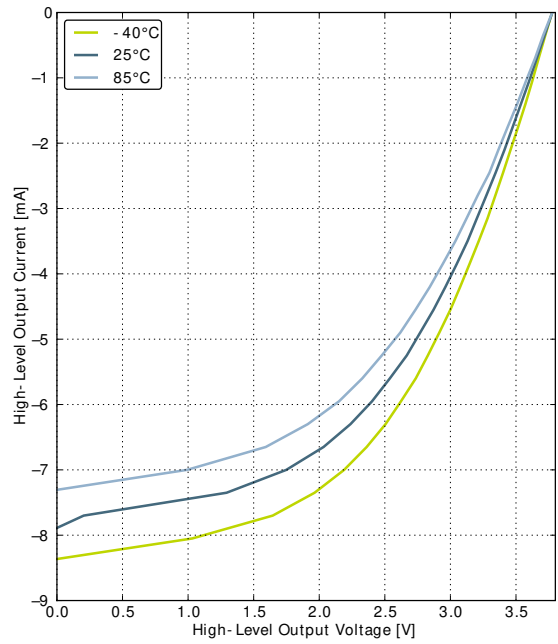


GPIO_Px_CTRL DRIVEMODE = HIGH

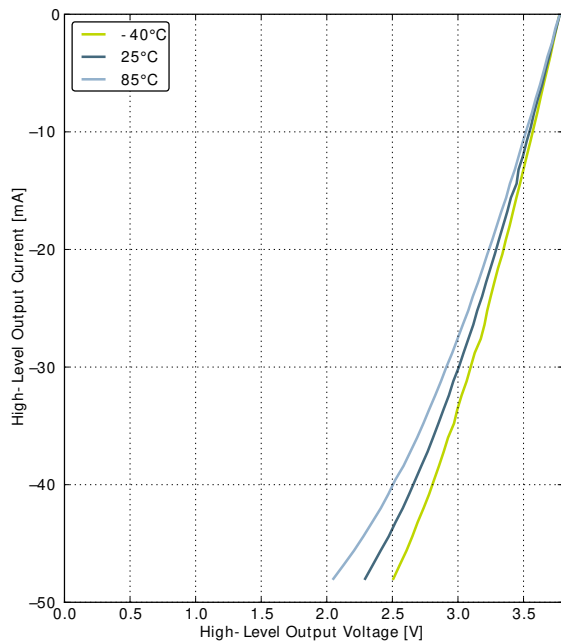
Figure 3.9. Typical High-Level Output Current, 3.8V Supply Voltage



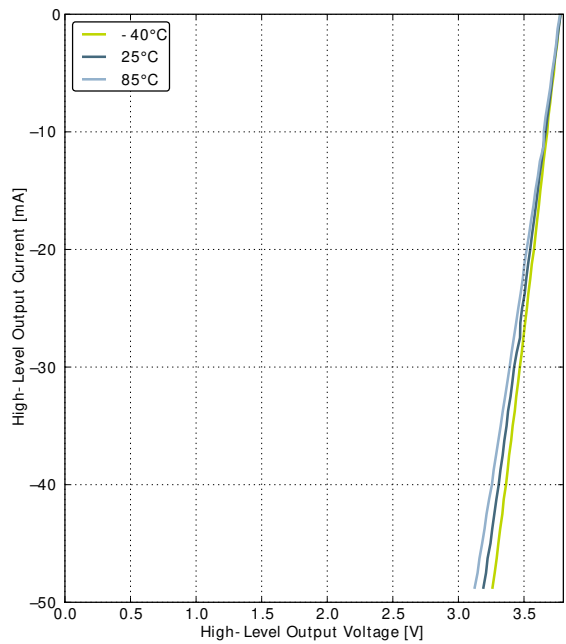
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9 Oscillators

3.9.1 LFXO

Table 3.8. LFXO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{LFXO}	Supported nominal crystal frequency			32.768		kHz
ESR _{LFXO}	Supported crystal equivalent series resistance (ESR)			30	120	kOhm
C _{LFXOL}	Supported crystal external load range		x ¹		25	pF
I _{LFXO}	Current consumption for core and buffer after startup.	ESR=30 kOhm, C _L =10 pF, LFXOBOOST in CMU_CTRL is 1		190		nA
t _{LFXO}	Start- up time.	ESR=30 kOhm, C _L =10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1		400		ms

¹See Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup in energyAware Designer in Simplicity Studio

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

3.9.2 HFXO

Table 3.9. HFXO

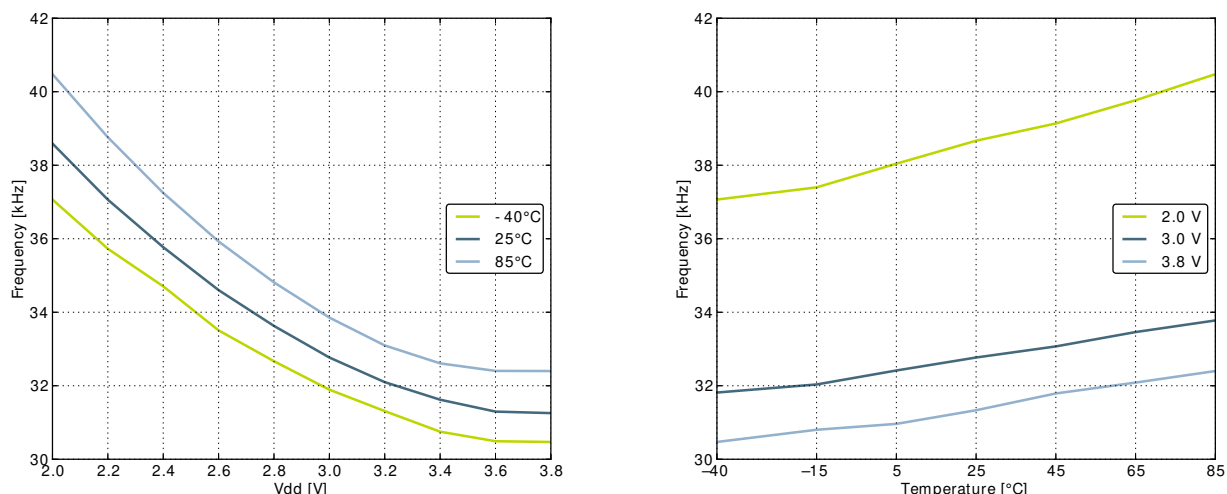
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{HFXO}	Supported nominal crystal Frequency		4		32	MHz
ESR _{HFXO}	Supported crystal equivalent series resistance (ESR)	Crystal frequency 32 MHz		30	60	Ohm
		Crystal frequency 4 MHz		400	1500	Ohm
g _{mHFXO}	The transconductance of the HFXO input transistor at crystal startup	HFXOBOOST in CMU_CTRL equals 0b11	20			mS
C _{HFXOL}	Supported crystal external load range		5		25	pF
I _{HFXO}	Current consumption for HFXO after startup	4 MHz: ESR=400 Ohm, C _L =20 pF, HFXOBOOST in CMU_CTRL equals 0b11		85		μA
		32 MHz: ESR=30 Ohm, C _L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		165		μA
t _{HFXO}	Startup time	32 MHz: ESR=30 Ohm, C _L =10 pF, HFXOBOOST in CMU_CTRL equals 0b11		400		μs

3.9.3 LFRCO

Table 3.10. LFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LFRCO}	Oscillation frequency, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$		31.29	32.768	34.24	kHz
t_{LFRCO}	Startup time not including software calibration			150		μs
I_{LFRCO}	Current consumption			210	380	nA
TUNESTEP _{LFRCO}	Frequency step for LSB change in TUNING value			1.5		%

Figure 3.10. Calibrated LFRCO Frequency vs Temperature and Supply Voltage



3.9.4 HFRCO

Table 3.11. HFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HFRCO}	Oscillation frequency, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	28 MHz frequency band	27.16	28.0	28.84	MHz
		21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40 ¹	6.60 ¹	6.80 ¹	MHz
		1 MHz frequency band	1.16 ²	1.20 ²	1.24 ²	MHz
$t_{HFRCO_settling}$	Settling time after start-up	$f_{HFRCO} = 14\text{ MHz}$		0.6		Cycles
I_{HFRCO}	Current consumption (Production test condition = 14 MHz)	$f_{HFRCO} = 28\text{ MHz}$		160	190	μA
		$f_{HFRCO} = 21\text{ MHz}$		125	155	μA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		$f_{\text{HFRCO}} = 14 \text{ MHz}$		104	120	μA
		$f_{\text{HFRCO}} = 11 \text{ MHz}$		94	110	μA
		$f_{\text{HFRCO}} = 6.6 \text{ MHz}$		63	90	μA
		$f_{\text{HFRCO}} = 1.2 \text{ MHz}$		22	32	μA
TUNESTEP _{H-FRCO}	Frequency step for LSB change in TUNING value			0.3 ³		%

¹For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

²For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

³The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

Figure 3.11. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

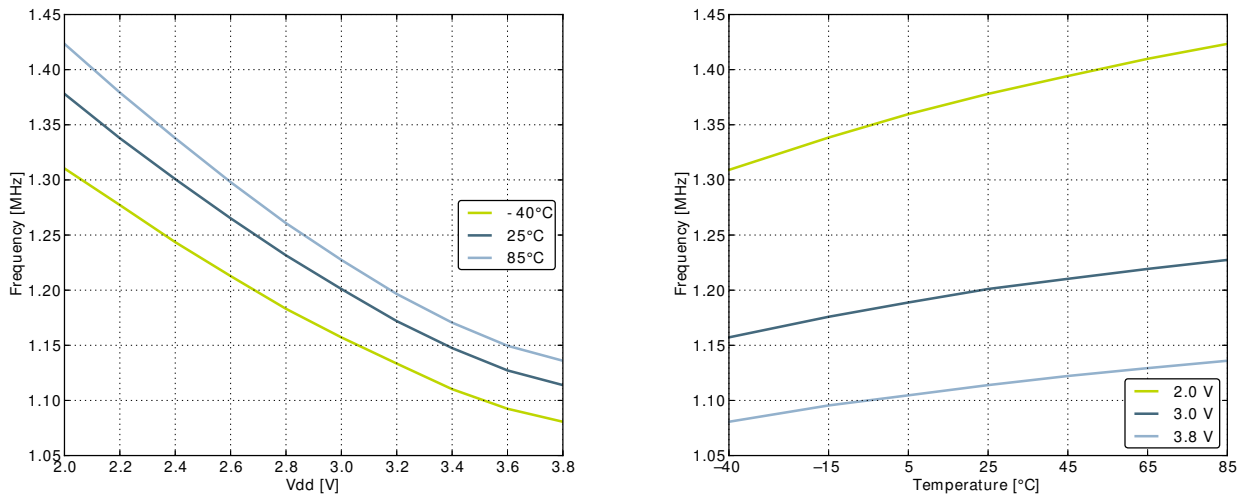


Figure 3.12. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature

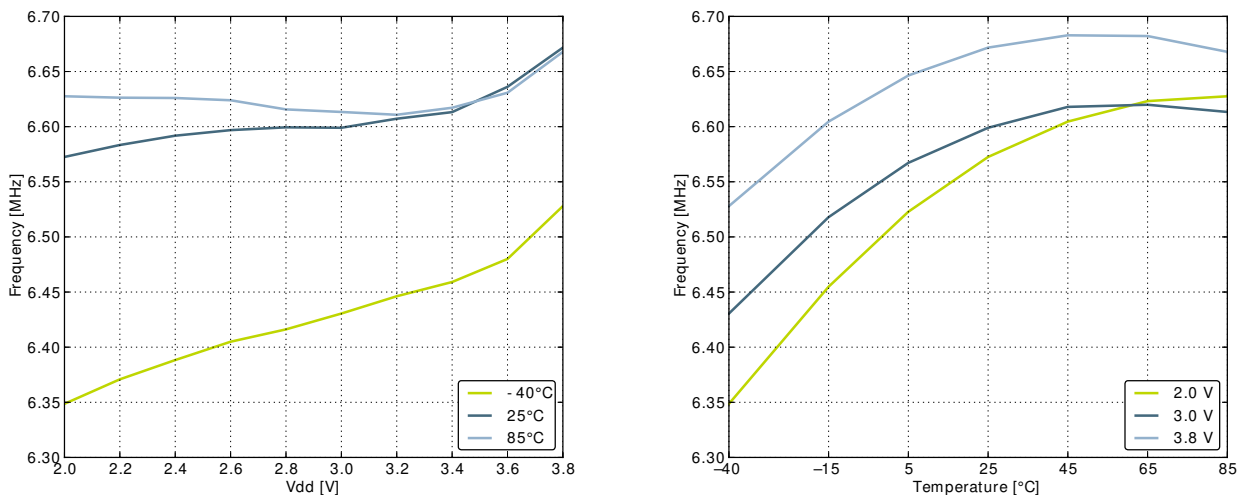


Figure 3.13. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature

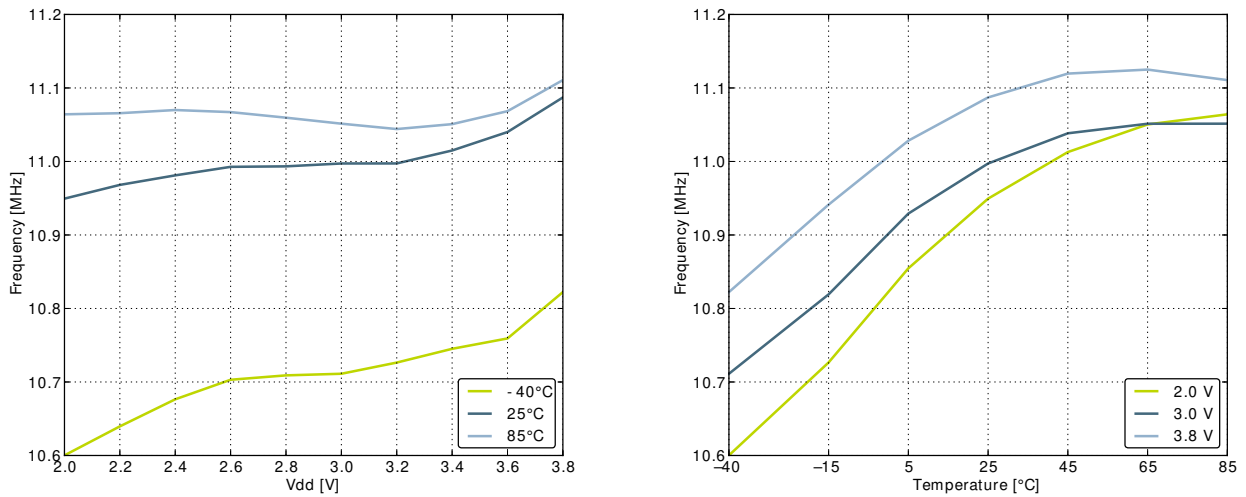


Figure 3.14. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature

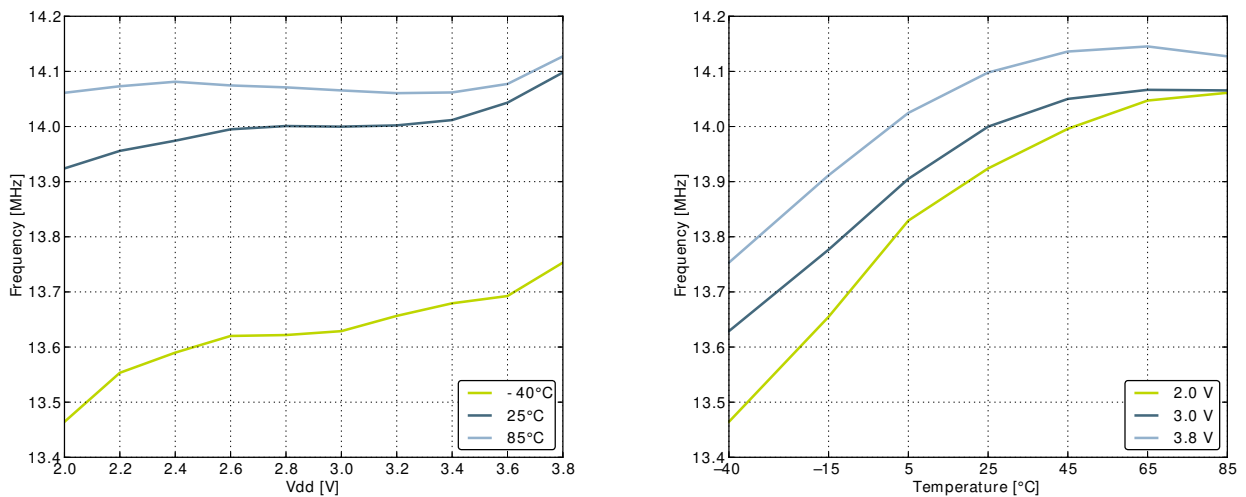


Figure 3.15. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature

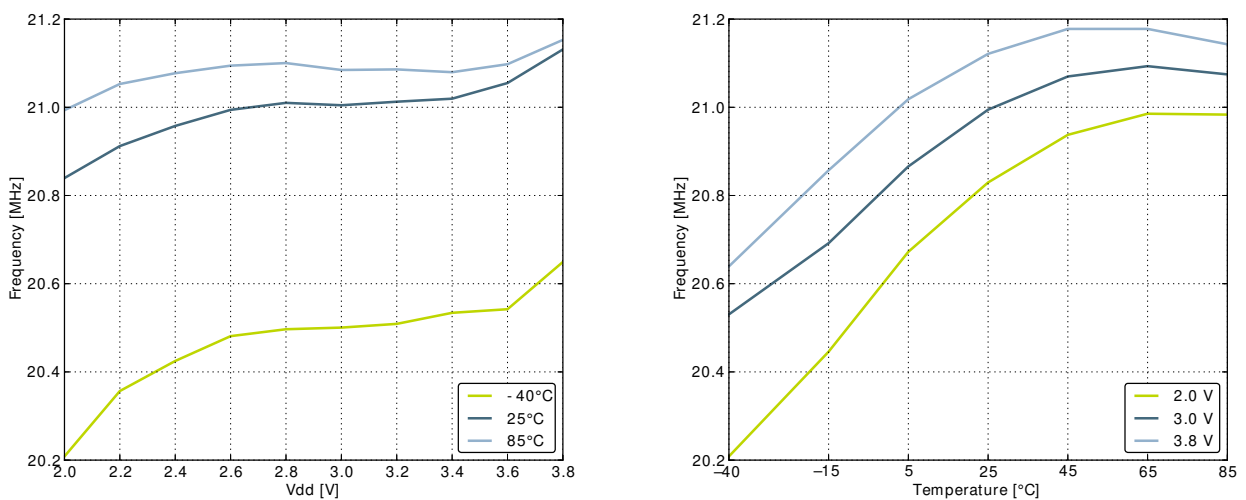
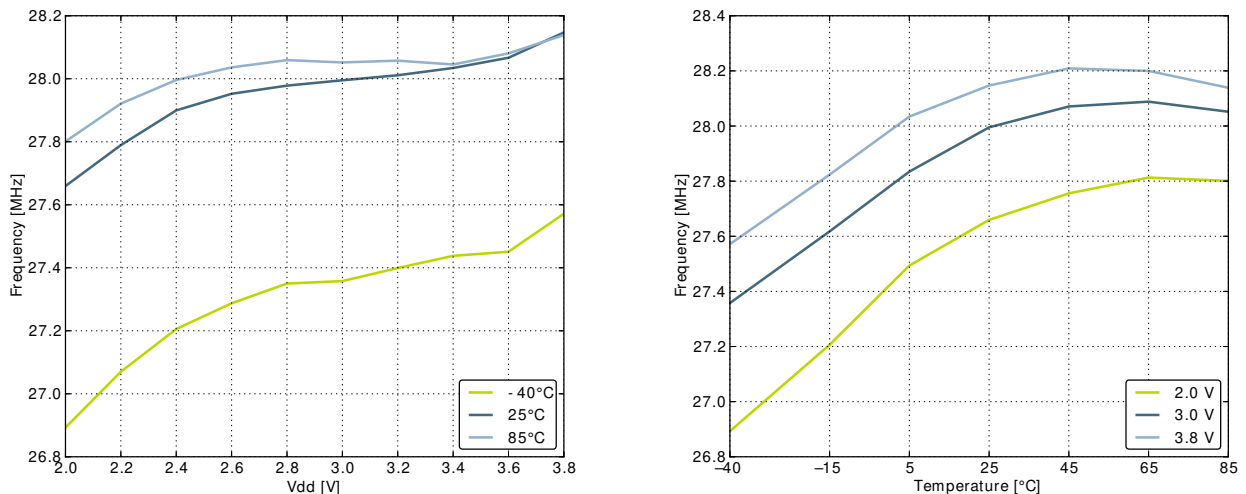


Figure 3.16. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature



3.9.5 AUXHFRCO

Table 3.12. AUXHFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{AUXHFRCO}$	Oscillation frequency, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	28 MHz frequency band	27.16	28.0	28.84	MHz
		21 MHz frequency band	20.37	21.0	21.63	MHz
		14 MHz frequency band	13.58	14.0	14.42	MHz
		11 MHz frequency band	10.67	11.0	11.33	MHz
		7 MHz frequency band	6.40 ¹	6.60 ¹	6.80 ¹	MHz
		1 MHz frequency band	1.16 ²	1.20 ²	1.24 ²	MHz
$t_{AUXHFRCO_settling}$	Settling time after start-up	$f_{AUXHFRCO} = 14\text{ MHz}$		0.6		Cycles
$TUNESTEP_{AUXHFRCO}$	Frequency step for LSB change in TUNING value			0.3 ³		%

¹For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.

²For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.

³The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

3.9.6 ULFRCO

Table 3.13. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ULFRCO}	Oscillation frequency	25°C, 3V	0.70		1.75	kHz
TC_{ULFRCO}	Temperature coefficient			0.05		%/°C
VC_{ULFRCO}	Supply voltage coefficient			-18.2		%/V