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# EFM<sup>®</sup>32

... the world's most energy friendly microcontrollers

## EFM32ZG110 DATASHEET

F32/F16/F8/F4

- **ARM Cortex-M0+ CPU platform**
  - High Performance 32-bit processor @ up to 24 MHz
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 20 nA @ 3 V Shutoff Mode
  - 0.5  $\mu$ A @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.9  $\mu$ A @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 48  $\mu$ A/MHz @ 3 V Sleep Mode
  - 114  $\mu$ A/MHz @ 3 V Run Mode, with code executed from flash
- **32/16/8/4 KB Flash**
- **4/4/2/2 KB RAM**
- **17 General Purpose I/O pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 11 asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **4 Channel DMA Controller**
- **4 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Hardware AES with 128-bit keys in 54 cycles**
- **Timers/Counters**
  - 2x 16-bit Timer/Counter
    - 2x3 Compare/Capture/PWM channels
  - 1x 24-bit Real-Time Counter
  - 1x 16-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- **Communication interfaces**
  - Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
    - Triple buffered full/half-duplex operation
  - Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - I<sup>2</sup>C Interface with SMBus support
    - Address recognition in Stop Mode
- **Ultra low power precision analog peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - 2 single ended channels/ differential channels
    - On-chip temperature sensor
  - Current Digital to Analog Converter
    - Selectable current range between 0.05 and 64  $\mu$ A
  - 1x Analog Comparator
    - Capacitive sensing with up to 2 inputs
  - Supply Voltage Comparator
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **2-pin Serial Wire Debug interface**
- **Pre-Programmed UART Bootloader**
- **Temperature range -40 to 85 °C**
- **Single power supply 1.98 to 3.8 V**
- **QFN24 package**

32-bit ARM Cortex-M0+, Cortex-M3 and Cortex-M4 microcontrollers for:

- Energy, gas, water and smart metering
- Health and fitness applications
- Smart accessories
- Alarm and security systems
- Industrial and home automation



# 1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32ZG110 devices.

**Table 1.1. Ordering Information**

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32ZG110F4-QFN24	4	2	24	1.98 - 3.8	-40 - 85	QFN24
EFM32ZG110F8-QFN24	8	2	24	1.98 - 3.8	-40 - 85	QFN24
EFM32ZG110F16-QFN24	16	4	24	1.98 - 3.8	-40 - 85	QFN24
EFM32ZG110F32-QFN24	32	4	24	1.98 - 3.8	-40 - 85	QFN24

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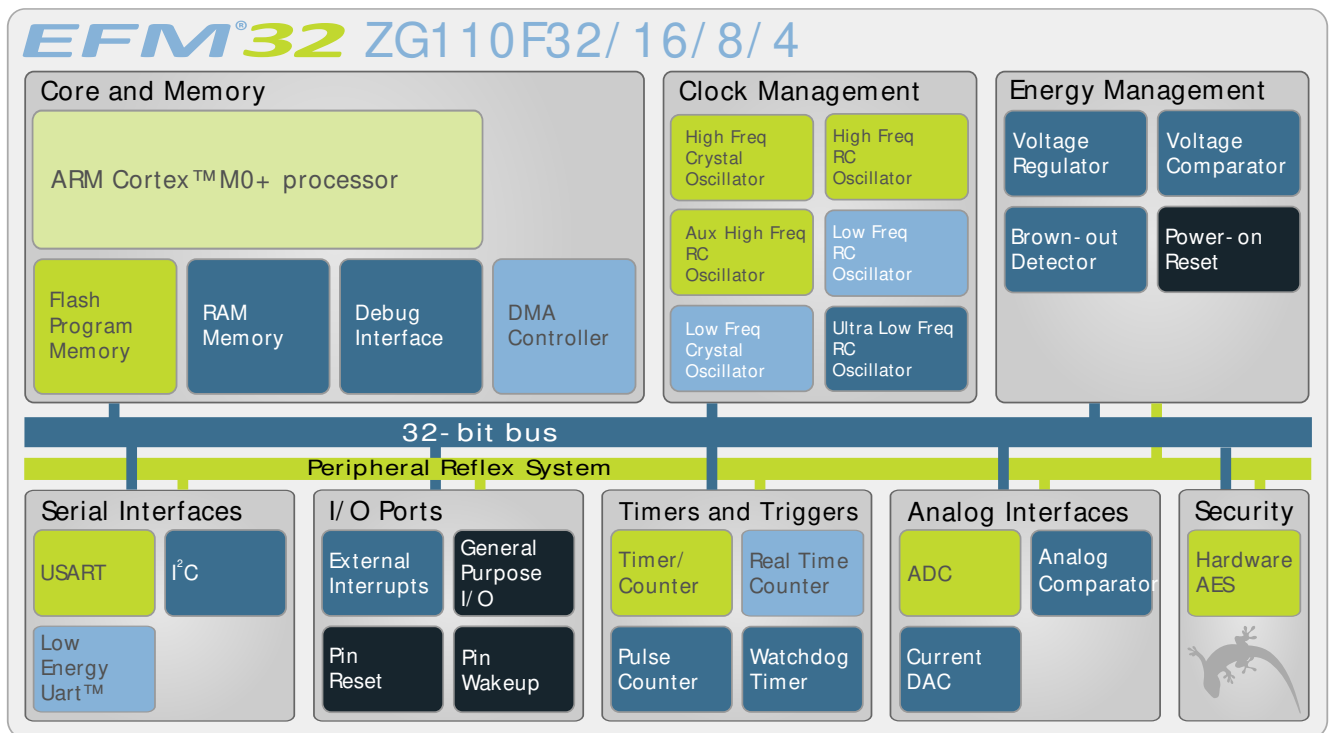
## 2 System Summary

### 2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0+, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32ZG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32ZG110 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32ZG Reference Manual*.

A block diagram of the EFM32ZG110 is shown in Figure 2.1 (p. 3) .

**Figure 2.1. Block Diagram**



#### 2.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

#### 2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface .

#### 2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32ZG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

## 2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230  $\mu$ DMA controller licensed from ARM.

## 2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32ZG.

## 2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32ZG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

## 2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32ZG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

## 2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

## 2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

## 2.1.10 Inter-Integrated Circuit Interface (I2C)

The I<sup>2</sup>C module provides an interface between the MCU and a serial I<sup>2</sup>C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I<sup>2</sup>C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

## 2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

### 2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

### 2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART<sup>™</sup>, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

### 2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output.

### 2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

### 2.1.16 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn\_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

### 2.1.17 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.18 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.19 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 2 external pins and 6 internal signals.

### 2.1.20 Current Digital to Analog Converter (IDAC)

The current digital to analog converter can source or sink a configurable constant current, which can be output on, or sinked from pin or ADC. The current is configurable with several ranges of various step sizes.

## 2.1.21 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

## 2.1.22 General Purpose Input/Output (GPIO)

In the EFM32ZG110, there are 17 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 11 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

## 2.2 Configuration Summary

The features of the EFM32ZG110 is a subset of the feature set described in the EFM32ZG Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

**Table 2.1. Configuration Summary**

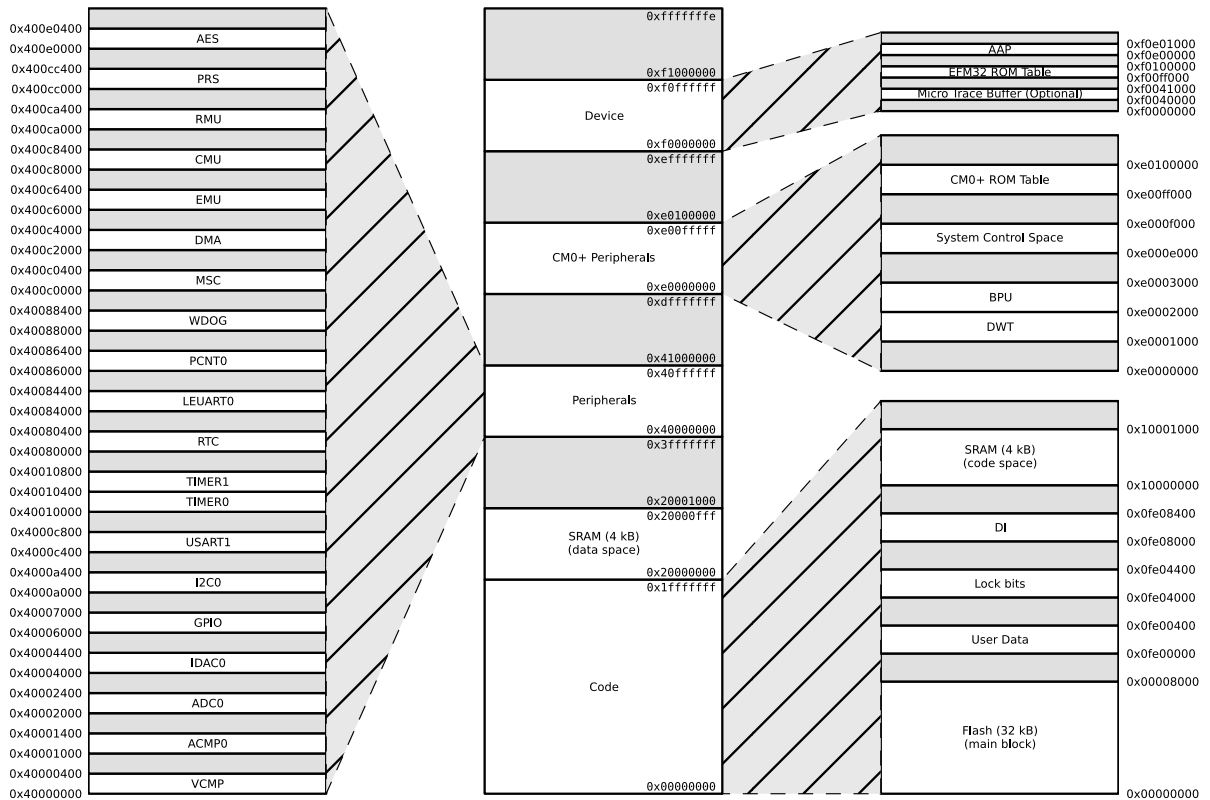
Module	Configuration	Pin Connections
Cortex-M0+	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO,
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
USART1	Full configuration with I2S and IrDA	US1_TX, US1_RX, US1_CLK, US1_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
TIMER0	Full configuration	TIM0_CC[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
RTC	Full configuration	NA
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
ACMP0	Full configuration	ACMP0_CH[1:0], ACMP0_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[1:0]
IDAC0	Full configuration	IDAC0_OUT
AES	Full configuration	NA

Module	Configuration	Pin Connections
GPIO	17 pins	Available pins are shown in Table 4.3 (p. 54)

## 2.3 Memory Map

The EFM32ZG110 memory map is shown in Figure 2.2 (p. 7), with RAM and Flash sizes for the largest memory configuration.

**Figure 2.2. EFM32ZG110 Memory Map with largest RAM and Flash sizes**





## 3 Electrical Characteristics

### 3.1 Test Conditions

#### 3.1.1 Typical Values

The typical data are based on  $T_{AMB}=25^{\circ}\text{C}$  and  $V_{DD}=3.0\text{ V}$ , as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

#### 3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

### 3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8).

**Table 3.1. Absolute Maximum Ratings**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$T_{STG}$	Storage temperature range		-40		150 <sup>1</sup>	$^{\circ}\text{C}$
$T_S$	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	$^{\circ}\text{C}$
$V_{DDMAX}$	External main supply voltage		0		3.8	V
$V_{IOPIN}$	Voltage on any I/O pin		-0.3		$V_{DD}+0.3$	V

<sup>1</sup>Based on programmed devices tested for 10000 hours at 150 $^{\circ}\text{C}$ . Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

### 3.3 General Operating Conditions

#### 3.3.1 General Operating Conditions

**Table 3.2. General Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Unit
$T_{AMB}$	Ambient temperature range	-40		85	$^{\circ}\text{C}$
$V_{DDOP}$	Operating supply voltage	1.98		3.8	V
$f_{APB}$	Internal APB clock frequency			24	MHz
$f_{AHB}$	Internal AHB clock frequency			24	MHz

### 3.4 Current Consumption

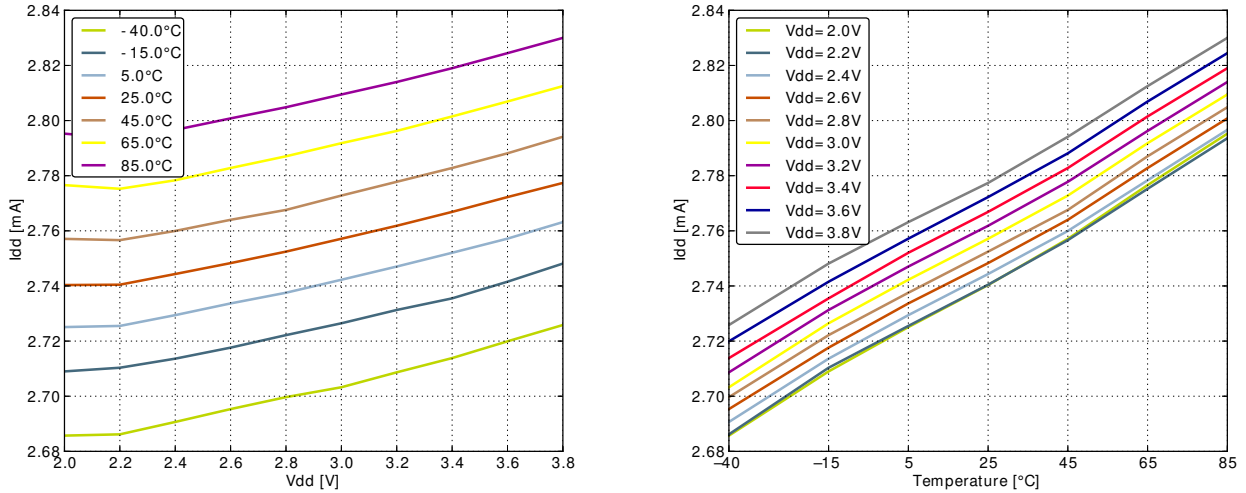
**Table 3.3. Current Consumption**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I <sub>EM0</sub>	EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	24 MHz HFXO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		115	132	μA/MHz
		24 MHz HFXO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		117	136	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		114	128	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		116	132	μA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		117	131	μA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		118	133	μA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		118	133	μA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		120	135	μA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		124	139	μA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		125	142	μA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		155	177	μA/MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		162	181	μA/MHz
I <sub>EM1</sub>	EM1 current (Production test condition = 14 MHz)	24 MHz HFXO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		48	57	μA/MHz
		24 MHz HFXO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		49	59	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		48	52	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		49	53	μA/MHz

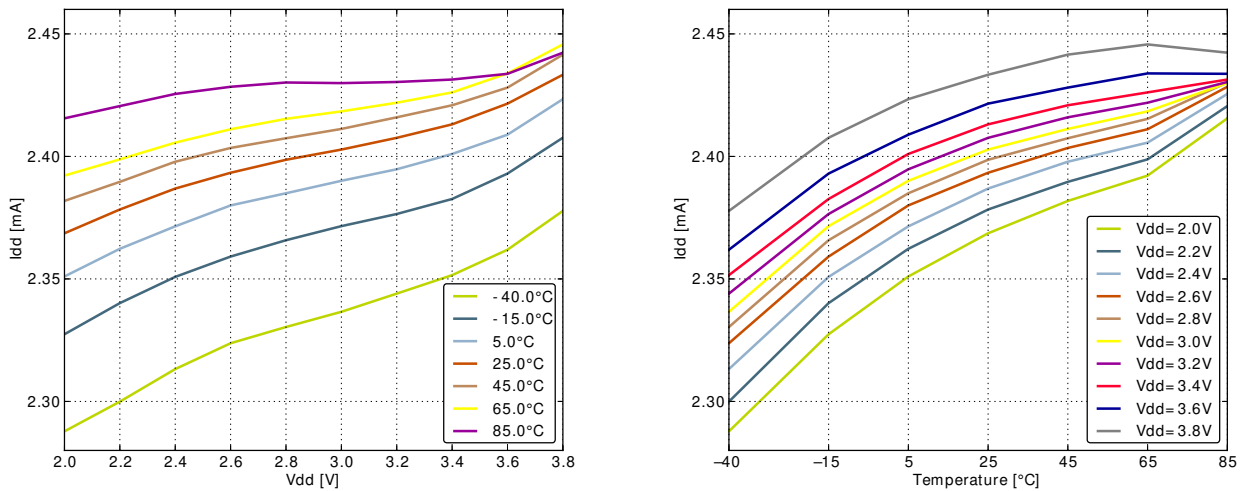
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		14 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		50	54	µA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		51	56	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		52	56	µA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		53	58	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		57	63	µA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		59	66	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		89	99	µA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		92	103	µA/MHz
I <sub>EM2</sub>	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		0.9	1.25	µA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		1.7	2.35	µA
I <sub>EM3</sub>	EM3 current	EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		0.5	0.9	µA
		EM3 current (ULFRCO enabled, LFRCO/LFXO disabled), V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		1.3	2.0	µA
I <sub>EM4</sub>	EM4 current	V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =25°C		0.02	0.035	µA
		V <sub>DD</sub> = 3.0 V, T <sub>AMB</sub> =85°C		0.29	0.700	µA

### 3.4.1 EM0 Current Consumption

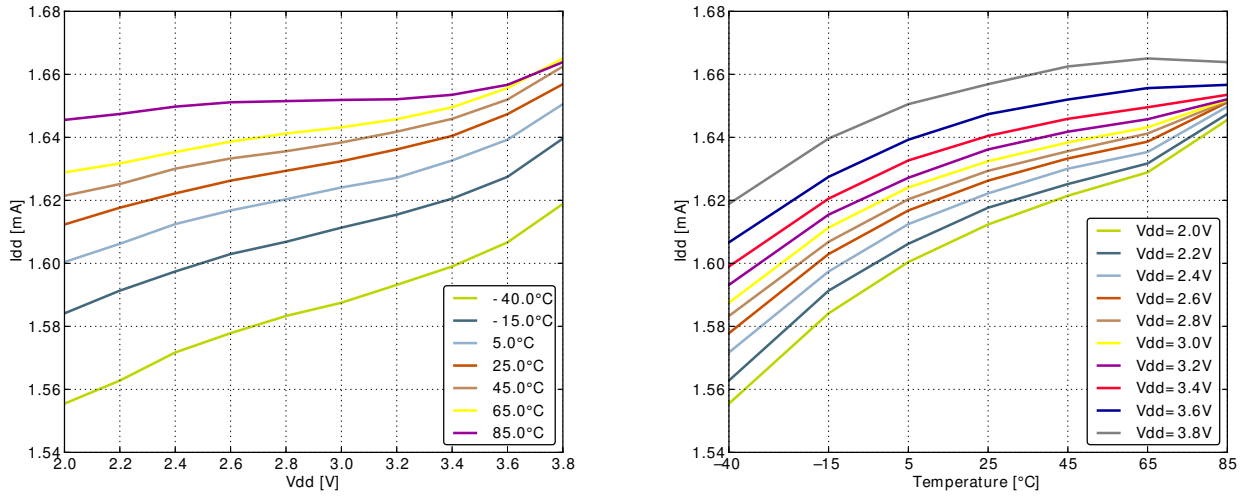
**Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 24 MHz**



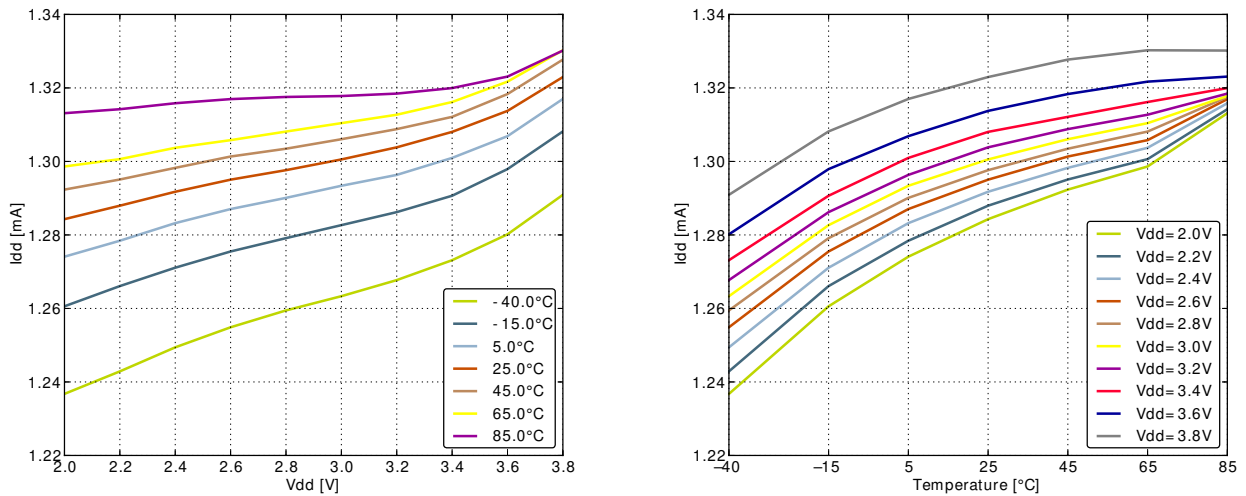
**Figure 3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21 MHz**



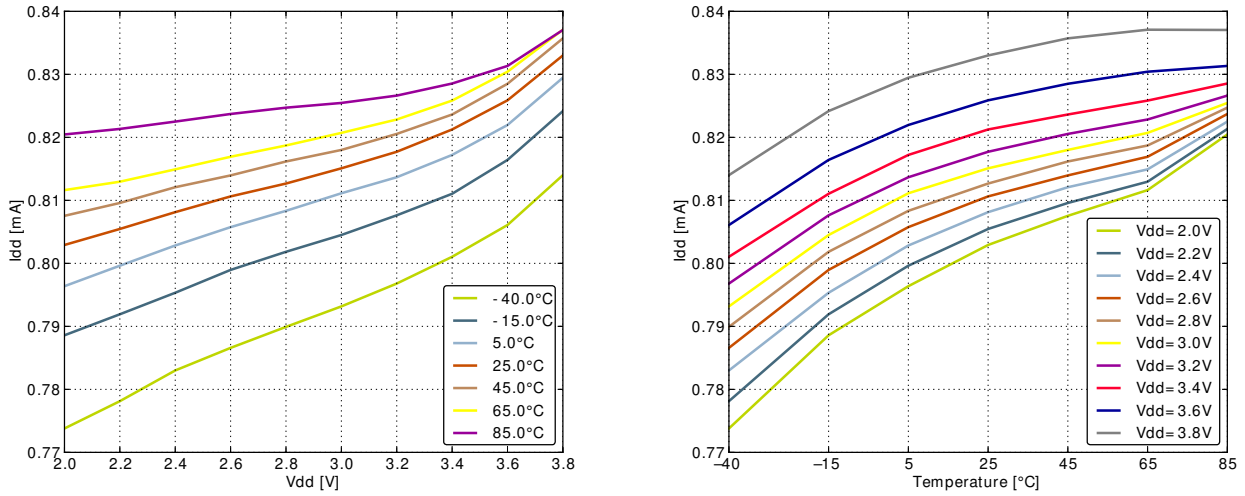
**Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14 MHz**



**Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11 MHz**

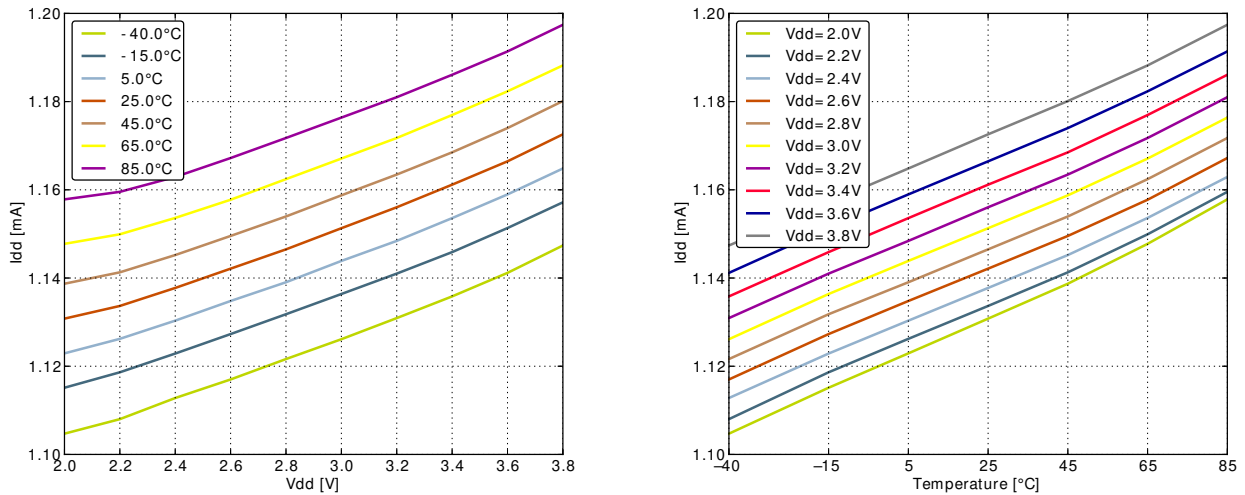


**Figure 3.5. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 6.6 MHz**

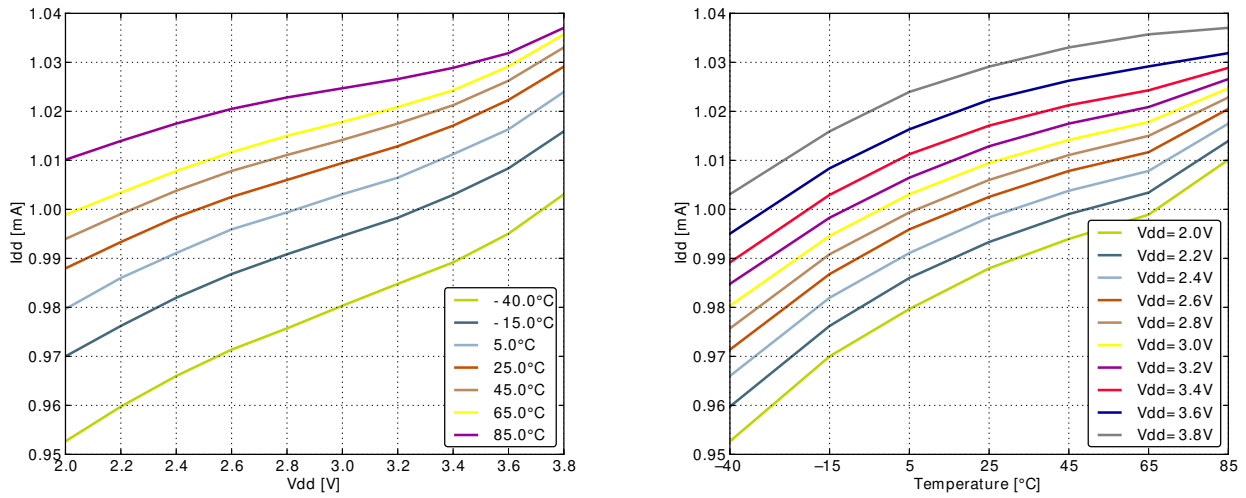


### 3.4.2 EM1 Current Consumption

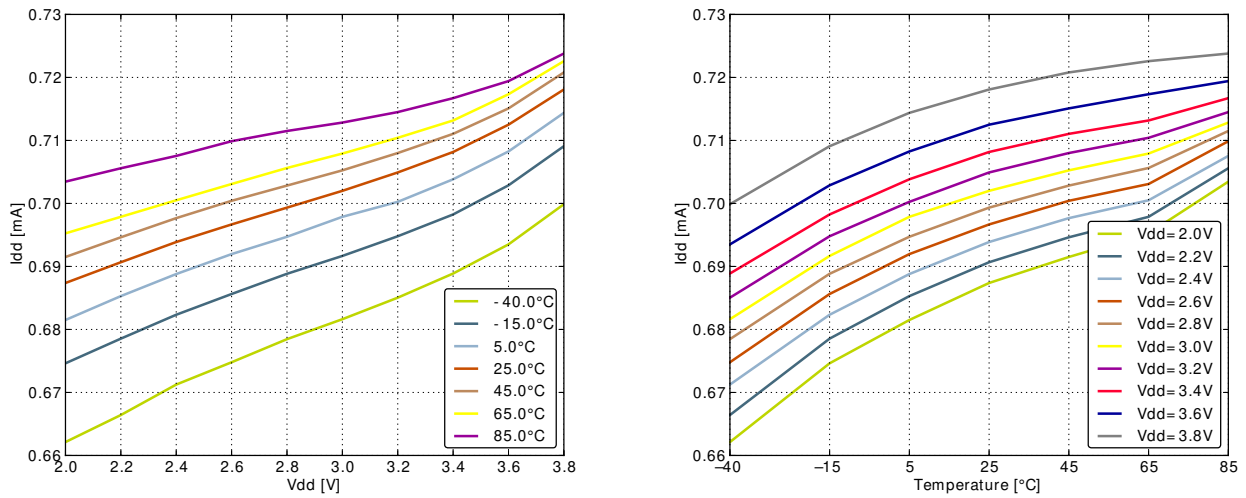
**Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 24 MHz**



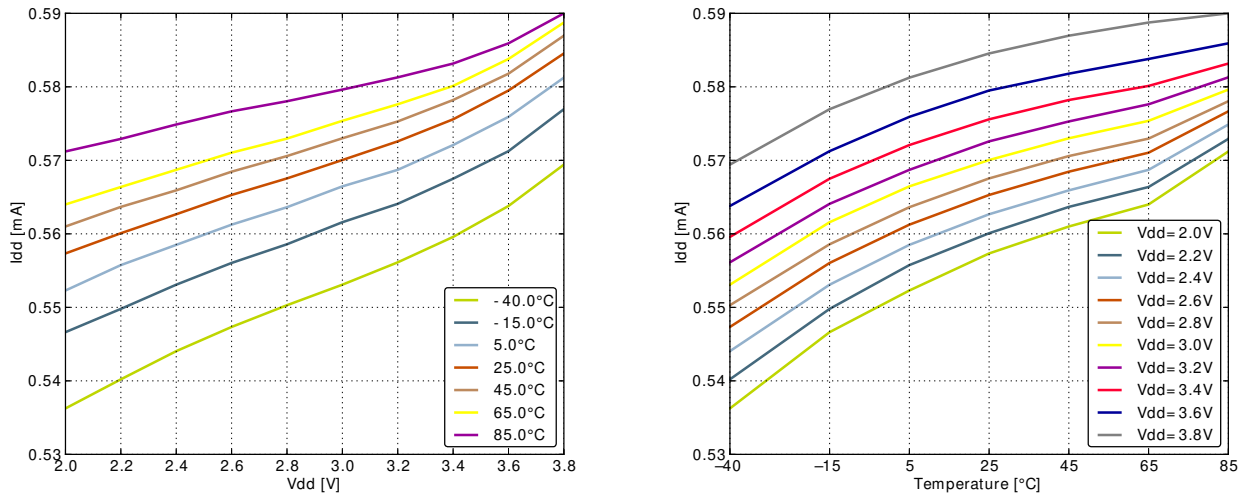
**Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21 MHz**



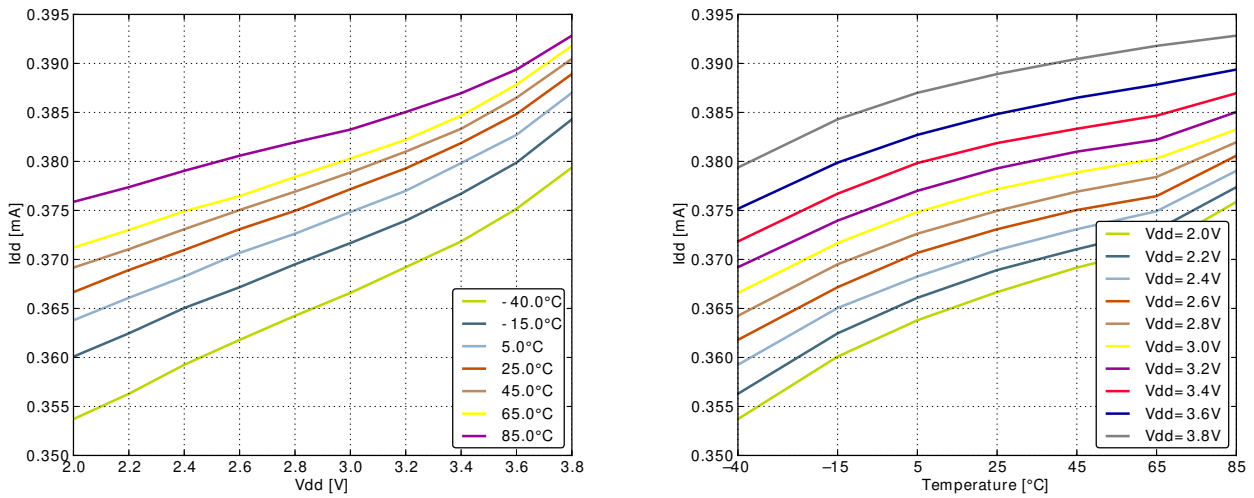
**Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14 MHz**



**Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11 MHz**



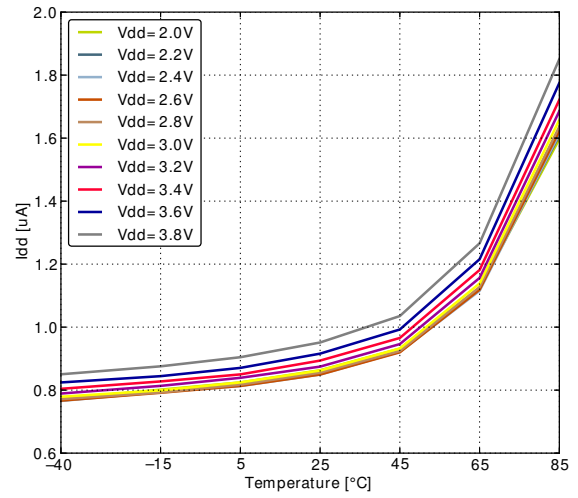
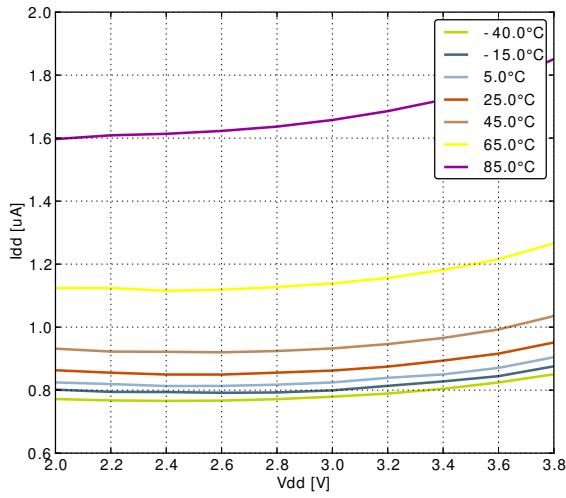
**Figure 3.10. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6 MHz**





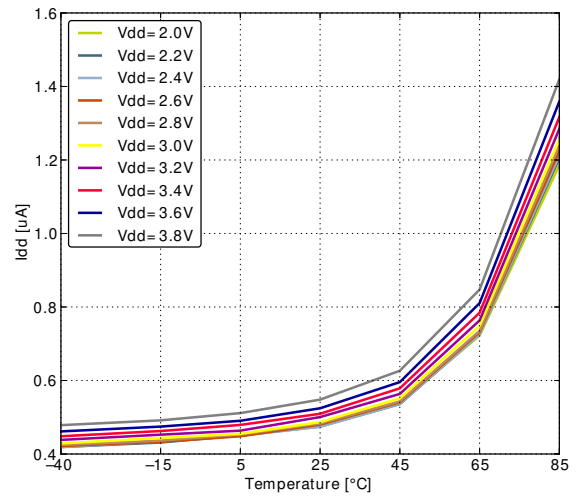
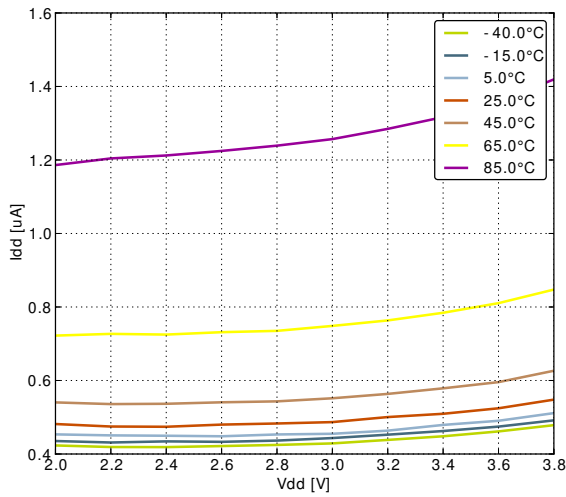
### 3.4.3 EM2 Current Consumption

Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.



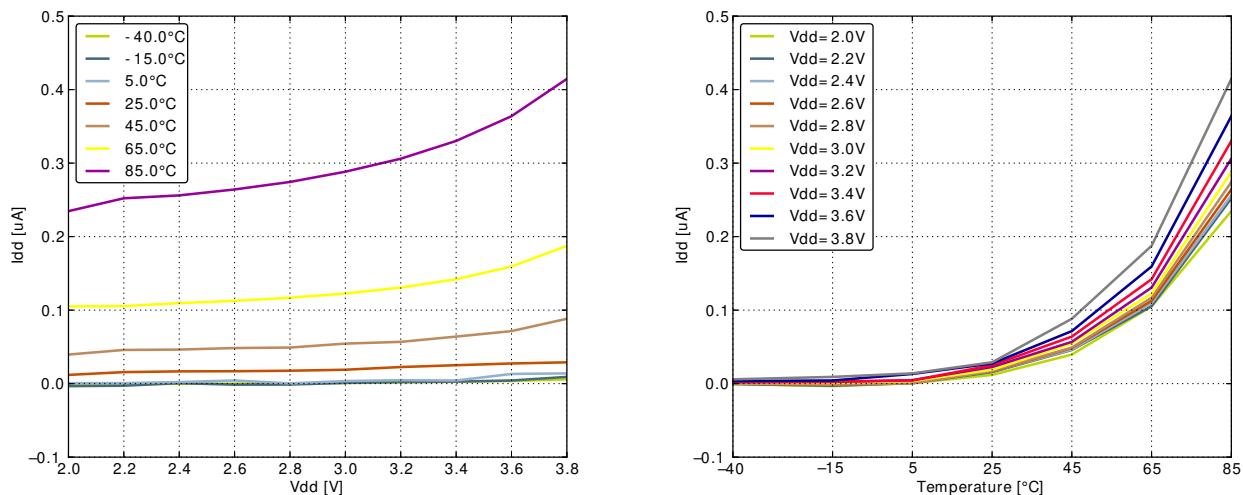
### 3.4.4 EM3 Current Consumption

Figure 3.12. EM3 current consumption.



### 3.4.5 EM4 Current Consumption

Figure 3.13. EM4 current consumption.



## 3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.4. Energy Modes Transitions

Symbol	Parameter	Min	Typ	Max	Unit
$t_{EM10}$	Transition time from EM1 to EM0		0		HF-CORE-CLK cycles
$t_{EM20}$	Transition time from EM2 to EM0		2		$\mu$ s
$t_{EM30}$	Transition time from EM3 to EM0		2		$\mu$ s
$t_{EM40}$	Transition time from EM4 to EM0		163		$\mu$ s

## 3.6 Power Management

The EFM32ZG requires the AVDD\_x, VDD\_DREG and IOVDD\_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

**Table 3.5. Power Management**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>BODextthr-</sub>	BOD threshold on falling external supply voltage		1.74		1.96	V
V <sub>BODextthr+</sub>	BOD threshold on rising external supply voltage			1.85		V
t <sub>RESET</sub>	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C <sub>DECOUPLE</sub>	Voltage regulator decoupling capacitor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF

## 3.7 Flash

**Table 3.6. Flash**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
EC <sub>FLASH</sub>	Flash erase cycles before failure		20000			cycles
RET <sub>FLASH</sub>	Flash data retention	T <sub>AMB</sub> <150°C	10000			h
		T <sub>AMB</sub> <85°C	10			years
		T <sub>AMB</sub> <70°C	20			years
t <sub>W_PROG</sub>	Word (32-bit) programming time		20			μs
t <sub>P_ERASE</sub>	Page erase time		20	20.4	20.8	ms
t <sub>D_ERASE</sub>	Device erase time		40	40.8	41.6	ms
I <sub>ERASE</sub>	Erase current				7 <sup>1</sup>	mA
I <sub>WRITE</sub>	Write current				7 <sup>1</sup>	mA
V <sub>FLASH</sub>	Supply voltage during flash erase and write		1.98		3.8	V

<sup>1</sup>Measured at 25°C

## 3.8 General Purpose Input Output

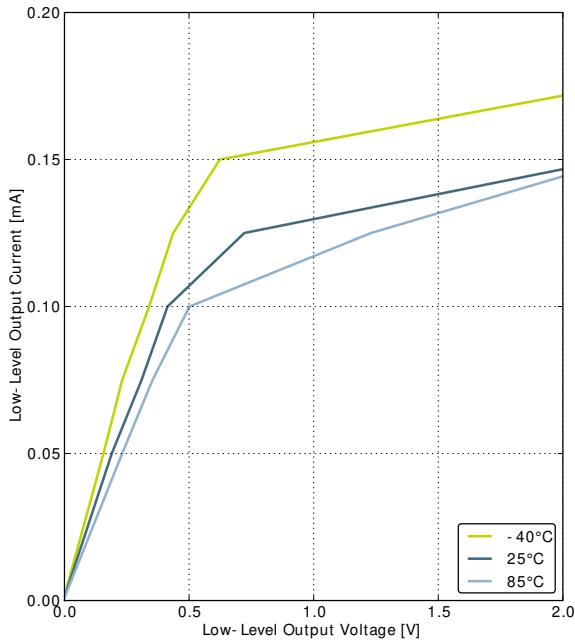
**Table 3.7. GPIO**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>IOIL</sub>	Input low voltage				0.30V <sub>DD</sub>	V
V <sub>IOIH</sub>	Input high voltage		0.70V <sub>DD</sub>			V
V <sub>IOOH</sub>	Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sourcing 0.1 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.80V <sub>DD</sub>		V
		Sourcing 0.1 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.90V <sub>DD</sub>		V

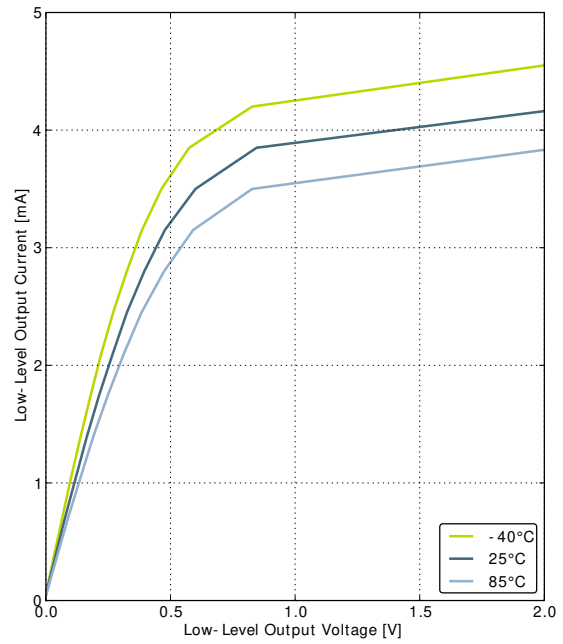
Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Sourcing 1 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.85V <sub>DD</sub>		V
		Sourcing 1 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.90V <sub>DD</sub>		V
		Sourcing 6 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.75V <sub>DD</sub>			V
		Sourcing 6 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD	0.85V <sub>DD</sub>			V
		Sourcing 20 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.60V <sub>DD</sub>			V
		Sourcing 20 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH	0.80V <sub>DD</sub>			V
V <sub>IOOL</sub>	Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	Sinking 0.1 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.20V <sub>DD</sub>		V
		Sinking 0.1 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST		0.10V <sub>DD</sub>		V
		Sinking 1 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.10V <sub>DD</sub>		V
		Sinking 1 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW		0.05V <sub>DD</sub>		V
		Sinking 6 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.30V <sub>DD</sub>	V
		Sinking 6 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD			0.20V <sub>DD</sub>	V
		Sinking 20 mA, V <sub>DD</sub> =1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.35V <sub>DD</sub>	V
		Sinking 20 mA, V <sub>DD</sub> =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.25V <sub>DD</sub>	V
I <sub>IOLEAK</sub>	Input leakage current	High Impedance IO connected to GROUND or V <sub>DD</sub>		±0.1	±100	nA
R <sub>PU</sub>	I/O pin pull-up resistor			40		kOhm
R <sub>PD</sub>	I/O pin pull-down resistor			40		kOhm
R <sub>IOESD</sub>	Internal ESD series resistor			200		Ohm
t <sub>IOGLITCH</sub>	Pulse width of pulses to be removed		10		50	ns

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	by the glitch suppression filter					
t <sub>IOOF</sub>	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capacitance C <sub>L</sub> =12.5-25pF.	20+0.1C <sub>L</sub>		250	ns
		GPIO_Px_CTRL DRIVEMODE = LOW and load capacitance C <sub>L</sub> =350-600pF	20+0.1C <sub>L</sub>		250	ns
V <sub>IOHYST</sub>	I/O pin hysteresis (V <sub>IOTHR+</sub> - V <sub>IOTHR-</sub> )	V <sub>DD</sub> = 1.98 - 3.8 V	0.1V <sub>DD</sub>			V

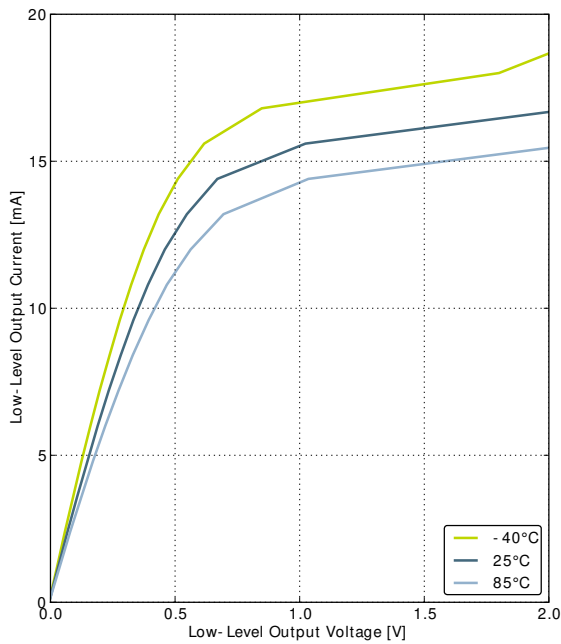
Figure 3.14. Typical Low-Level Output Current, 2V Supply Voltage



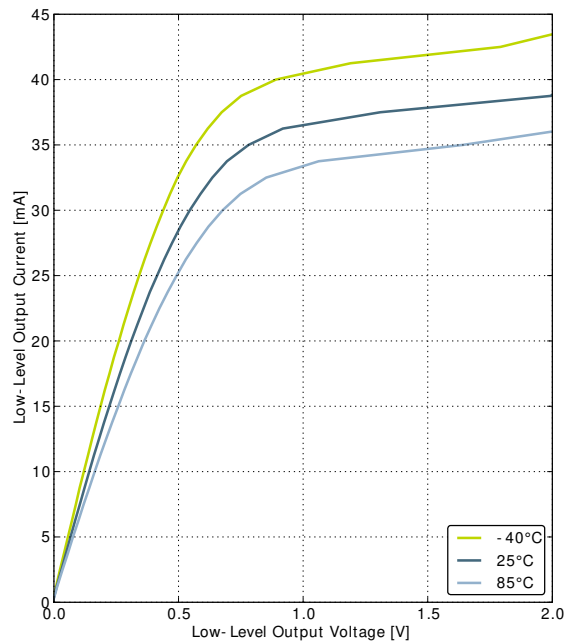
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW

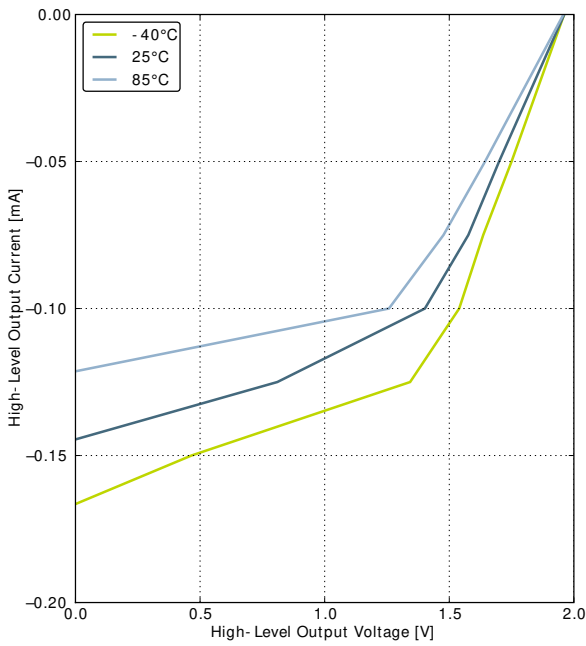


GPIO\_Px\_CTRL DRIVEMODE = STANDARD

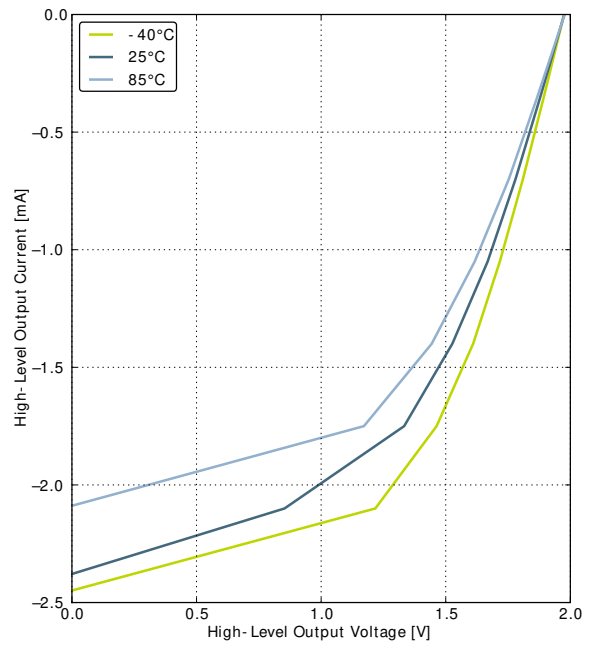


GPIO\_Px\_CTRL DRIVEMODE = HIGH

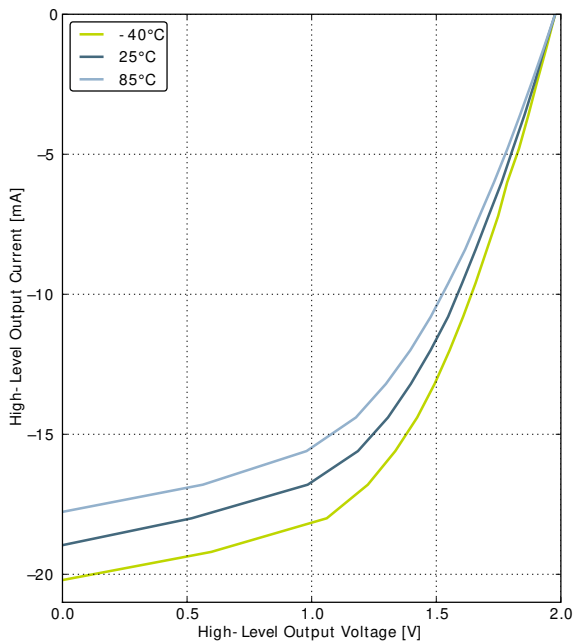
Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage



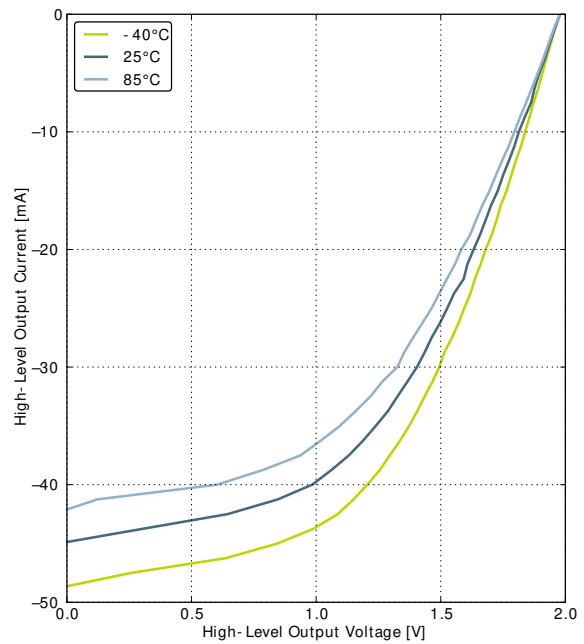
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW

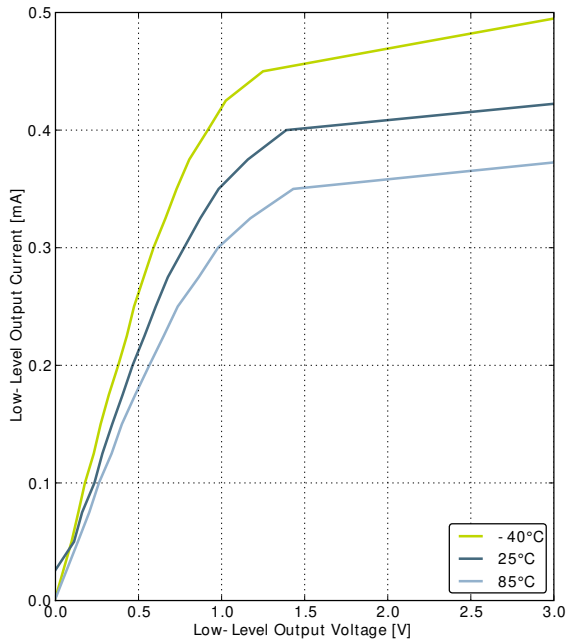


GPIO\_Px\_CTRL DRIVEMODE = STANDARD

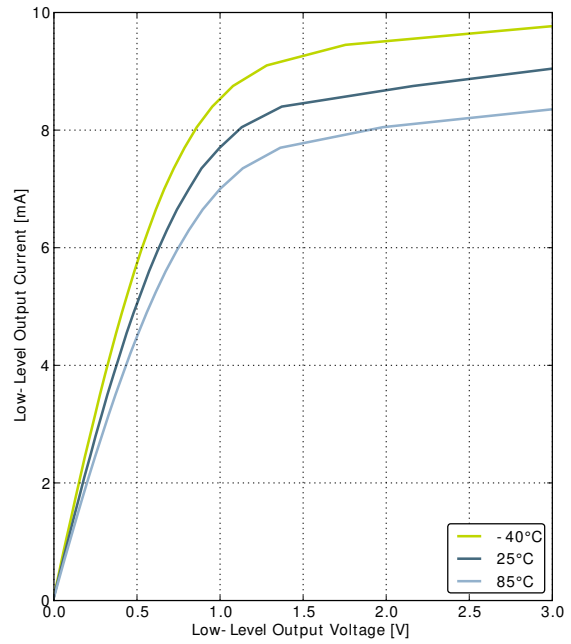


GPIO\_Px\_CTRL DRIVEMODE = HIGH

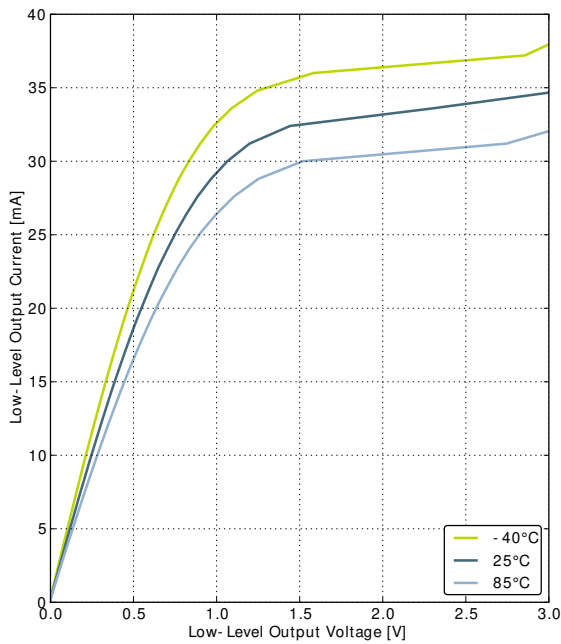
Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage



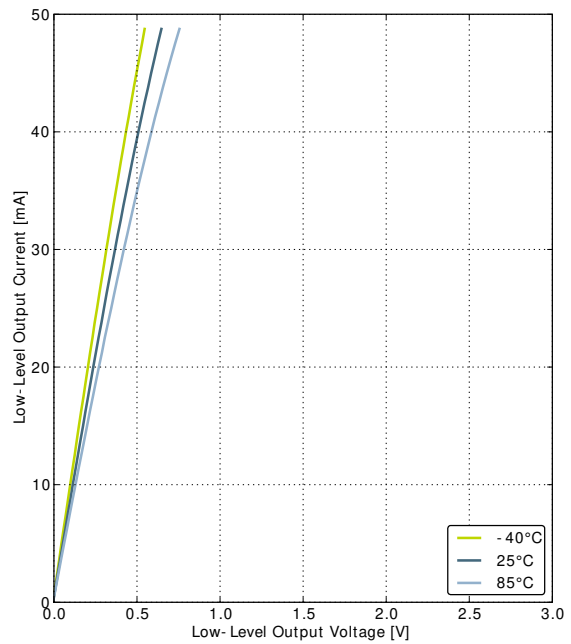
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW



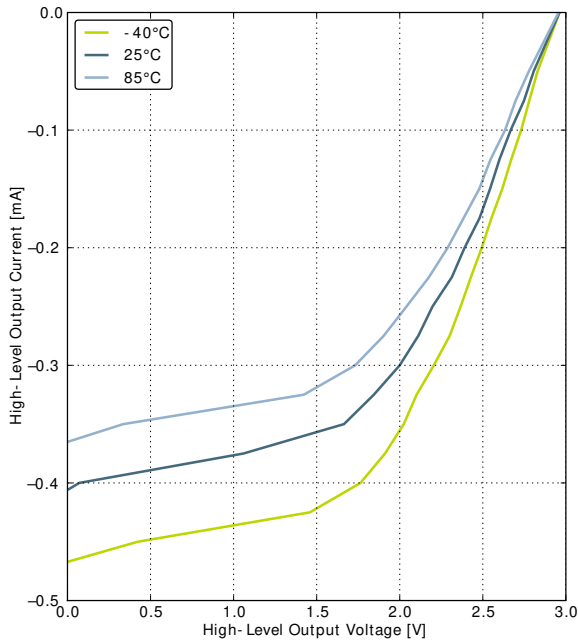
GPIO\_Px\_CTRL DRIVEMODE = STANDARD



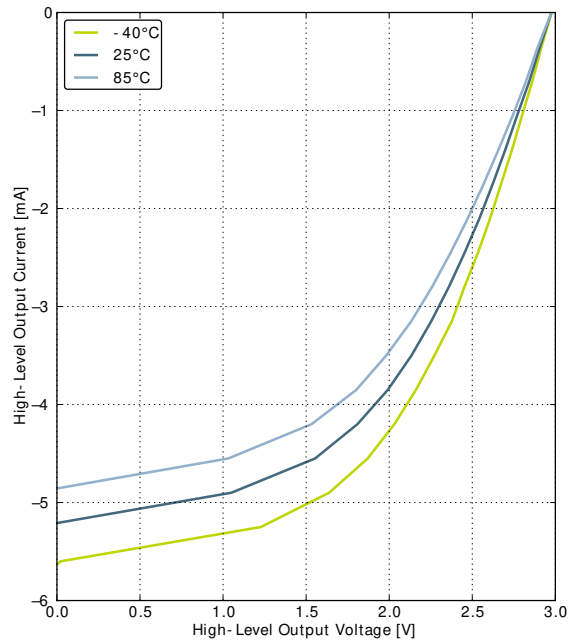
GPIO\_Px\_CTRL DRIVEMODE = HIGH



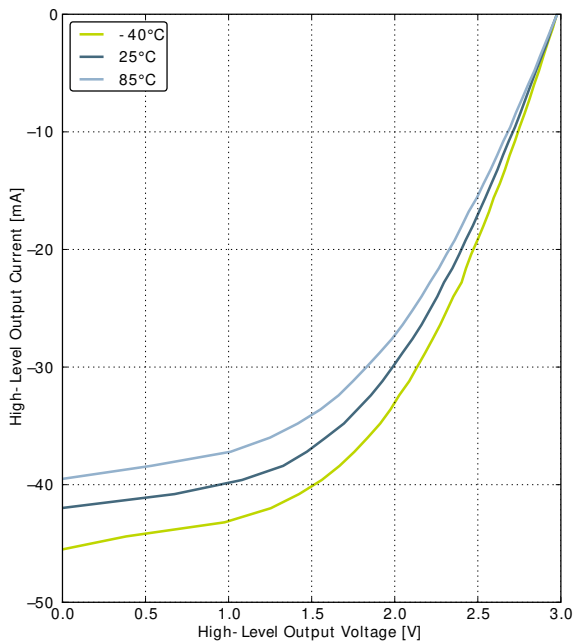
Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage



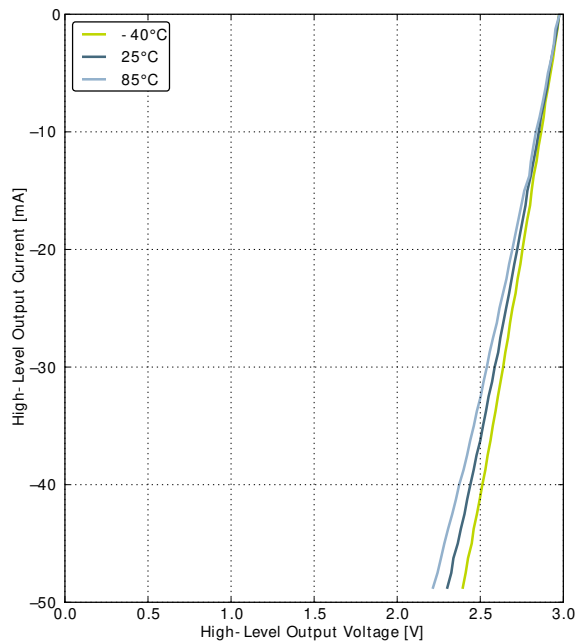
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW

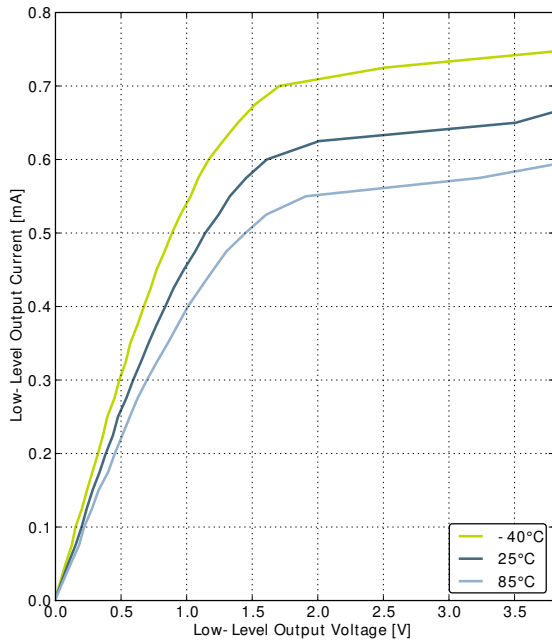


GPIO\_Px\_CTRL DRIVEMODE = STANDARD

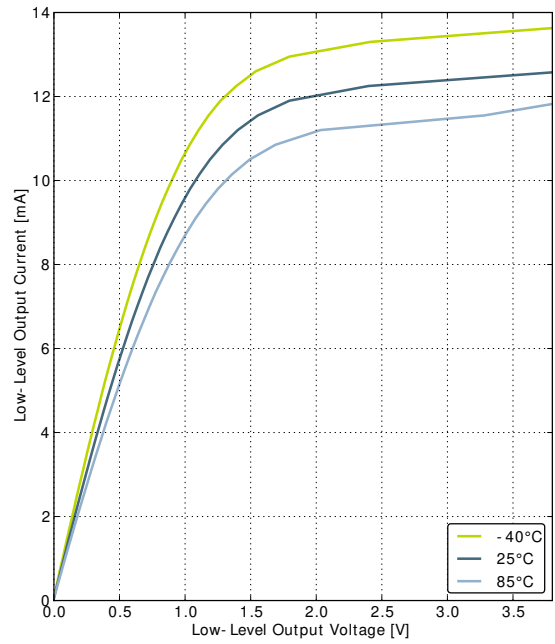


GPIO\_Px\_CTRL DRIVEMODE = HIGH

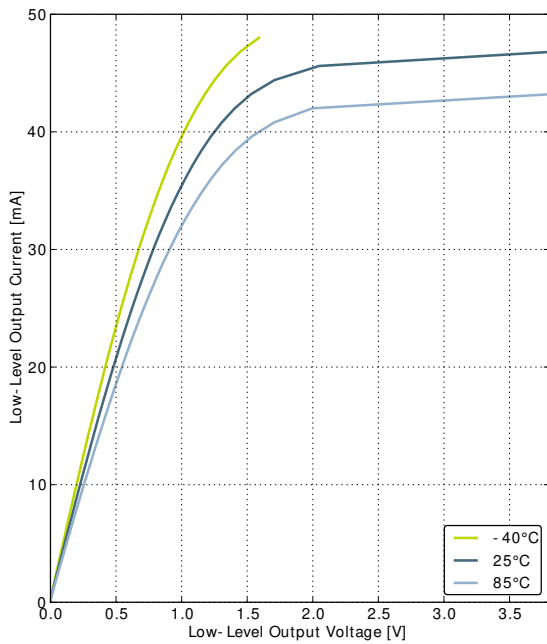
Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage



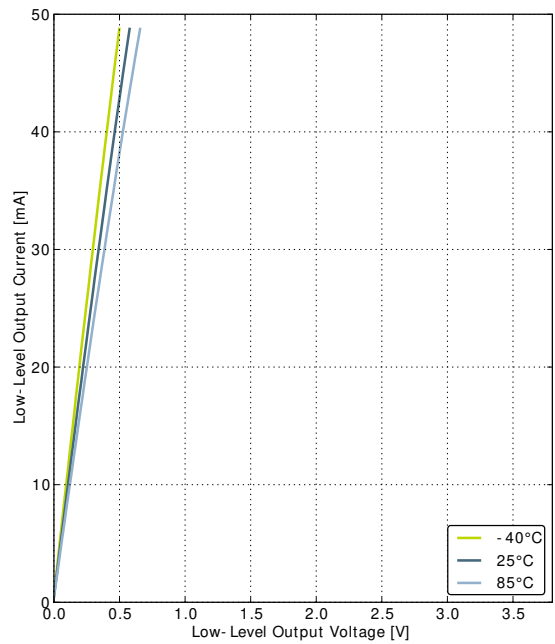
GPIO\_Px\_CTRL DRIVEMODE = LOWEST



GPIO\_Px\_CTRL DRIVEMODE = LOW



GPIO\_Px\_CTRL DRIVEMODE = STANDARD



GPIO\_Px\_CTRL DRIVEMODE = HIGH