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# EFM8 Busy Bee Family

## EFM8BB3 Data Sheet



The EFM8BB3, part of the Busy Bee family of MCUs, is a performance line of 8-bit microcontrollers with a comprehensive analog and digital feature set in small packages.

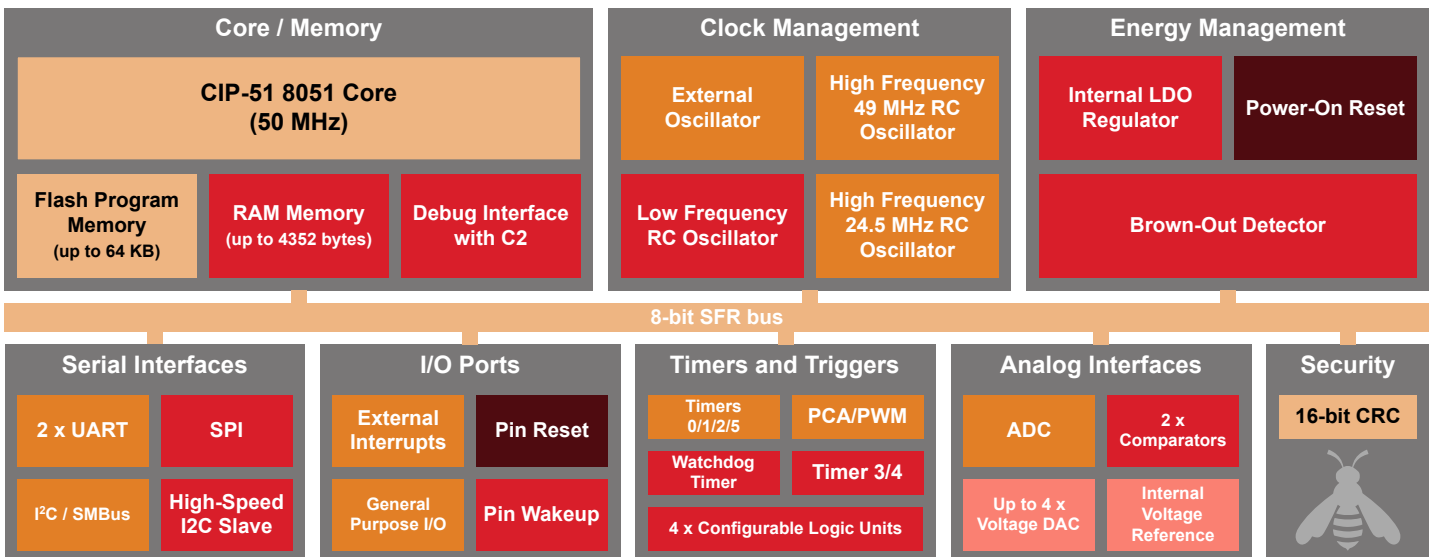
These devices offer state-of-the-art performance by integrating 12-bit ADC, internal temperature sensor, and up to two 12-bit DACs into small packages, making them ideal for general purpose applications. With an efficient, pipelined 8051 core with maximum operating frequency at 50 MHz, various communication interfaces, and four channels of configurable logic, the EFM8BB3 family is optimal for many embedded applications.

EFM8BB3 applications include the following:

- Consumer electronics
- Precision instrumentation
- Power management and control
- Industrial control and automation
- Smart sensors

### KEY FEATURES

- Pipelined 8-bit 8051 MCU Core with 50 MHz operating frequency
- Up to 29 multifunction I/O pins
- One 12-bit/10-bit ADC
- Two 12-bit DACs with synchronization and PWM capabilities
- Two low-current analog comparators with built-in reference DACs
- Internal temperature sensor
- Internal 49 MHz and 24.5 MHz oscillators accurate to  $\pm 2\%$
- Four channels of Configurable Logic
- 6-channel PWM / PCA
- Six 16-bit general-purpose timers



Lowest power mode with peripheral operational:

- Normal
- Idle
- Suspend
- Snooze
- Shutdown

## 1. Feature List

The EFM8BB3 device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 50 MHz maximum operating frequency
- Memory:
  - Up to 64 kB flash memory (63 kB user-accessible), in-system re-programmable from firmware in 512-byte sectors
  - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 29 total multifunction I/O pins:
  - Up to 25 pins 5 V tolerant under bias
  - Selectable state retention through reset events
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 49 MHz oscillator with accuracy of  $\pm 1.5\%$
  - Internal 24.5 MHz oscillator with  $\pm 2\%$  accuracy
  - Internal 80 kHz low-frequency oscillator
  - External CMOS clock option
  - External crystal/RC/C Oscillator (up to 25 MHz)
- Analog:
  - 12/10-Bit Analog-to-Digital Converter (ADC)
  - Internal temperature sensor
  - 2 x 12-Bit Digital-to-Analog Converters (DAC)
  - 2 x Low-current analog comparators with adjustable reference
- Communications and Digital Peripherals:
  - 2 x UART, up to 3 Mbaud
  - SPI™ Master / Slave, up to 12 Mbps
  - SMBus™/I2C™ Master / Slave, up to 400 kbps
  - I<sup>2</sup>C High-Speed Slave, up to 3.4 Mbps
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
  - 4 Configurable Logic Units
- Timers/Counters and PWM:
  - 6-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
  - 6 x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from the low frequency oscillator
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB3 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing nonvolatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Device operation is specified from 2.2 V up to a 3.6 V supply. Devices are AEC-Q100 qualified (pending) and available in 4x4 mm 32-pin QFN, 3x3 mm 24-pin QFN, 32-pin QFP, or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.



## 2. Ordering Information

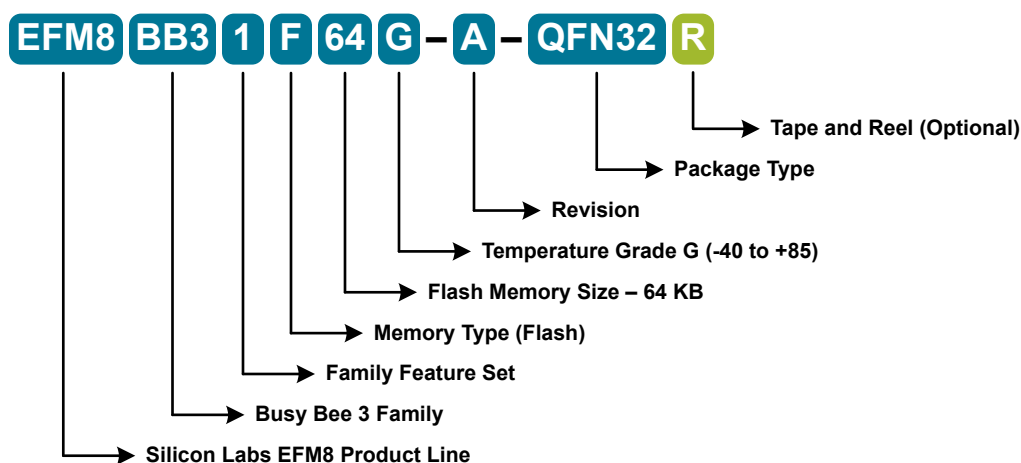


Figure 2.1. EFM8BB3 Part Numbering

All EFM8BB3 family members have the following features:

- CIP-51 Core running up to 49 MHz
- Three Internal Oscillators (49 MHz, 24.5 MHz and 80 kHz)
- SMBus
- I2C Slave
- SPI
- 2 UARTs
- 6-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- Six 16-bit Timers
- Four Configurable Logic Units
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, temperature sensor, channel sequencer, and direct-to-XRAM data transfer
- Two Voltage Digital-to-Analog Converters (DACs)
- Two Analog Comparators
- 16-bit CRC Unit
- AEC-Q100 qualified (pending)

In addition to these features, each part number in the EFM8BB3 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Number of DACs	ADC Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-A-QFN32	64	4352	29	4	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F64G-A-QFP32	64	4352	28	4	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F64G-A-QFN24	64	4352	20	4	12	6	6	Yes	-40 to +85 °C	QFN24

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Number of DACs	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB31F64G-A-QSOP24	64	4352	21	4	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F32G-A-QFN32	32	2304	29	2	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F32G-A-QFP32	32	2304	28	2	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F32G-A-QFN24	32	2304	20	2	12	6	6	Yes	-40 to +85 °C	QFN24
EFM8BB31F32G-A-QSOP24	32	2304	21	2	13	6	7	Yes	-40 to +85 °C	QSOP24
EFM8BB31F16G-A-QFN32	16	2304	29	2	20	10	9	Yes	-40 to +85 °C	QFN32
EFM8BB31F16G-A-QFP32	16	2304	28	2	20	10	9	Yes	-40 to +85 °C	QFP32
EFM8BB31F16G-A-QSOP24	16	2304	21	2	13	6	7	Yes	-40 to +85 °C	QSOP24

### 3. System Overview

#### 3.1 Introduction

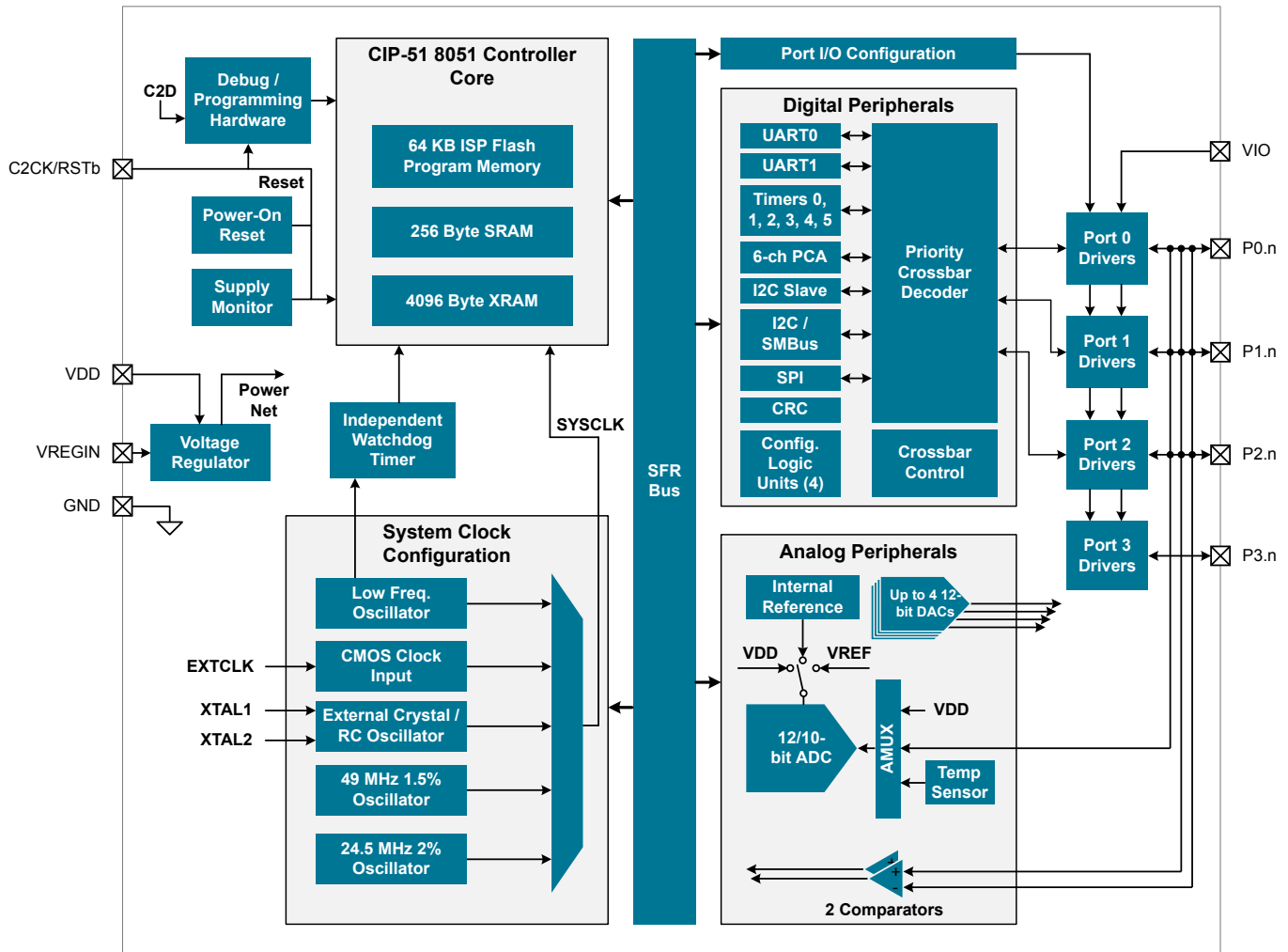


Figure 3.1. Detailed EFM8BB3 Block Diagram

### 3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

**Table 3.1. Power Modes**

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational		
Idle	<ul style="list-style-type: none"> <li>Core halted</li> <li>All peripherals clocked and fully operational</li> <li>Code resumes execution on wake event</li> </ul>	Set IDLE bit in PCON0	Any interrupt
Suspend	<ul style="list-style-type: none"> <li>Core and peripheral clocks halted</li> <li>HFOSC0 and HFOSC1 oscillators stopped</li> <li>Regulator in normal bias mode for fast wake</li> <li>Timer 3 and 4 may clock from LFOSC0</li> <li>Code resumes execution on wake event</li> </ul>	<ol style="list-style-type: none"> <li>Switch SYSCLK to HFOSC0</li> <li>Set SUSPEND bit in PCON1</li> </ol>	<ul style="list-style-type: none"> <li>Timer 4 Event</li> <li>SPI0 Activity</li> <li>I2C0 Slave Activity</li> <li>Port Match Event</li> <li>Comparator 0 Rising Edge</li> <li>CLUn Interrupt-Enabled Event</li> </ul>
Stop	<ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on any reset source</li> </ul>	<ol style="list-style-type: none"> <li>Clear STOPCF bit in REG0CN</li> <li>Set STOP bit in PCON0</li> </ol>	Any reset source
Snooze	<ul style="list-style-type: none"> <li>Core and peripheral clocks halted</li> <li>HFOSC0 and HFOSC1 oscillators stopped</li> <li>Regulator in low bias current mode for energy savings</li> <li>Timer 3 and 4 may clock from LFOSC0</li> <li>Code resumes execution on wake event</li> </ul>	<ol style="list-style-type: none"> <li>Switch SYSCLK to HFOSC0</li> <li>Set SNOOZE bit in PCON1</li> </ol>	<ul style="list-style-type: none"> <li>Timer 4 Event</li> <li>SPI0 Activity</li> <li>I2C0 Slave Activity</li> <li>Port Match Event</li> <li>Comparator 0 Rising Edge</li> <li>CLUn Interrupt-Enabled Event</li> </ul>
Shutdown	<ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on pin or power-on reset</li> </ul>	<ol style="list-style-type: none"> <li>Set STOPCF bit in REG0CN</li> <li>Set STOP bit in PCON0</li> </ol>	<ul style="list-style-type: none"> <li>RSTb pin reset</li> <li>Power-on reset</li> </ul>

### 3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P2.3 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.4 to P3.7 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P3.0 or P3.7, depending on the package option.

The port control block offers the following features:

- Up to 29 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- State retention feature allows pins to retain configuration through most reset sources.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 24 direct-pin interrupt sources with shared interrupt vector (Port Match).

### 3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

The clock control system offers the following features:

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to  $\pm 2\%$  over supply and temperature corners.
- 49 MHz internal oscillator (HFOSC1), accurate to  $\pm 2\%$  over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External Crystal / RC / C Oscillator.
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling:
  - Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.
  - HFOSC0 and HFOSC1 include 1.5x pre-scalers for further flexibility.

### 3.5 Counters/Timers and PWM

#### Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to six independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0 or comparator 1



## Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources for all timers include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8
- LFOSC0 divided by 8 may be used to clock Timer 3 and Timer 4 in active or suspend/snooze power modes
- Timer 4 is a low-power wake source, and can be chained together with Timer 3
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture
- LFOSC0 capture
- Comparator 0 capture
- Configurable Logic output capture

## Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

## 3.6 Communications and Other Digital Peripherals

### Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions
- Baud rates up to SYSCLK/2 (transmit) or SYSCLK/8 (receive)
- 8- or 9-bit data
- Automatic start and stop generation
- Single-byte buffer on transmit and receive

## Universal Asynchronous Receiver/Transmitter (UART1)

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions
- Dedicated baud rate generator supports baud rates up to  $\text{SYSCLK}/2$  (transmit) or  $\text{SYSCLK}/8$  (receive)
- 5, 6, 7, 8, or 9 bit data
- Automatic start and stop generation
- Automatic parity generation and checking
- Single-byte buffer on transmit and receive
- Auto-baud detection
- LIN break and sync field detection
- CTS / RTS hardware flow control

## Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

- Supports 3- or 4-wire master or slave modes
- Supports external clock frequencies up to 12 Mbps in master or slave mode
- Support for all clock phase and polarity modes
- 8-bit programmable clock rate (master)
- Programmable receive timeout (slave)
- Two byte FIFO on transmit and receive
- Can operate in suspend or snooze modes and wake the CPU on reception of a byte
- Support for multiple masters on the same data lines

## System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I<sup>2</sup>C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds
- Support for master, slave, and multi-master modes
- Hardware synchronization and arbitration for multi-master mode
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave and general call address recognition
- Firmware support for 10-bit slave address decoding
- Ability to inhibit all slave states
- Programmable data setup/hold times
- Transmit and receive buffers to help increase throughput in faster applications

## I2C Slave (I2CSLAVE0)

The I2C Slave interface is a 2-wire, bidirectional serial bus that is compatible with the I2C Bus Specification 3.0. It is capable of transferring in high-speed mode (HS-mode) at speeds of up to 3.4 Mbps. Firmware can write to the I2C interface, and the I2C interface can autonomously control the serial transfer of data. The interface also supports clock stretching for cases where the core may be temporarily prohibited from transmitting a byte or processing a received byte during an I2C transaction. This module operates only as an I2C slave device.

The I2C module includes the following features:

- Standard (up to 100 kbps), Fast (400 kbps), Fast Plus (1 Mbps), and High-speed (3.4 Mbps) transfer speeds
- Support for slave mode only
- Clock low extending (clock stretching) to interface with faster masters
- Hardware support for 7-bit slave address recognition
- Hardware support for multiple slave addresses with the option to save the matching address in the receive FIFO

## 16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

## Configurable Logic Units (CLU0, CLU1, CLU2, and CLU3)

The Configurable Logic block consists of multiple Configurable Logic Units (CLUs). CLUs are flexible logic functions which may be used for a variety of digital functions, such as replacing system glue logic, aiding in the generation of special waveforms, or synchronizing system event triggers.

- Four configurable logic units (CLUs), with direct-pin and internal logic connections
- Each unit supports 256 different combinatorial logic functions (AND, OR, XOR, muxing, etc.) and includes a clocked flip-flop for synchronous operations
- Units may be operated synchronously or asynchronously
- May be cascaded together to perform more complicated logic functions
- Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers and PCA channels
- Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, Timers, etc.)
- Asynchronous output may be used to wake from low-power states

## 3.7 Analog

### 12/10-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12- and 10-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 20 external inputs
- Single-ended 12-bit and 10-bit modes
- Supports an output update rate of up to 400 ksps in 12-bit mode
- Channel sequencer logic with direct-to-XDATA output transfers
- Operation in a low power mode at lower conversion speeds
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Output data window comparator allows automatic range checking
- Support for output data accumulation
- Conversion complete and window compare interrupts supported
- Flexible output data formatting
- Includes a fully-internal fast-settling 1.65 V reference and an on-chip precision 2.4 / 1.2 V reference, with support for using the supply as the reference, an external reference and signal ground
- Integrated temperature sensor

### 12-Bit Digital-to-Analog Converters (DAC0, DAC1, DAC2, DAC3)

The DAC modules are 12-bit Digital-to-Analog Converters with the capability to synchronize multiple outputs together. The DACs are fully configurable under software control. The voltage reference for the DACs is selectable between internal and external reference sources.

- Voltage output with 12-bit performance
- Supports an update rate of 200 ksps
- Hardware conversion trigger, selectable between software, external I/O and internal timer and configurable logic sources
- Outputs may be configured to persist through reset and maintain output state to avoid system disruption
- Multiple DAC outputs can be synchronized together
- DAC pairs (DAC0 and 1 or DAC2 and 3) support complementary output waveform generation
- Outputs may be switched between two levels according to state of configurable logic / PWM input trigger
- Flexible input data formatting
- Supports references from internal supply, on-chip precision reference, or external VREF pin

## Low Current Comparators (CMP0, CMP1)

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator includes the following features:

- Up to 10 (CMP0) or 9 (CMP1) external positive inputs
- Up to 10 (CMP0) or 9 (CMP1) external negative inputs
- Additional input options:
  - Internal connection to LDO output
  - Direct connection to GND
  - Direct connection to VDD
  - Dedicated 6-bit reference DAC
- Synchronous and asynchronous outputs can be routed to pins via crossbar
- Programmable hysteresis between 0 and  $\pm 20$  mV
- Programmable response time
- Interrupts generated on rising, falling, or both edges
- PWM output kill feature

## 3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. By default, the Port I/O latches are reset to 1 in open-drain mode, with weak pullups enabled during and after the reset. Optionally, firmware may configure the port I/O, DAC outputs, and precision reference to maintain state through system resets other than power-on resets. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

## 3.9 Debugging

The EFM8BB3 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.



### 3.10 Bootloader

All devices come pre-programmed with a UART0 bootloader. This bootloader resides in the code security page, which is the last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

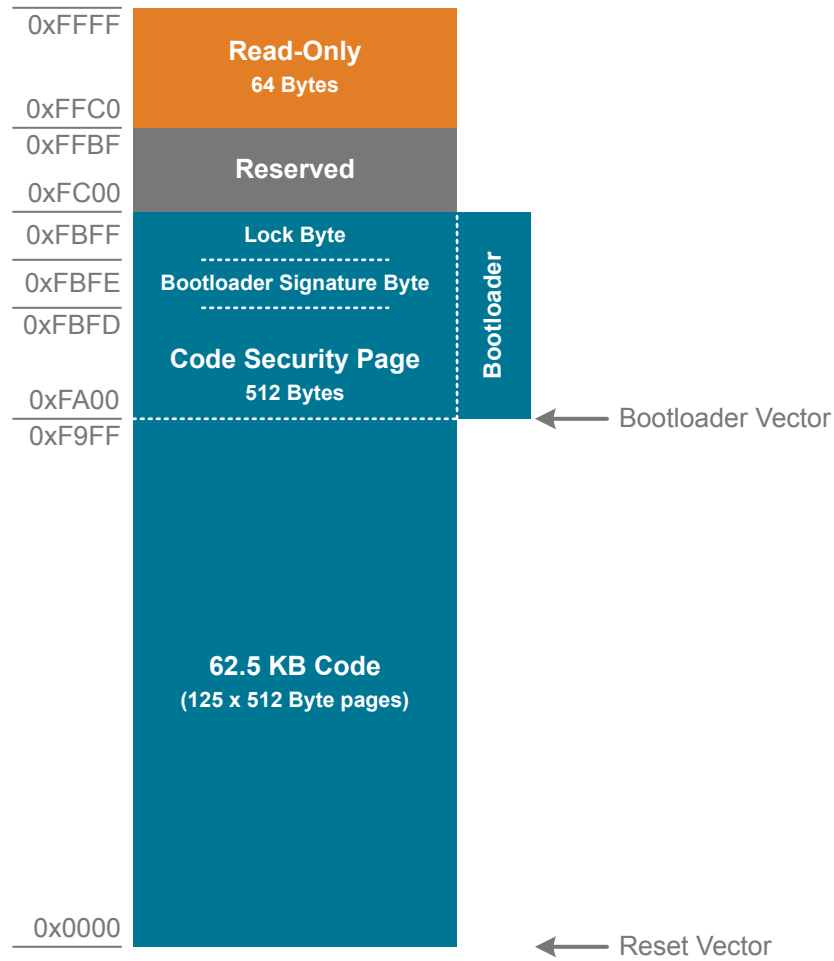


Figure 3.2. Flash Memory Map with Bootloader — 62.5 KB Devices

## 4. Electrical Specifications

### 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions](#) on page 13, unless stated otherwise.

#### 4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V <sub>DD</sub>		2.2	—	3.6	V
Operating Supply Voltage on VIO <sup>2,3</sup>	V <sub>IO</sub>		TBD	—	V <sub>DD</sub>	V
System Clock Frequency	f <sub>SYSCLK</sub>		0	—	50	MHz
Operating Ambient Temperature	T <sub>A</sub>		-40	—	85	°C

**Note:**

1. All voltages with respect to GND
2. In certain package configurations, the VIO and VDD supplies are bonded to the same pin.
3. GPIO levels are undefined whenever VIO is less than 1 V.

## 4.1.2 Power Consumption

**Table 4.2. Power Consumption**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current						
Normal Mode-Full speed with code executing from flash	I <sub>DD</sub>	F <sub>SYSCLK</sub> = 49 MHz <sup>2</sup>	—	TBD	TBD	mA
		F <sub>SYSCLK</sub> = 24.5 MHz <sup>2</sup>	—	4.5	TBD	mA
		F <sub>SYSCLK</sub> = 1.53 MHz <sup>2</sup>	—	615	TBD	μA
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup>	—	155	TBD	μA
Idle Mode-Core halted with peripherals running	I <sub>DD</sub>	F <sub>SYSCLK</sub> = 49 MHz <sup>2</sup>	—	TBD	TBD	mA
		F <sub>SYSCLK</sub> = 24.5 MHz <sup>2</sup>	—	2.8	TBD	mA
		F <sub>SYSCLK</sub> = 1.53 MHz <sup>2</sup>	—	455	TBD	μA
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup>	—	145	TBD	μA
Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off.	I <sub>DD</sub>	LFO Running	—	125	TBD	μA
		LFO Stopped	—	120	TBD	μA
Snooze Mode-Core halted and high frequency clocks stopped. Regulator in low-power state, Supply monitor off.	I <sub>DD</sub>	LFO Running	—	26	TBD	μA
		LFO Stopped	—	21	TBD	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I <sub>DD</sub>		—	120	TBD	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I <sub>DD</sub>		—	0.2	—	μA
Analog Peripheral Supply Currents						
High-Frequency Oscillator 0	I <sub>HFOSC0</sub>	Operating at 24.5 MHz, T <sub>A</sub> = 25 °C	—	55	—	μA
High-Frequency Oscillator 1	I <sub>HFOSC1</sub>	Operating at 49 MHz, T <sub>A</sub> = 25 °C	—	TBD	—	μA
Low-Frequency Oscillator	I <sub>LFOSC</sub>	Operating at 80 kHz, T <sub>A</sub> = 25 °C	—	5	—	μA
ADC0 <sup>4</sup>	I <sub>ADC</sub>	TBD	—	TBD	TBD	μA
Internal ADC0 Reference <sup>5</sup>	I <sub>VREFFS</sub>	Normal Power Mode	—	680	TBD	μA
		Low Power Mode	—	160	TBD	μA
On-chip Precision Reference	I <sub>VREFP</sub>		—	75	—	μA
Temperature Sensor	I <sub>TSENSE</sub>		—	75	120	μA
Digital-to-Analog Converters (DAC0, DAC1) <sup>6</sup>	I <sub>DAC</sub>		—	125	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Comparators (CMP0, CMP1)	I <sub>CMP</sub>	CPMD = 11	—	0.5	—	μA
		CPMD = 10	—	3	—	μA
		CPMD = 01	—	10	—	μA
		CPMD = 00	—	25	—	μA
Comparator Reference	I <sub>CPREF</sub>		—	TBD	—	μA
Voltage Supply Monitor (VMON0)	I <sub>VMON</sub>		—	15	20	μA

**Note:**

1. Currents are additive. For example, where I<sub>DD</sub> is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal LDO regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal LDO regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in low power mode. Total ADC + Reference current will depend on sampling rate.
6. DAC supply current for each enabled DA and not including external load on pin.

### 4.1.3 Reset and Supply Monitor

**Table 4.3. Reset and Supply Monitor**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Supply Monitor Threshold	V <sub>VDDM</sub>		1.85	1.95	2.1	V
Power-On Reset (POR) Threshold	V <sub>POR</sub>	Rising Voltage on VDD	—	1.4	—	V
		Falling Voltage on VDD	0.75	—	1.36	V
VDD Ramp Time	t <sub>RMP</sub>	Time to V <sub>DD</sub> > 2.2 V	10	—	—	μs
Reset Delay from POR	t <sub>POR</sub>	Relative to V <sub>DD</sub> > V <sub>POR</sub>	3	10	31	ms
Reset Delay from non-POR source	t <sub>RST</sub>	Time between release of reset source and code execution	—	50	—	μs
RST Low Time to Generate Reset	t <sub>RSTL</sub>		15	—	—	μs
Missing Clock Detector Response Time (final rising edge to reset)	t <sub>MCD</sub>	F <sub>SYSClk</sub> > 1 MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F <sub>MCD</sub>		—	7.5	13.5	kHz
VDD Supply Monitor Turn-On Time	t <sub>MON</sub>		—	2	—	μs

#### 4.1.4 Flash Memory

**Table 4.4. Flash Memory**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time <sup>1,2</sup>	t <sub>WRITE</sub>	One Byte, F <sub>SYSClk</sub> = 24.5 MHz	19	20	21	μs
Erase Time <sup>1,2</sup>	t <sub>ERASE</sub>	One Page, F <sub>SYSClk</sub> = 24.5 MHz	5.2	5.35	5.5	ms
V <sub>DD</sub> Voltage During Programming <sup>3</sup>	V <sub>PROG</sub>		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N <sub>WE</sub>		20k	100k	—	Cycles

**Note:**

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSClk cycles.
2. The internal High-Frequency Oscillator 0 has a programmable output frequency, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V<sub>VDDM</sub>).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

#### 4.1.5 Power Management Timing

**Table 4.5. Power Management Timing**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Idle Mode Wake-up Time	t <sub>IDLEWK</sub>		2	—	3	SYSClks
Suspend Mode Wake-up Time	t <sub>SUS- PENDWK</sub>	SYSClk = HFOSC0 CLKDIV = 0x00	—	170	—	ns
Snooze Mode Wake-up Time	t <sub>SLEEPWK</sub>	SYSClk = HFOSC0 CLKDIV = 0x00	—	12	—	μs



#### 4.1.6 Internal Oscillators

**Table 4.6. Internal Oscillators**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	$f_{HFOSC0}$	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	$PSS_{HFOSC0}$	$T_A = 25\text{ }^\circ\text{C}$	—	0.5	—	%/V
Temperature Sensitivity	$TS_{HFOSC0}$	$V_{DD} = 3.0\text{ V}$	—	40	—	ppm/ $^\circ\text{C}$
High Frequency Oscillator 1 (49 MHz)						
Oscillator Frequency	$f_{HFOSC1}$	Full Temperature and Supply Range	48.25	49	49.75	MHz
Power Supply Sensitivity	$PSS_{HFOSC1}$	$T_A = 25\text{ }^\circ\text{C}$	—	TBD	—	%/V
Temperature Sensitivity	$TS_{HFOSC1}$	$V_{DD} = 3.0\text{ V}$	—	TBD	—	ppm/ $^\circ\text{C}$
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	$f_{LFOSC}$	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	$PSS_{LFOSC}$	$T_A = 25\text{ }^\circ\text{C}$	—	0.05	—	%/V
Temperature Sensitivity	$TS_{LFOSC}$	$V_{DD} = 3.0\text{ V}$	—	65	—	ppm/ $^\circ\text{C}$

#### 4.1.7 External Clock Input

**Table 4.7. External Clock Input**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	$f_{CMOS}$		0	—	50	MHz
External Input CMOS Clock High Time	$t_{CMOSH}$		9	—	—	ns
External Input CMOS Clock Low Time	$t_{CMOSL}$		9	—	—	ns

#### 4.1.8 Crystal Oscillator

**Table 4.8. Crystal Oscillator**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	$f_{XTAL}$		0.02	—	25	MHz
Crystal Drive Current	$I_{XTAL}$	XFCN = 0	—	0.5	—	$\mu A$
		XFCN = 1	—	1.5	—	$\mu A$
		XFCN = 2	—	4.8	—	$\mu A$
		XFCN = 3	—	14	—	$\mu A$
		XFCN = 4	—	40	—	$\mu A$
		XFCN = 5	—	120	—	$\mu A$
		XFCN = 6	—	550	—	$\mu A$
		XFCN = 7	—	2.6	—	mA

## 4.1.9 ADC

Table 4.9. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N <sub>bits</sub>	12 Bit Mode	12			Bits
		10 Bit Mode	10			Bits
Throughput Rate (High Speed Mode)	f <sub>S</sub>	10 Bit Mode	—	—	1.125	Msp/s
Throughput Rate (Low Power Mode)	f <sub>S</sub>	12 Bit Mode	—	—	300	ksps
		10 Bit Mode	—	—	1.125	Msp/s
Tracking Time	t <sub>TRK</sub>	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t <sub>PWR</sub>		1.2	—	—	μs
SAR Clock Frequency	f <sub>SAR</sub>	High Speed Mode	—	—	18	MHz
		Low Power Mode	—	—	TBD	MHz
Conversion Time <sup>1</sup>	t <sub>CNV</sub>	12-Bit Conversion, SAR Clock = 18 MHz, System Clock = 49 MHz	0.7			μs
		10-Bit Conversion, SAR Clock = 18 MHz, System Clock = 49 MHz	0.59			μs
Sample/Hold Capacitor	C <sub>SAR</sub>	Gain = 1	—	5.2	—	pF
		Gain = 0.75	—	3.9	—	pF
		Gain = 0.5	—	2.6	—	pF
		Gain = 0.25	—	1.3	—	pF
Input Pin Capacitance	C <sub>IN</sub>		—	20	—	pF
Input Mux Impedance	R <sub>MUX</sub>		—	550	—	Ω
Voltage Reference Range	V <sub>REF</sub>		1	—	V <sub>IO</sub>	V
Input Voltage Range <sup>2</sup>	V <sub>IN</sub>	Gain = 1	0	—	V <sub>REF</sub> / Gain	V
Power Supply Rejection Ratio	PSRR <sub>ADC</sub>		—	TBD	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	-1.4	TBD	+1.4	LSB
		10 Bit Mode	—	TBD	—	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	—	TBD	0.9	LSB
		10 Bit Mode	—	TBD	—	LSB
Offset Error	E <sub>OFF</sub>	12 Bit Mode	-2	TBD	2	LSB
		10 Bit Mode	—	TBD	—	LSB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset Temperature Coefficient	TC <sub>OFF</sub>		—	TBD	—	LSB/°C
Slope Error	E <sub>M</sub>	12 Bit Mode	—	TBD	TBD	%
		10 Bit Mode	—	TBD	—	%
Dynamic Performance 10 kHz Sine Wave Input 1 dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	—	TBD	—	dB
		10 Bit Mode	—	TBD	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	TBD	TBD	—	dB
		10 Bit Mode	—	TBD	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	TBD	—	dB
		10 Bit Mode	—	TBD	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	TBD	—	dB
		10 Bit Mode	—	TBD	—	dB

**Note:**

1. Conversion Time does not include Tracking Time. Total Conversion Time is:

$$\text{Total Conversion Time} = [\text{RPT} \times (\text{ADTK} + \text{NUMBITS} + 1) \times \text{T}(\text{SARCLK})] + (\text{T}(\text{ADCCLK}) \times 4)$$

where RPT is the number of conversions represented by the ADRPT field and ADCCLK is the clock selected for the ADC.

2. Absolute input pin voltage is limited by the V<sub>IO</sub> supply.

#### 4.1.10 Voltage Reference

**Table 4.10. Voltage Reference**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	$V_{REFFS}$		1.62	1.65	1.68	V
Temperature Coefficient	$TC_{REFFS}$		—	50	—	ppm/°C
Turn-on Time	$t_{REFFS}$		—	—	1.5	μs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
On-chip Precision Reference						
Valid Supply Range	$V_{DD}$	1.2 V Output	2.2	—	3.6	V
		2.4 V Output	2.7	—	3.6	V
Output Voltage	$V_{REFP}$	1.2 V Output, T = 25 °C	TBD	1.2	TBD	V
		2.4 V Output, T = 25 °C	TBD	2.4	TBD	V
Turn-on Time, settling to 0.5 LSB	$t_{VREFP}$	4.7 μF tantalum + 0.1 μF ceramic bypass on VREF pin	—	3	—	ms
		0.1 μF ceramic bypass on VREF pin	—	100	—	μs
Load Regulation	$LR_{VREFP}$	Load = 0 to 200 μA to GND	—	TBD	—	μV/μA
Load Capacitor	$C_{VREFP}$	Load = 0 to 200 μA to GND	0.1	—	—	μF
Short-circuit current	$ISC_{VREFP}$		—	—	8	mA
Power Supply Rejection	$PSRR_{VREFP}$		—	TBD	—	ppm/V
External Reference						
Input Current	$I_{EXTREF}$	ADC Sample Rate = 800 ksp/s; VREF = 3.0 V	—	5	—	μA



4.1.11 Temperature Sensor

Table 4.11. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V <sub>OFF</sub>	T <sub>A</sub> = 0 °C	—	TBD	—	mV
Offset Error <sup>1</sup>	E <sub>OFF</sub>	T <sub>A</sub> = 0 °C	—	TBD	—	mV
Slope	M		—	TBD	—	mV/°C
Slope Error <sup>1</sup>	E <sub>M</sub>		—	TBD	—	μV/°C
Linearity			—	TBD	—	°C
Turn-on Time			—	TBD	—	μs

**Note:**

1. Represents one standard deviation from the mean.

#### 4.1.12 DACs

Table 4.12. DACs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$N_{\text{bits}}$			12		Bits
Throughput Rate	$f_S$		—	—	200	ksps
Integral Nonlinearity	INL		TBD	$\pm 0.5$	TBD	LSB
Differential Nonlinearity	DNL		TBD	$\pm 5$	TBD	LSB
Output Noise	$V_{\text{REF}} = 2.4 \text{ V}$ $f_S = 0.1 \text{ Hz to } 300 \text{ kHz}$		—	110	—	$\mu\text{V}_{\text{RMS}}$
Slew Rate	SLEW		—	$\pm 1$	—	$\text{V}/\mu\text{s}$
Output Settling Time to 1 LSB	$t_{\text{SETTLE}}$	$V_{\text{OUT}}$ change between 25% and 75% Full Scale	—	2.6	5	$\mu\text{s}$
Power-on Time	$t_{\text{PWR}}$		—	—	10	$\mu\text{s}$
Voltage Reference Range	$V_{\text{REF}}$		1.15	—	$V_{\text{DD}}$	V
Power Supply Rejection Ratio	PSRR	DC, $V_{\text{OUT}} = 50\%$ Full Scale	—	110	—	dB
		1 kHz, $V_{\text{OUT}} = 50\%$ Full Scale	—	60	—	dB
Total Harmonic Distortion	THD	$V_{\text{OUT}} = 10 \text{ kHz}$ sine wave, 10% to 90%	60	—	—	dB
Offset Error	$E_{\text{OFF}}$	$V_{\text{REF}} = 2.4 \text{ V}$	TBD	$\pm 0.5$	TBD	LSB
Offset Temperature Coefficient	$TC_{\text{OFF}}$		—	TBD	—	$\text{ppm}/^\circ\text{C}$
Full-Scale Error	$E_{\text{FS}}$	$V_{\text{REF}} = 2.4 \text{ V}$	TBD	$\pm 5$	TBD	LSB
Full-Scale Error Tempco	$TC_{\text{FS}}$		—	TBD	—	$\text{ppm}/^\circ\text{C}$
External Load Impedance	$R_{\text{LOAD}}$		2	—	—	$\text{k}\Omega$
External Load Capacitance	$C_{\text{LOAD}}$		TBD	—	100	$\mu\text{F}$
Load Regulation		$V_{\text{OUT}} = 50\%$ Full Scale $I_{\text{OUT}} = -2 \text{ to } 2 \text{ mA}$	—	100	TBD	$\mu\text{V}/\text{mA}$

### 4.1.13 Comparators

**Table 4.13. Comparators**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	$t_{RESP0}$	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	150	—	ns
Response Time, CPMD = 11 (Low- est Power)	$t_{RESP3}$	+100 mV Differential	—	1.5	—	$\mu$ s
		-100 mV Differential	—	3.5	—	$\mu$ s
Positive Hysteresis Mode 0 (CPMD = 00)	$HYS_{CP+}$	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	$HYS_{CP-}$	CPHYN = 00	—	-0.4	—	mV
		CPHYN = 01	—	-8	—	mV
		CPHYN = 10	—	-16	—	mV
		CPHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	$HYS_{CP+}$	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	$HYS_{CP-}$	CPHYN = 00	—	-0.5	—	mV
		CPHYN = 01	—	-6	—	mV
		CPHYN = 10	—	-12	—	mV
		CPHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	$HYS_{CP+}$	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	$HYS_{CP-}$	CPHYN = 00	—	-0.6	—	mV
		CPHYN = 01	—	-4.5	—	mV
		CPHYN = 10	—	-9	—	mV
		CPHYN = 11	—	-18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	$HYS_{CP+}$	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV