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System Generator for DSP

Getting Started Guide

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About This Guide

This Getting Started Guide introduces you to **System Generator for DSP**, then provides installation and configuration instructions, release information, and six mini-training modules that highlight the main features of the product. Each module starts with a lesson of 8-10 slides that explain important concepts, followed by a lab exercise that take about 30 minutes to complete. Because this introductory training is part of the tool, you can progress through the material at your own pace and on your own time schedule

Guide Contents

This Getting Started Guide contains the following topics:

- Introduction
- Installation
- Release Information
- Getting Started
 - a. Design Creation Basics
 - b. Fixed Point and Bit Operations
 - c. System Control
 - d. Multi-Rate Systems
 - e. Using Memories
 - f. Designing Filters
 - g. Additional Examples and Tutorials

System Generator PDF Doc Set

This Getting Started Guide can be found in the System Generator Help system and is also part of the System Generator Doc Set that is provided in PDF format. The content of the doc set is as follows:

- *System Generator for DSP Getting Started Guide*
- *System Generator for DSP User Guide*
- *System Generator for DSP Reference Guide*

Note: Hyperlinks across these PDF documents work only when the PDF files reside in the same folder. After clicking a Hyperlink in the Adobe Reader, you can return to the previous page by pressing the Alt key and the left arrow key (←) at the same time.

Additional Resources

To find additional documentation, see the Xilinx website at:

<http://www.xilinx.com/support/documentation/index.htm>.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

<http://www.xilinx.com/support/mysupport.htm>.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Courier font	Messages, prompts, and program files that the system displays	speed grade: - 100
Courier bold	Literal commands that you enter in a syntactical statement	ngdbuild <i>design_name</i>
Helvetica bold	Commands that you select from a menu	File Ø Open
	Keyboard shortcuts	Ctrl+C
Italic font	Variables in a syntax statement for which you must supply values	ngdbuild <i>design_name</i>
	References to other manuals	See the <i>Development System Reference Guide</i> for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected.
Square brackets []	An optional entry or parameter. However, in bus specifications, such as bus [7 : 0] , they are required.	ngdbuild [<i>option_name</i>] <i>design_name</i>
Braces { }	A list of items from which you must choose one or more	lowpwr = { on off }
Vertical bar	Separates items in a list of choices	lowpwr = { on off }

Convention	Meaning or Use	Example
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	allow block <i>block_name loc1 loc2 ... locn;</i>

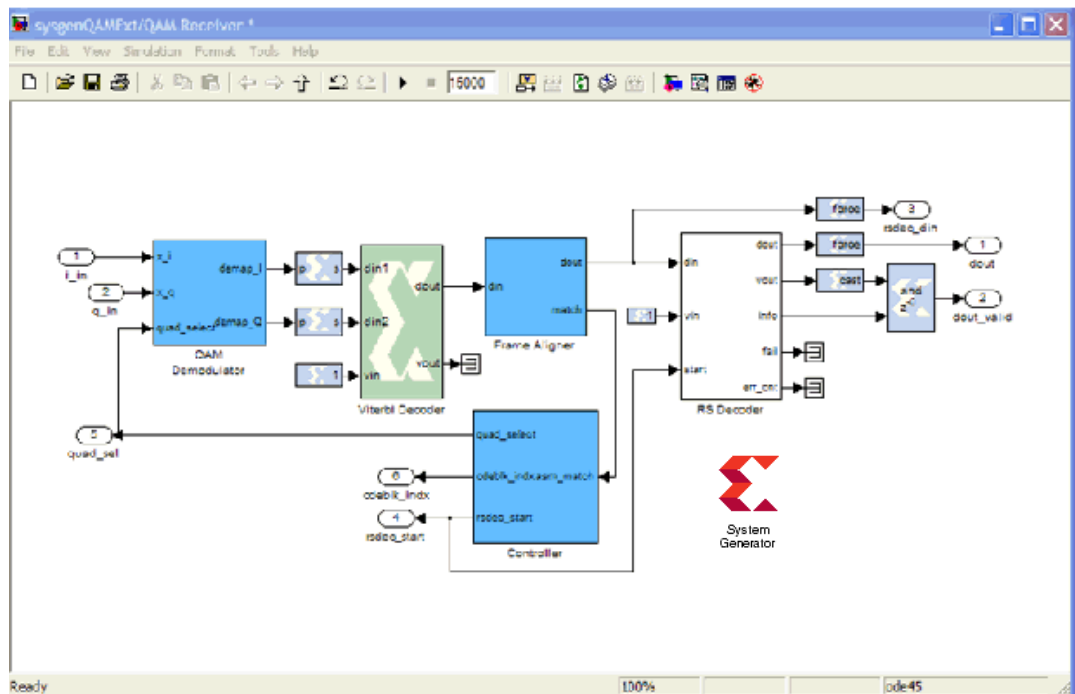
Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the topic " Additional Resources " for details. Refer to " Title Formats " in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the <i>Virtex-II Platform FPGA User Guide</i> .
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

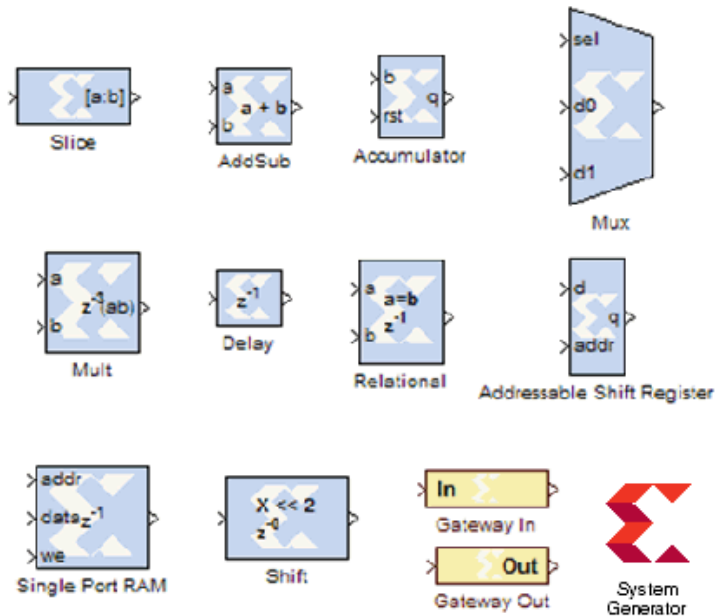
Introduction

System Generator is a DSP design tool from Xilinx that enables the use of the MathWorks model-based Simulink® design environment for FPGA design. Previous experience with Xilinx FPGAs or RTL design methodologies are not required when using System Generator. Designs are captured in the DSP friendly Simulink modeling environment using a Xilinx specific blockset. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file.



The Xilinx DSP Block Set

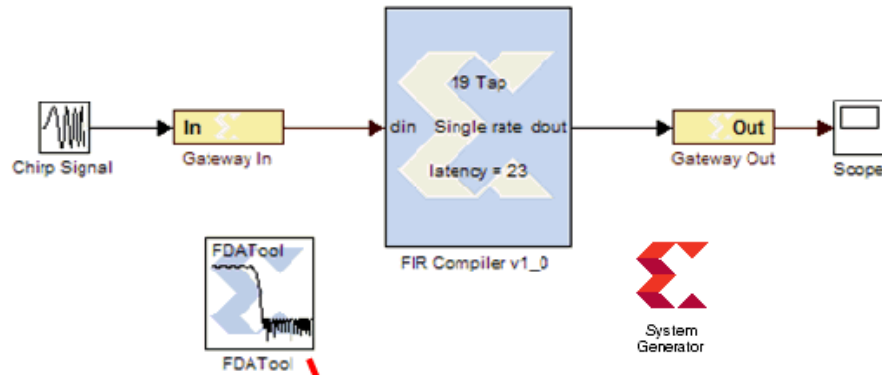
Over 90 DSP building blocks are provided in the Xilinx DSP blockset for Simulink. These blocks include the common DSP building blocks such as adders, multipliers and registers. Also included are a set of complex DSP building blocks such as forward error correction blocks, FFTs, filters and memories. These blocks leverage the Xilinx IP core generators to deliver optimized results for the selected device.



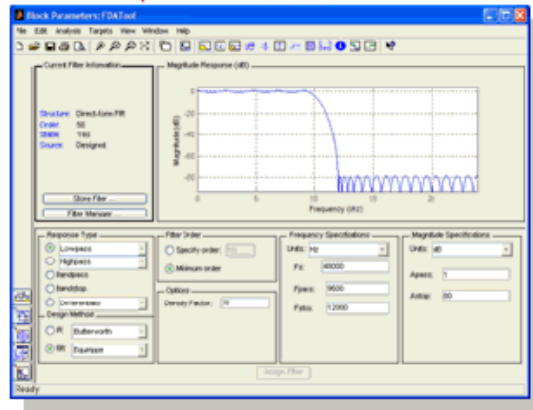
FIR Filter Generation

System Generator includes a FIR Compiler block that targets the dedicated DSP48 hardware resources in the Virtex®-4 and Virtex-5 devices to create highly optimized implementations that can run in excess of 500 Mhz. Configuration options allow generation of direct, polyphase decimation, polyphase interpolation and oversampled implementations. Standard MATLAB functions such as fir2 or the MathWorks FDAtool can be used to create coefficients for the Xilinx FIR Compiler.

FIR Compiler

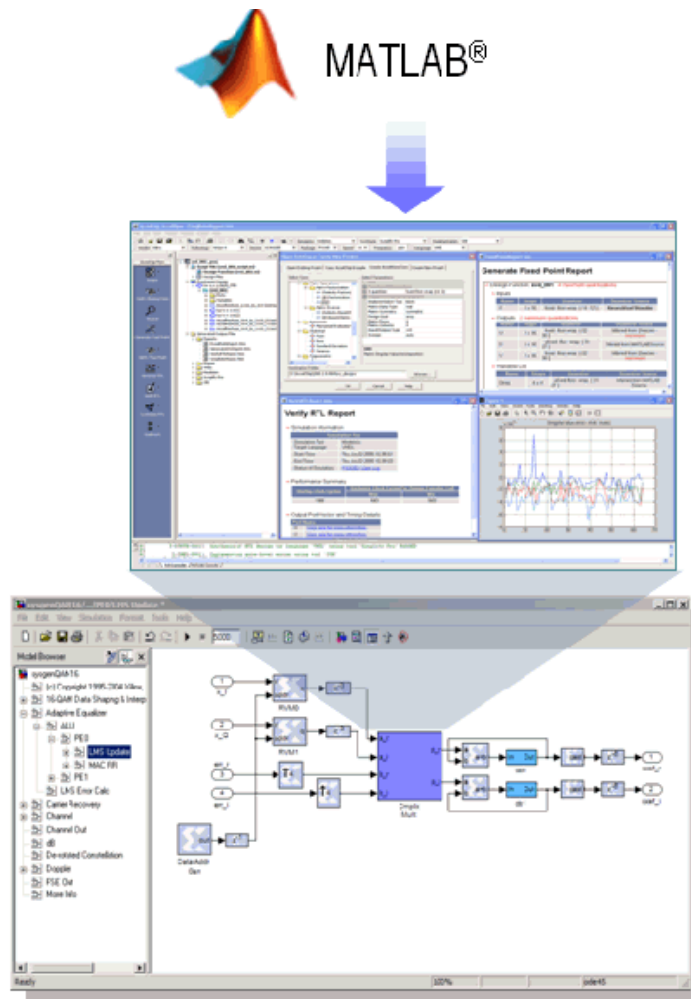


FDA Tool



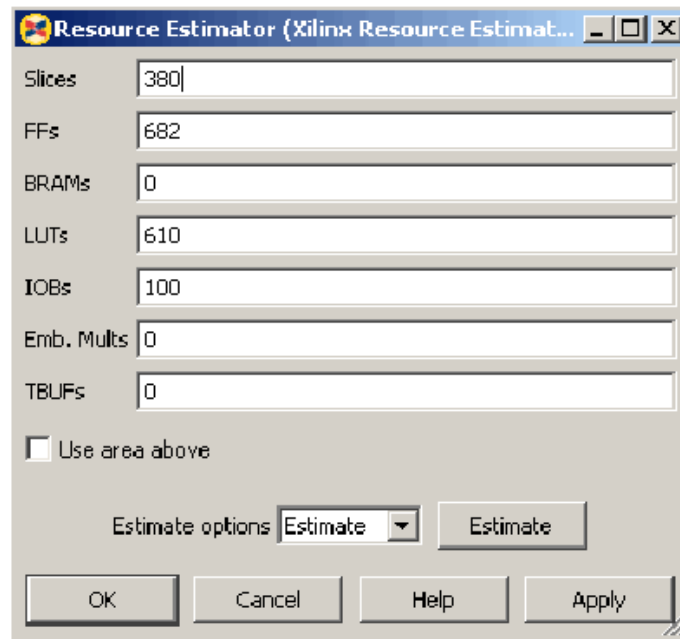
Support for MATLAB

Included in System Generator is an MCode block that allows the use of non-algorithmic MATLAB for the modeling and implementation of simple control operations.



System Resource Estimation

System Generator provides a Resource Estimator block that quickly estimates the area of a design prior to place and route. This can be a valuable aid in the hardware / software partitioning process by helping system designers take full advantage of the FPGA resources which include up to 640 multiply/accumulate (or DSP) blocks in the Virtex®-5 devices.



The screenshot shows the 'Resource Estimator' dialog box with the following fields and controls:

Field	Value
Slices	380
FFs	682
BRAMs	0
LUTs	610
IOBs	100
Emb. Mults	0
TBUFs	0

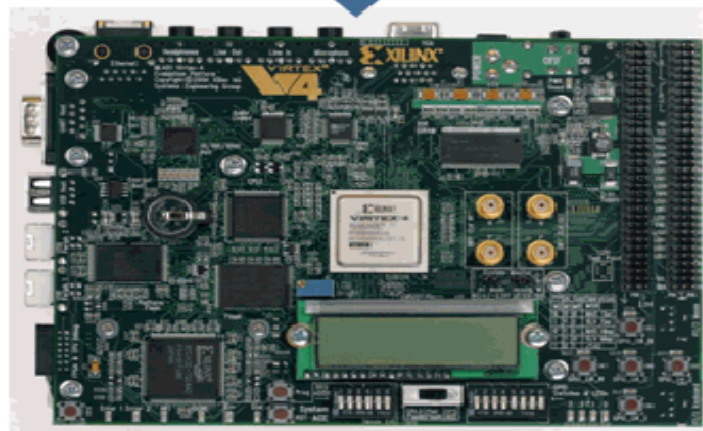
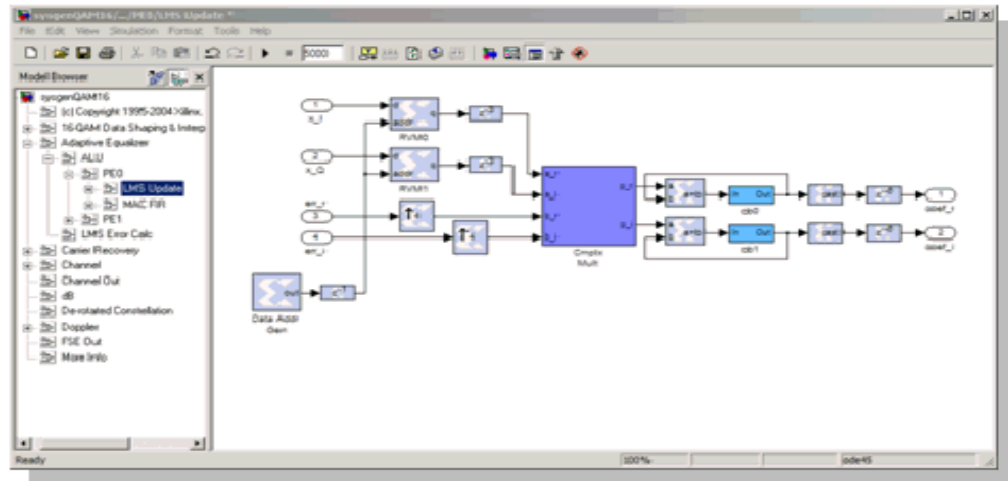
Use area above

Estimate options: Estimate (dropdown) Estimate (button)

Buttons: OK, Cancel, Help, Apply

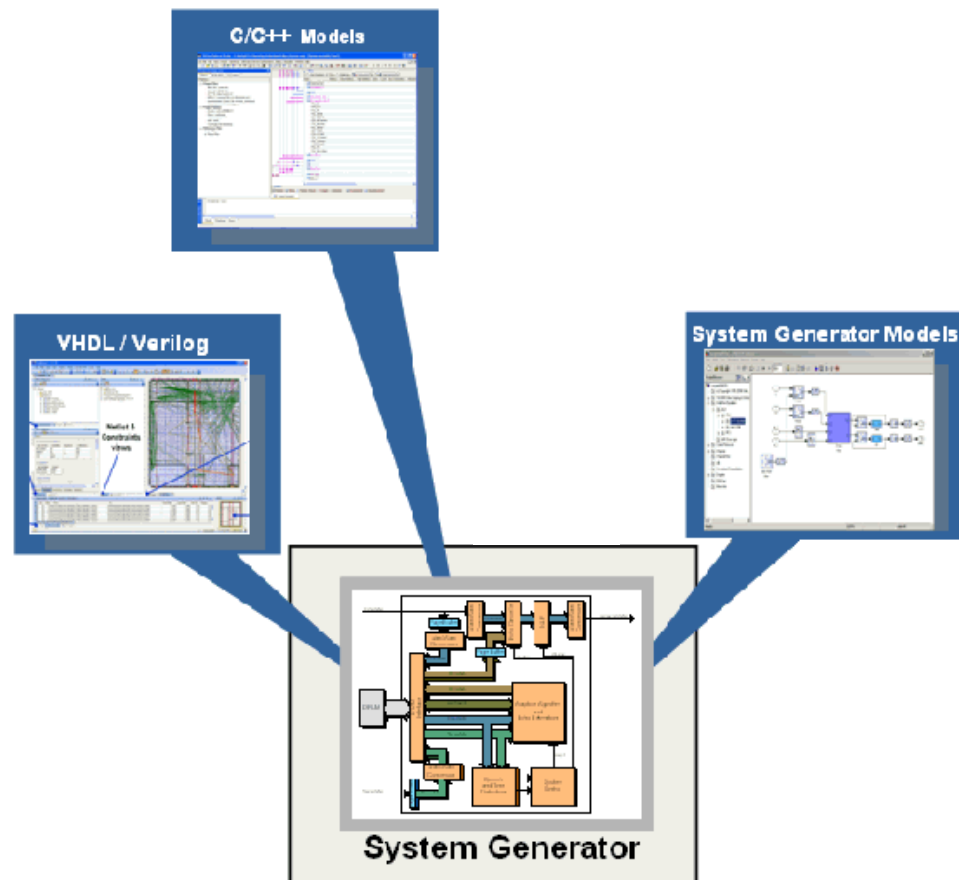
Hardware Co-Simulation

System Generator provides accelerated simulation through hardware co-simulation. System Generator will automatically create a hardware simulation token for a design captured in the Xilinx DSP blockset that will run on one of over 20 supported hardware platforms. This hardware will co-simulate with the rest of the Simulink system to provide up to a 1000x simulation performance increase.



System Integration Platform

System Generator provides a system integration platform for the design of DSP FPGAs that allows the RTL, Simulink, MATLAB and C/C++ components of a DSP system to come together in a single simulation and implementation environment. System Generator supports a black box block that allows RTL to be imported into Simulink and co-simulated with either ModelSim or Xilinx® ISE® Simulator. System Generator also supports the inclusion of a MicroBlaze® embedded processor running C/C++ programs.



Installation

Downloading

System Generator is part of the ISE® Design Suite and may be download from the Xilinx web page. You may purchase, register, and download the System Generator software from the site at:

<http://www.xilinx.com/tools/sysgen.htm>

Note: In special circumstances, System Generator can be delivered on a CD. Please contact your Xilinx distributor if your circumstances prohibit you from downloading the software via the web.

Hardware Co-Simulation Support

If you have an FPGA development board, you may be able to take advantage of System Generator's ability to use FPGA hardware co-simulation with Simulink simulations. The System Generator software includes support for the XtremeDSP Development Kit, the MicroBlaze™ Multimedia Demonstration boards, the MVI hardware platform, the ML402 Virtex®-4 Board, the ML506 Virtex-5 Board, the ML605 Virtex-6 Board, the Spartan-3A DSP 1800 Starter Board, the Spartan-3A DSP 3400 Development Board, and the Spartan-6 SP601/SP605 Board. Additional System Generator board support packages provide support for additional hardware co-simulation boards. System Generator board support packages can be downloaded from the following URL:

http://www.xilinx.com/products/boards_kits/index.htm

UNC Paths Not Supported

System Generator does not support UNC (Universal Naming Convention) paths. For example System Generator cannot operate on a design that is located on a shared network drive without mapping to the drive first.

Using the ISE Design Suite Installer

System Generator for DSP is part of the Xilinx ISE® Design Suite and you must use the ISE Design Suite installer to install System Generator.

Before invoking the ISE Design Suite installer, it is a good idea to make sure that all instances of MATLAB are closed. When all instances of MATLAB are closed, launch the installer and follow the directions on the screen.

Choosing the MATLAB Version for a Windows OS Installation

As the last step of the System Generator Windows installation, click the check box of the MATLAB installation you wish to associate with this version of System Generator, then click **Apply**.

If you don't see a valid version of MATLAB listed, for example a version installed on a network device, click the **Add Version** button, browse to the MATLAB root directory of the unlisted version, then click **Add**. If you wish to associate this version of MATLAB with System Generator, click the check box of the newly listed MATLAB installation, then click **Apply**.

If you have no version of MATLAB available, click **Choose Later** to continue with the installation. At a later time, after you have installed MATLAB, you can associate that version of MATLAB with System Generator by executing the Windows menu item **Start > All Programs > Xilinx ISE Design Suite 13.1 > System Generator > Select MATLAB version for Xilinx System Generator**.

Post Installation Tasks

Post-Installation Tasks on Linux

After following the directions of the main ISE Design Suite Installation Wizard, you are ready to launch System Generator by typing: `sysgen`

Note: This will invoke MATLAB and dynamically add System Generator to that MATLAB session. At the top of the MATLAB Command Window, you should see the "Installed System Generator dynamically" messages. You are now ready to run System Generator.

The following is an expected message under certain conditions. If System Generator is already installed when this script runs, you will see the following message:

```
System Generator currently found installed into matlab
default path.
```

Troubleshooting a Linux Installation

The following four functions are used to troubleshoot and verify the Linux Installation.

`xl_get_matlab_support_xmlfile`

This MATLAB function will retrieve the expected location of the common XML file used for determining MATLAB support within System Generator.

`xl_verify_matlab_support_xmlfile`

This matlab function will verify that the XML file exists and is readable. If no XML file exists, the following error message is thrown to the MATLAB console"

Could not find ml_supported.xml to determine supported versions of MATLAB with System Generator.

If the XML file is unreadable, the error message that is thrown to the MATLAB console is:

```
Could not read ml_supported.xml to determine supported versions of MATLAB with System Generator
```

xl_read_matlab_support_xmlfile

This MATLAB function reads and parses the XML file looking for the supported MATLAB version information and provides error/warning messages used by the sysgen_startup.m script.

xl_test_matlab_support_xmlfile

This MATLAB function tests the current instantiated MATLAB session and compares its version to those which are supported. Errors or warnings will be displayed based on results of this comparison. If the XML file is devoid of information, the error thrown to the MATLAB console is as follows:

```
Matlab support table used by System Generator is empty!
```

If the XML file information does not conform to the expected format, the following error is thrown to the MATLAB console:

```
Input matlab support table is not well formed. It should have only 2 columns!
```

If you are using a version of MATLAB that is too old (unsupported), then you will see the following error messages:

```
System Generator will not properly function under this version of MATLAB!
```

```
Error occurred while attempting to install System Generator into MATLAB path.
```

If you are using a version of MATLAB that is too new, then you will see the following warning messages:

```
System Generator may not properly function under this version of MATLAB!
```

Hardware Co-Simulation Installation

This topic provides links to hardware and software installation procedures for hardware co-simulation. If you do not plan to use hardware co-simulation, you may skip this topic.

Ethernet-Based Hardware Co-Simulation

[Installing an ML402 Board for Ethernet Hardware Co-Simulation](#)

[Installing an ML560 Board for Ethernet Hardware Co-Simulation](#)

[Installing an ML650 Board for Ethernet Hardware Co-Simulation](#)

[Installing a Spartan-3A DSP 1800A Starter Board for Ethernet Hardware Co-Simulation](#)

[Installing a Spartan-3A DSP 3400A Development Board for Ethernet Hardware Co-Simulation](#)

[Installing an SP601/SP605 Board for Ethernet Hardware Co-Simulation](#)

Note: If installation instructions for your particular platform are not provided here, please refer to the installation instructions that come with your Platform Kit. For instructions on how to install a Xilinx USB Cable and cable driver software on a Windows or Linux Operating System, refer to the Xilinx document titled: [USB Cable Installation Guide](#)

JTAG-Based Hardware Co-Simulation

[Installing an ML402 Board for JTAG Hardware Co-Simulation](#)

[Installing an ML605 Board for JTAG Hardware Co-Simulation](#)

[Installing an SP601/SP605 Board for JTAG Hardware Co-Simulation](#)

Third-Party Hardware Co-Simulation

As part of the Xilinx XtremeDSP™ Initiative, Xilinx works with distributors and many OEMs to provide a variety of DSP prototyping and development platforms. Please refer to the following Xilinx web site page for more information on available platforms:

http://www.xilinx.com/products/boards_kits/index.htm

Compiling Xilinx HDL Libraries

If you intend to simulate System Generator designs using ModelSim, you must compile your IP (cores) libraries. This topic describes the procedure.

ModelSim SE

The Xilinx tool that compiles libraries for use in ModelSim SE is named **compplib**. The following command can, for example, be used to compile all the VHDL and Verilog libraries with ModelSim SE:

```
compplib -s mti_se -f all -l all
```

Complete instructions for running compplib can be found in the ISE Software Manual titled “Command Line Tool User Guide”.

Configuring the System Generator Cache

Both the System Generator simulator and the design generator incorporate a disk cache to speed up the iterative design process. The cache does this by tagging and storing files related to simulation and generation, then recalling those files during subsequent simulation and generation rather than rerunning the time consuming tools used to create those files.

Setting the Size

By default, the cache will use up to 500 MB of disk space to store files. To specify the amount of disk space the cache should use, set the `SYSGEN_CACHE_SIZE` environment variable to the size of the cache in megabytes. Set this number to a higher value when working on several large designs.

Setting the Number of Entries

The cache entry database stores a fixed number of entries. The default is 20,000 entries. To set size of the cache entry database, set the `SYSGEN_CACHE_ENTRIES` environment

variable to the desired number of entries. Setting this number too small will adversely affect cache performance. Set this number to a higher value when working on several large designs.

You can use the `xlCache` function to manage and inspect the properties of difference caches used by System Generator. A detailed description of this function can be found under the topic [System Generator Utilities](#).

Displaying and Changing Versions of System Generator

It is possible to have several versions of System Generator installed. The MATLAB command `xlVersion` displays which versions are installed, and makes it possible to switch from one to another. `xlVersion` is useful when upgrading a model to run in the latest version of System Generator.

Entering "xlVersion" in the MATLAB console displays the version of System Generator that is installed.

```
Available System Generator installations:  
Version 13.1.4000 in C:/Xilinx/13.1/ISE_DS/ISE/sysgen  
Current version of System Generator is 13.1.4000
```


Release Information

System Generator for DSP release information can now be found in the following Web-based document:

[ISE Design Suite 13: Release Notes Guide](#)