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EFR32FG1 Flex Gecko Proprietary Protocol SoC Family Data Sheet

The Flex Gecko proprietary protocol family of SoCs is part of the Wireless Gecko portfolio. Flex Gecko SoCs are ideal for enabling energy-friendly proprietary protocol networking for IoT devices.

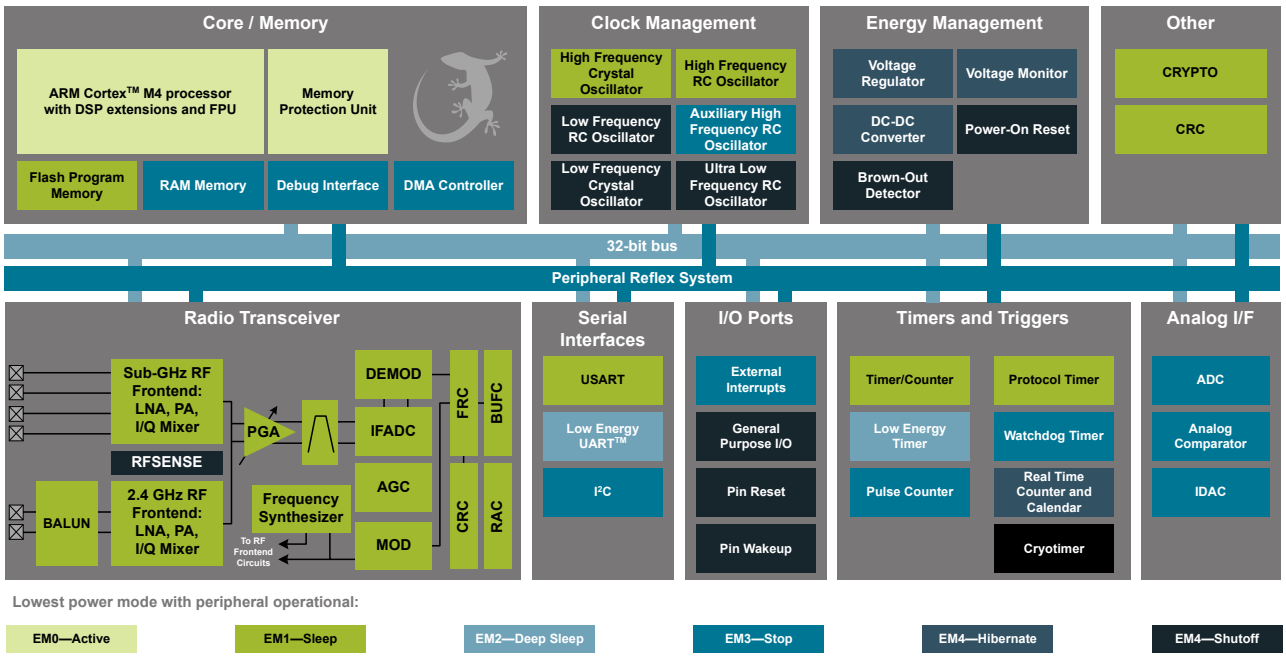
The single-die solution provides industry-leading energy efficiency, ultra-fast wakeup times, a scalable power amplifier, an integrated balun and no-compromise MCU features.

Flex Gecko applications include:

- Home and Building Automation and Security
- Metering
- Electronic Shelf Labels
- Industrial Automation
- Commercial and Retail Lighting and Sensing

KEY FEATURES

- 32-bit ARM® Cortex®-M4 core with 40 MHz maximum operating frequency
- Scalable Memory and Radio configuration options available in several footprint compatible QFN packages
- 12-channel Peripheral Reflex System enabling autonomous interaction of MCU peripherals
- Autonomous Hardware Crypto Accelerator and Random Number Generator
- Integrated balun for 2.4 GHz and integrated PA with up to 19.5 dBm transmit power for 2.4 GHz and 20 dBm transmit power for Sub-GHz radios
- Integrated DC-DC with RF noise mitigation



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1. Feature List

The EFR32FG1 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**.
  - High Performance 32-bit 40 MHz ARM Cortex®-M4 with DSP instruction and floating-point unit for efficient signal processing
  - Up to 256 kB flash program memory
  - Up to 32 kB RAM data memory
  - 2.4 GHz and Sub-GHz radio operation
  - Transmit power:
    - 2.4 GHz radio: Up to 19.5 dBm
    - Sub-GHz radio: Up to 20 dBm
- **Low Energy Consumption**
  - 8.7 mA RX current at 2.4 GHz
  - 8.2 mA TX current @ 0 dBm output power at 2.4 GHz
  - 8.1 mA RX current at 868 MHz
  - 34.5 mA TX current @ 14 dBm output power at 868 MHz
  - 63 µA/MHz in Active Mode (EM0)
  - 1.4 µA EM2 DeepSleep current (full RAM retention and RTCC running from LFXO)
  - 0.58 µA EM4H Hibernate Mode (128 byte RAM retention)
  - Wake on Radio with signal strength detection, preamble pattern detection, frame detection and timeout
- **High Receiver Performance**
  - -94 dBm sensitivity @ 1 Mbit/s GFSK (2.4GHz)
  - -121.4 dBm sensitivity at 2.4 kbps GFSK (868 MHz)
- **Supported Modulation Formats**
  - 2-FSK / 4-FSK with fully configurable shaping
  - Shaped OQPSK / (G)MSK
  - Configurable DSSS and FEC
  - BPSK / DBPSK TX
  - OOK / ASK
- **Supported Protocols:**
  - Proprietary Protocols
  - Wireless M-Bus
  - Low Power Wide Area Networks
- **Support for Internet Security**
  - General Purpose CRC
  - Random Number Generation
  - Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **Wide selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2× Analog Comparator (ACMP)
  - Digital to Analog Current Converter (IDAC)
  - Up to 32 pins connected to analog channels (APORT) shared between Analog Comparators, ADC, and IDAC
  - Up to 32 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2×16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 16-bit Pulse Counter with asynchronous operation
  - Watchdog Timer with dedicated RC oscillator @ 50nA
  - 2×Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - Low Energy UART (LEUART™)
  - I^2C interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
  - 1.85 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - -40 °C to 85 °C
- **QFN32 5x5 mm Package**
- **QFN48 7x7 mm Package**

2. Ordering Information

Ordering Code	Protocol Stack	Frequency Band @ Max TX Power	Flash (kB)	RAM (kB)	GPIO	Package
EFR32FG1P133F256GM48-C0	Proprietary	• 2.4 GHz @ 19.5 dBm • Sub-GHz @ 20 dBm	256	32	28	QFN48
EFR32FG1P133F128GM48-C0	Proprietary	• 2.4 GHz @ 19.5 dBm • Sub-GHz @ 20 dBm	128	32	28	QFN48
EFR32FG1P133F64GM48-C0	Proprietary	• 2.4 GHz @ 19.5 dBm • Sub-GHz @ 20 dBm	64	16	28	QFN48
EFR32FG1P132F256GM48-C0	Proprietary	2.4 GHz @ 19.5 dBm	256	32	31	QFN48
EFR32FG1P132F128GM48-C0	Proprietary	2.4 GHz @ 19.5 dBm	128	32	31	QFN48
EFR32FG1P132F64GM48-C0	Proprietary	2.4 GHz @ 19.5 dBm	64	16	31	QFN48
EFR32FG1P132F256GM32-C0	Proprietary	2.4 GHz @ 19.5 dBm	256	32	16	QFN32
EFR32FG1P132F128GM32-C0	Proprietary	2.4 GHz @ 19.5 dBm	128	32	16	QFN32
EFR32FG1P132F64GM32-C0	Proprietary	2.4 GHz @ 19.5 dBm	64	16	16	QFN32
EFR32FG1P131F256GM48-C0	Proprietary	Sub-GHz @ 20 dBm	256	32	32	QFN48
EFR32FG1P131F128GM48-C0	Proprietary	Sub-GHz @ 20 dBm	128	32	32	QFN48
EFR32FG1P131F64GM48-C0	Proprietary	Sub-GHz @ 20 dBm	64	16	32	QFN48
EFR32FG1P131F256GM32-C0	Proprietary	Sub-GHz @ 20 dBm	256	32	16	QFN32
EFR32FG1P131F128GM32-C0	Proprietary	Sub-GHz @ 20 dBm	128	32	16	QFN32
EFR32FG1P131F64GM32-C0	Proprietary	Sub-GHz @ 20 dBm	64	16	16	QFN32
EFR32FG1V132F256GM48-C0	Proprietary	2.4 GHz @ 16.5 dBm	256	32	31	QFN48
EFR32FG1V132F128GM48-C0	Proprietary	2.4 GHz @ 16.5 dBm	128	16	31	QFN48
EFR32FG1V132F64GM48-C0	Proprietary	2.4 GHz @ 16.5 dBm	64	16	31	QFN48
EFR32FG1V132F32GM48-C0	Proprietary	2.4 GHz @ 16.5 dBm	32	8	31	QFN48
EFR32FG1V132F256GM32-C0	Proprietary	2.4 GHz @ 16.5 dBm	256	32	16	QFN32
EFR32FG1V132F128GM32-C0	Proprietary	2.4 GHz @ 16.5 dBm	128	16	16	QFN32
EFR32FG1V132F64GM32-C0	Proprietary	2.4 GHz @ 16.5 dBm	64	16	16	QFN32
EFR32FG1V132F32GM32-C0	Proprietary	2.4 GHz @ 16.5 dBm	32	8	16	QFN32
EFR32FG1V131F256GM48-C0	Proprietary	Sub-GHz @ 16.5 dBm	256	32	32	QFN48
EFR32FG1V131F128GM48-C0	Proprietary	Sub-GHz @ 16.5 dBm	128	16	32	QFN48
EFR32FG1V131F64GM48-C0	Proprietary	Sub-GHz @ 16.5 dBm	64	16	32	QFN48
EFR32FG1V131F32GM48-C0	Proprietary	Sub-GHz @ 16.5 dBm	32	8	32	QFN48
EFR32FG1V131F256GM32-C0	Proprietary	Sub-GHz @ 16.5 dBm	256	32	16	QFN32
EFR32FG1V131F128GM32-C0	Proprietary	Sub-GHz @ 16.5 dBm	128	16	16	QFN32
EFR32FG1V131F64GM32-C0	Proprietary	Sub-GHz @ 16.5 dBm	64	16	16	QFN32
EFR32FG1V131F32GM32-C0	Proprietary	Sub-GHz @ 16.5 dBm	32	8	16	QFN32
EFR32FG1V032F256GM32-C0	Proprietary	2.4 GHz @ 8 dBm	256	32	16	QFN32

Ordering Code	Protocol Stack	Frequency Band @ Max TX Power	Flash (kB)	RAM (kB)	GPIO	Package
EFR32FG1V032F128GM32-C0	Proprietary	2.4 GHz @ 8 dBm	128	16	16	QFN32

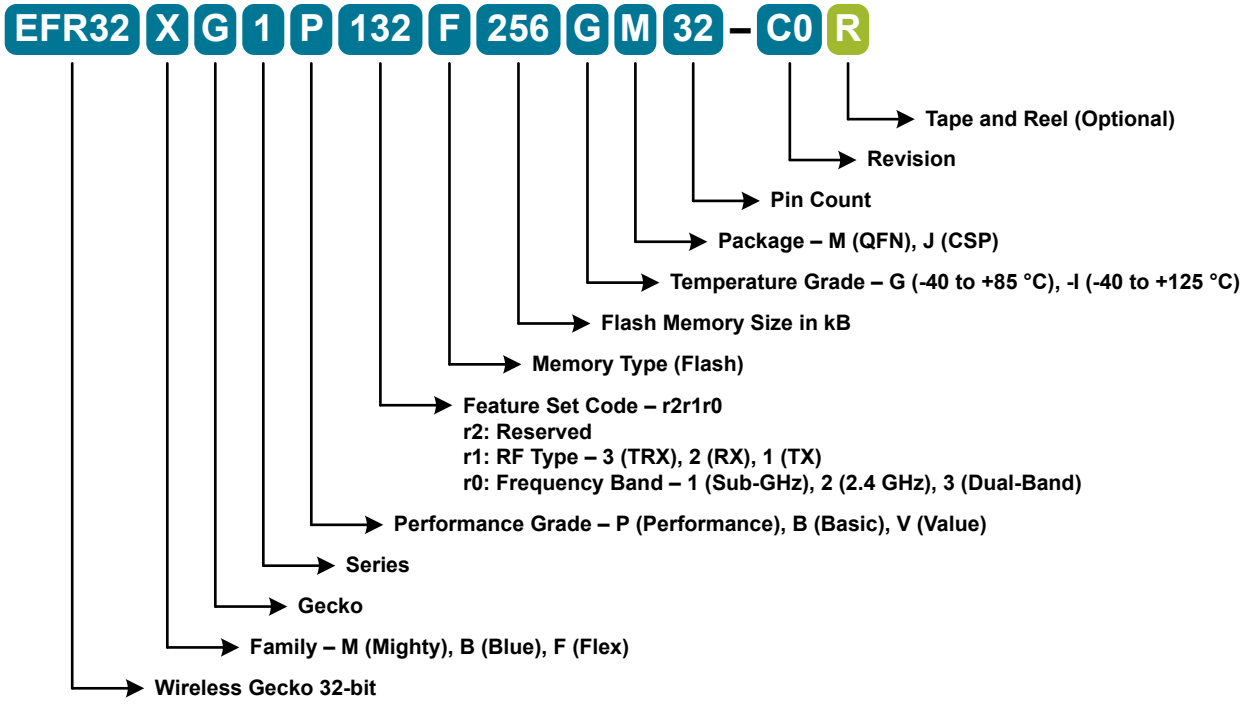

Figure 2.1. OPN Decoder

3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a highly integrated radio transceiver. The devices are well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32 Reference Manual.

A block diagram of the EFR32FG1 family is shown in Figure 3.1 Detailed EFR32FG1 Block Diagram on page 4. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

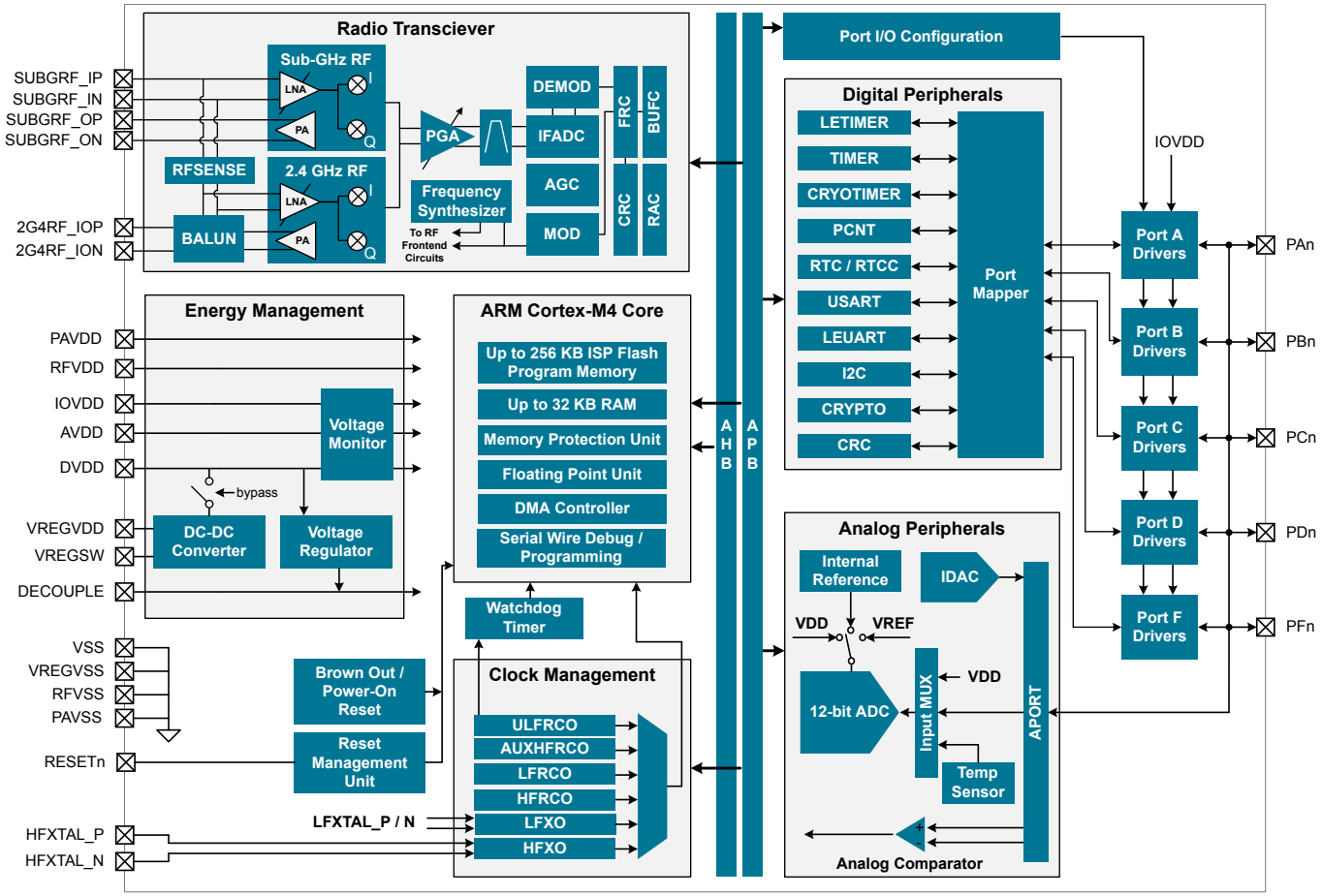

Figure 3.1. Detailed EFR32FG1 Block Diagram

3.2 Radio

The Flex Gecko family features a radio transceiver supporting proprietary wireless protocols.

3.2.1 Antenna Interface

The EFR32FG1 family includes devices which support both single-band and dual-band RF communication over separate physical RF interfaces.

The 2.4 GHz antenna interface consists of two pins (2G4RF_IOP and 2G4RF_ION) that interface directly to the on-chip BALUN. The 2G4RF_ION pin should be grounded externally.

The sub-GHz antenna interface consists of a differential transmit interface (pins SUBGRF_OP and SUBGRF_ON) and a differential receive interface (pinsSUBGRF_IP and SUBGRF_IN).

The external components and power supply connections for the antenna interface typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32FG1 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency used by the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance combined with frequency resolution better than 100 Hz, with low energy consumption. The synthesizer has fast frequency settling which allows very short receiver and transmitter wake up times to optimize system energy consumption.

3.2.3 Receiver Architecture

The EFR32FG1 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer, employing a crystal reference. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance. The sub-GHz radio can be calibrated on-demand by the user for the desired frequency band.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

The EFR32FG1 features integrated support for antenna diversity to improve link budget for 802.15.4 DSSS-OQPSK PHY configuration in the 2.4GHz band, using complementary control outputs to an external switch. Internal configurable hardware controls automatic switching between antennae during RF receive detection operations.

3.2.4 Transmitter Architecture

The EFR32FG1 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32FG1. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Wake on Radio

The Wake on Radio feature allows flexible, autonomous RF sensing, qualification, and demodulation without required MCU activity, using a subsystem of the EFR32FG1 including the Radio Controller (RAC), Peripheral Reflex System (PRS), and Low Energy peripherals.

3.2.6 RFSENSE

The RFSENSE module generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.2.7 Flexible Frame Handling

EFR32FG1 has an extensive and flexible frame handling support for easy implementation of even complex communication protocols. The Frame Controller (FRC) supports all low level and timing critical tasks together with the Radio Controller and Modulator/Demodulator:

- Highly adjustable preamble length
- Up to 2 simultaneous synchronization words, each up to 32 bits and providing separate interrupts
- Frame disassembly and address matching (filtering) to accept or reject frames
- Automatic ACK frame assembly and transmission
- Fully flexible CRC generation and verification:
  - Multiple CRC values can be embedded in a single frame
  - 8, 16, 24 or 32-bit CRC value
  - Configurable CRC bit and byte ordering
- Selectable bit-ordering (least significant or most significant bit first)
- Optional data whitening
- Optional Forward Error Correction (FEC), including convolutional encoding / decoding and block encoding / decoding
- Half rate convolutional encoder and decoder with constraint lengths from 2 to 7 and optional puncturing
- Optional symbol interleaving, typically used in combination with FEC
- Symbol coding, such as Manchester or DSSS, or biphase space encoding using FEC hardware
- UART encoding over air, with start and stop bit insertion / removal
- Test mode support, such as modulated or unmodulated carrier output
- Received frame timestamping

3.2.8 Packet and State Trace

The EFR32FG1 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.9 Data Buffering

The EFR32FG1 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.10 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32FG1. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.2.11 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The EFR32FG1 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

AVDD and VREGVDD need to be 1.85 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.4 General Purpose Input/Output (GPIO)

EFR32FG1 has up to 32 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32FG1. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal and External Oscillators

The EFR32FG1 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

3.6.3 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.4 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.5 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 µA and 64 µA with several ranges consisting of various step sizes.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32FG1. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 256 kB flash program memory
- Up to 32 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller features 8 channels capable of performing memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The EFR32FG1 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

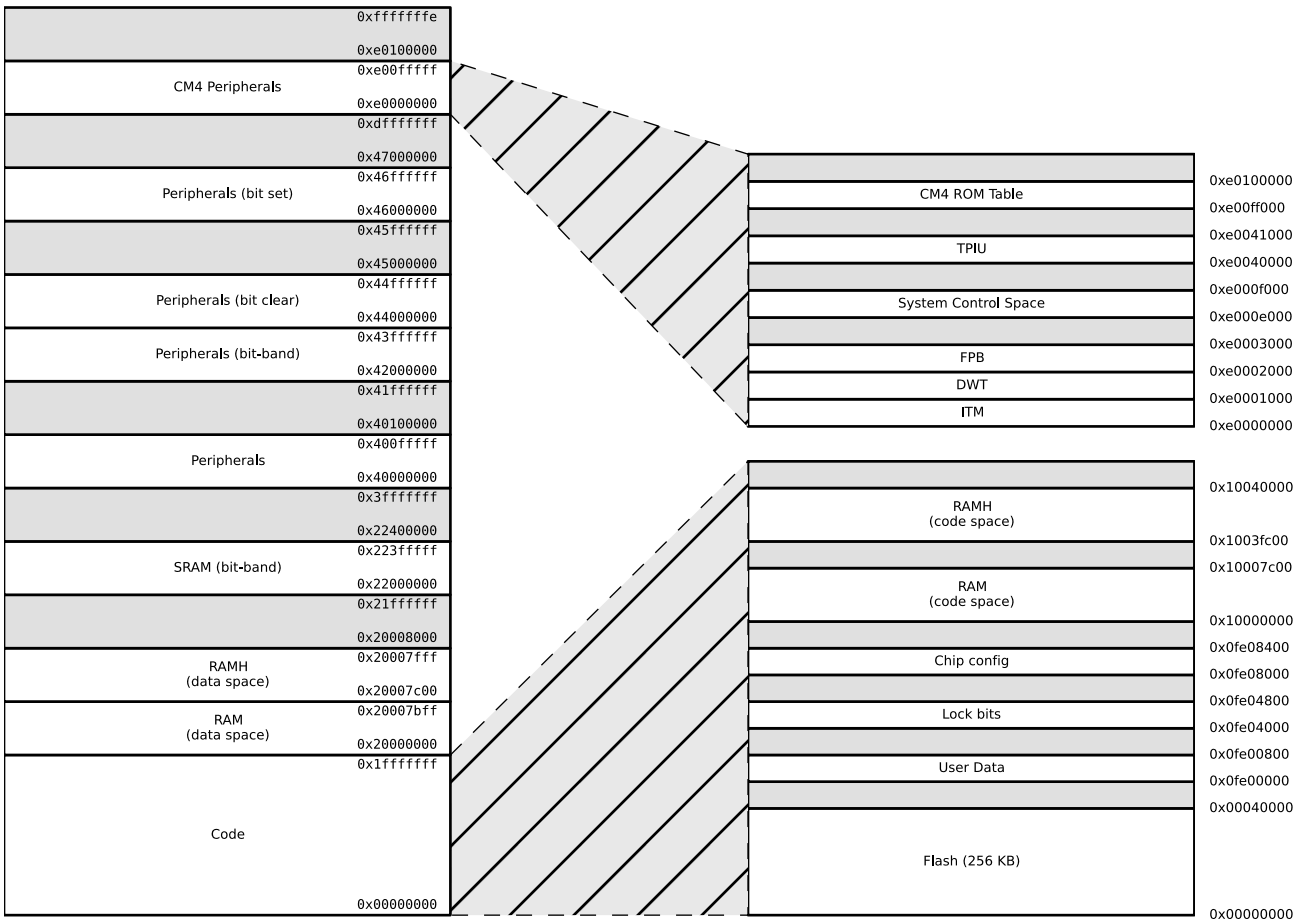

Figure 3.2. EFR32FG1 Memory Map — Core Peripherals and Code Space

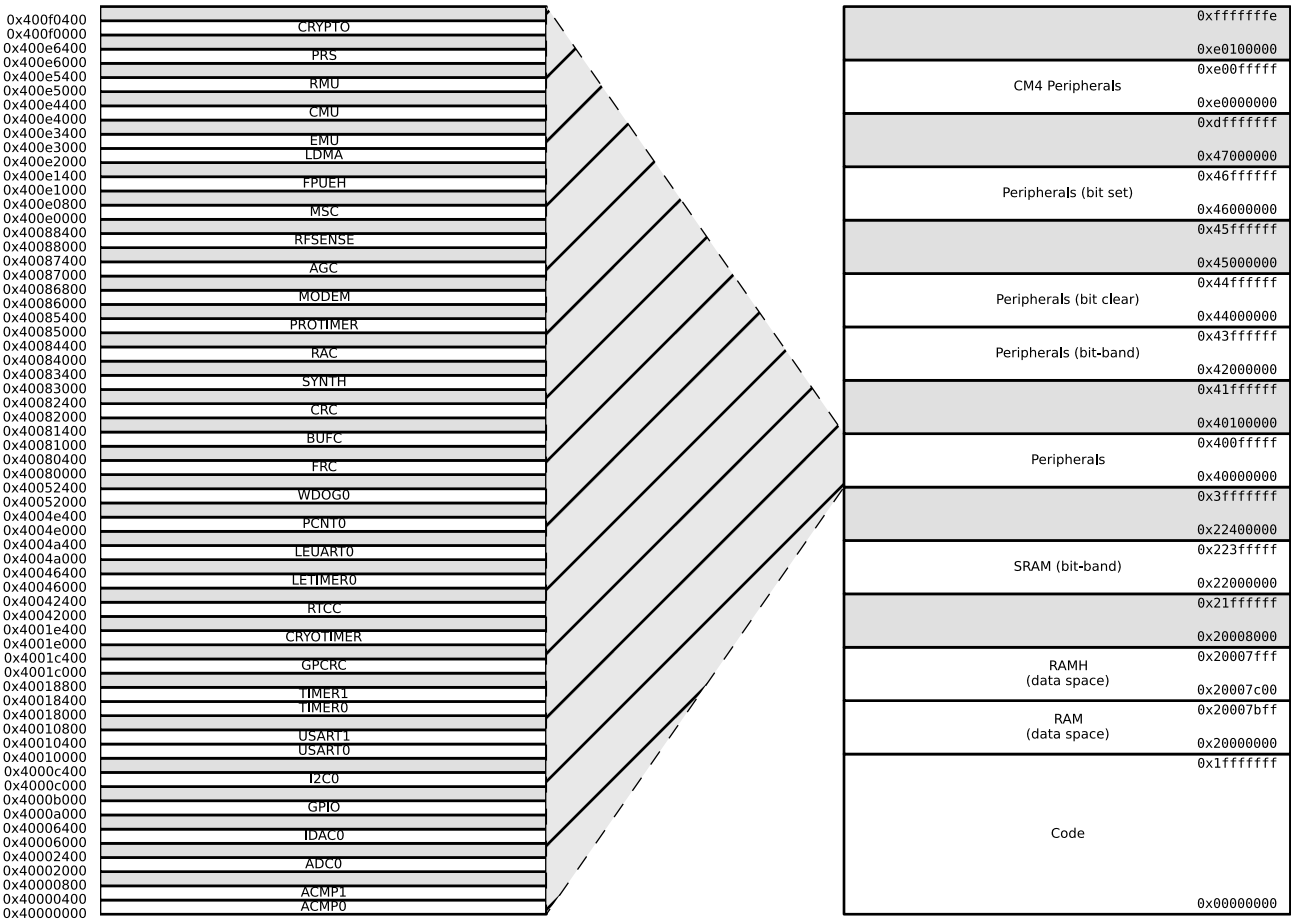

Figure 3.3. EFR32FG1 Memory Map — Peripherals

3.13 Configuration Summary

The features of the EFR32FG1 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.1. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	IrDA I^2S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
TIMER0	with DTI.	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1		TIM1_CC[3:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to Table 4.2 General Operating Conditions on page 17 for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
External main supply voltage ramp rate	$V_{DDRAMPMAX}$		—	—	1	V / µs
Voltage on any 5V tolerant GPIO pin[1]	V_{DIGPIN}		-0.3	—	Min of 5.25 and IOVDD +2	V
Voltage on non-5V tolerant GPIO pins			-0.3	—	IOVDD+0.3	V
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.4	V
Input RF level on pins 2G4RF_IOP and 2G4RF_ION	$P_{RFMAX2G4}$		—	—	10	dBm
Voltage differential between RF pins (2G4RF_IOP - 2G4RF_ION)	$V_{MAXDIFF2G4}$		-50	—	50	mV
Absolute Voltage on RF pins 2G4RF_IOP and 2G4RF_ION	V_{MAX2G4}		-0.3	—	3.3	V
Input RF level on pins SUBGRF_IP and SUBGRF_IN	$P_{RFMAXSUBG}$		—	—	10	dBm
Voltage differential between RF pins (SUBGRF_IP - SUBGRF_IN)	$V_{MAXDIFFSUBG}$		-50	—	50	mV
Absolute Voltage on RF pins SUBGRF_IP, SUBGRF_IN, SUBGRF_OP, and SUBGRF_ON	$V_{MAXSUBG}$		-0.3	—	3.3	V
Total current into VDD power lines (source)	I_{VDDMAX}		—	—	200	mA
Total current into VSS ground lines (sink)	I_{VSSMAX}		—	—	200	mA
Current per I/O pin (sink)	I_{IOMAX}		—	—	50	mA
Current per I/O pin (source)			—	—	50	mA
Current for all I/O pins (sink)	$I_{IOALLMAX}$		—	—	200	mA
Current for all I/O pins (source)			—	—	200	mA
Voltage difference between AVDD and VREGVDD	ΔV_{DD}		—	—	0.3	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Junction Temperature	T_J		-40	—	105	°C

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be the highest voltage in the system
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD
- RFVDD ≤ AVDD
- PAVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating temperature range	T_{OP}	-G temperature grade, Ambient Temperature	-40	25	85	°C
AVDD Supply voltage[1]	V_{AVDD}		1.85	3.3	3.8	V
VREGVDD Operating supply voltage[1 2]	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.85	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.85	3.3	3.8	V
VREGVDD Current	$I_{VREGVDD}$	DCDC in bypass	—	—	200	mA
RFVDD Operating supply voltage	V_{RFVDD}		1.62	—	$V_{VREGVDD}$	V
DVDD Operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
PAVDD Operating supply voltage	V_{PAVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD Operating supply voltage	V_{IOVDD}		1.62	—	$V_{VREGVDD}$	V
Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD)	dV_{DD}		—	—	0.1	V
HFCLK frequency	f_{CORE}	0 wait-states (MODE = WS0) [3]	—	—	26	MHz
		1 wait-states (MODE = WS1) [3]	—	—	40	MHz

Note:

1. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
2. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$
3. In MSC_READCTRL register

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	$THETA_{JA}$	QFN32 Package, 2-Layer PCB, Air velocity = 0 m/s	—	79	—	°C/W
		QFN32 Package, 2-Layer PCB, Air velocity = 1 m/s	—	62.2	—	°C/W
		QFN32 Package, 2-Layer PCB, Air velocity = 2 m/s	—	54.1	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 0 m/s	—	32	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 1 m/s	—	28.1	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 2 m/s	—	26.9	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 0 m/s	—	64.5	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 1 m/s	—	51.6	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 2 m/s	—	47.7	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 0 m/s	—	26.2	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 1 m/s	—	23.1	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 2 m/s	—	22.1	—	°C/W

4.1.4 DC-DC Converter

Test conditions: L_{DCDC}=4.7 µH (Murata LQH3NPN4R7MM0L), C_{DCDC}=1.0 µF (Murata GRM188R71A105KA61D), V_{DCDC_I}=3.3 V, V_{DCDC_O}=1.8 V, I_{DCDC_LOAD}=50 mA, Heavy Drive configuration, F_{DCDC_LN}=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.85	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC Accuracy	ACC_{DC}	Low noise (LN) mode, 1.8 V target output	1.7	—	1.9	V
Regulation Window[2]	WIN_{REG}	Low power (LP) mode, LPCMPBIAS[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 µA	1.63	—	2.2	V
		Low power (LP) mode, LPCMPBIAS[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	1.63	—	2.1	V
Steady-state output ripple	V_R	Radio disabled.	—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	—	150	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	—	150	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	50	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	125	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive[4]	—	—	200	mA
		Low noise (LN) mode, Medium Drive[4]	—	—	100	mA
		Low noise (LN) mode, Light Drive[4]	—	—	50	mA
		Low power (LP) mode, LPCMPBIAS[3] = 0	—	—	75	µA
		Low power (LP) mode, LPCMPBIAS[3] = 3	—	—	10	mA
DCDC nominal output capacitor	C_{DCDC}	25% tolerance	1	1	1	µF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	µH
Resistance in Bypass mode	R_{BYP}		—	1.2	2.5	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$
2. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits
3. In EMU_DCDCMISCCTRL register
4. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.