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EFR32MG13 Mighty Gecko Multi-Protocol Wireless SoC Family Data Sheet

The Mighty Gecko multi-protocol family of SoCs is part of the Wireless Gecko portfolio. Mighty Gecko SoCs are ideal for enabling energy-friendly multi-protocol, multi-band networking for IoT devices.

The single-die solution provides industry-leading energy efficiency, ultra-fast wakeup times, a scalable power amplifier, and no-compromise MCU features.

Mighty Gecko applications include:

- IoT Multi-Protocol Devices
- Connected Home
- Lighting
- Health and Wellness
- Metering
- Home and Building Automation and Security

KEY FEATURES

- 32-bit ARM® Cortex®-M4 core with 40 MHz maximum operating frequency
- 512 kB of flash and 64 kB of RAM
- Pin-compatible across EFR32MG families (exceptions apply for 5V-tolerant pins)
- 12-channel Peripheral Reflex System enabling autonomous interaction of MCU peripherals
- Autonomous Hardware Crypto Accelerator and True Random Number Generator
- Integrated PA with up to 19 dBm (2.4 GHz) or 20 dBm (Sub-GHz) tx power
- Integrated balun for 2.4 GHz
- Robust peripheral set and up to 31 GPIO
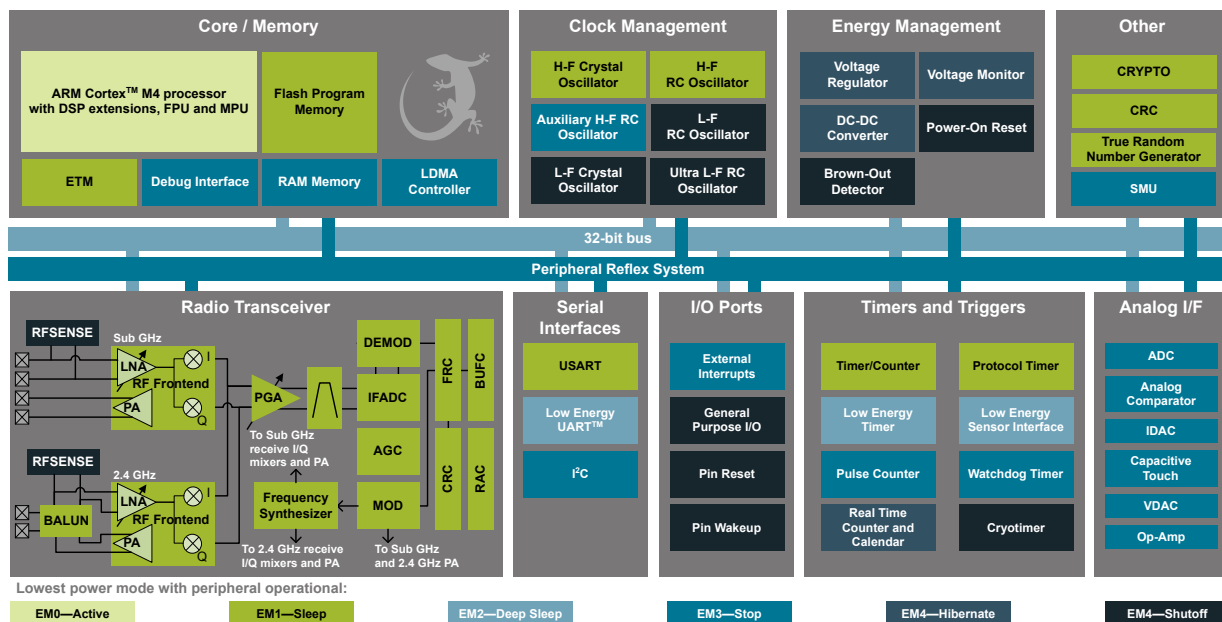
1. Feature List

The EFR32MG13 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**
  - High Performance 32-bit 40 MHz ARM Cortex®-M4 with DSP instruction and floating-point unit for efficient signal processing
  - Embedded Trace Macrocell (ETM) for advanced debugging
  - 512 kB flash program memory
  - 64 kB RAM data memory
  - 2.4 GHz and Sub-GHz radio operation
  - Transmit power:
    - 2.4 GHz radio: Up to 19 dBm
    - Sub-GHz radio: Up to 20 dBm
- **Low Energy Consumption**
  - 10.2 mA RX current at 250 kbps, DSSS-OQPSK, 2.4 GHz
  - 9.5 mA RX current at 1 Mbps, GFSK, 2.4 GHz
  - 8.4 mA RX current at 38.4 kbps, GFSK, 169 MHz
  - 8.5 mA TX current at 0 dBm output power at 2.4 GHz
  - 35.3 mA TX current at 14 dBm output power at 868 MHz
  - 69 µA/MHz in Active Mode (EM0)
  - 1.3 µA EM2 DeepSleep current (16 kB RAM retention and RTCC running from LFRCO)
  - Wake on Radio with signal strength detection, preamble pattern detection, frame detection and timeout
- **High Receiver Performance**
  - -103.3 dBm sensitivity at 125 kbit/s GFSK, 2.4 GHz
  - -94.8 dBm sensitivity at 1 Mbit/s GFSK, 2.4 GHz
  - -91.5 dBm sensitivity at 2 Mbit/s GFSK, 2.4 GHz
  - -102.7 dBm sensitivity at 250 kbps DSSS-OQPSK, 2.4 GHz
  - -126.2 dBm sensitivity at 600 bps, GFSK, 915 MHz
  - -120.6 dBm sensitivity at 2.4 kbps, GFSK, 868 MHz
  - -107.4 dBm sensitivity at 4.8 kbps, OOK, 433 MHz
  - -112.2 dBm sensitivity at 38.4 kbps, GFSK, 169 MHz
- **Supported Modulation Formats**
  - 2/4 (G)FSK with fully configurable shaping
  - BPSK / DBPSK TX
  - OOK / ASK
  - Shaped OQPSK / (G)MSK
  - Configurable DSSS and FEC
- **Supported Protocols**
  - Zigbee
  - Thread
  - Bluetooth® Low Energy (Bluetooth 5)
  - Proprietary Protocols
  - Wireless M-Bus
  - Selected IEEE 802.15.4g SUN-FSK PHYs
  - Low Power Wide Area Networks
- **Suitable for Systems Targeting Compliance With:**
  - FCC Part 90.210 Mask D, FCC part 15.247, 15.231, 15.249
  - ETSI Category I Operation, EN 300 220, EN 300 328
  - ARIB T-108, T-96
  - China regulatory

- **Wide selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2 × Analog Comparator (ACMP)
  - 2 × Digital to Analog Converter (VDAC)
  - 3 × Operational Amplifier (Opamp)
  - Digital to Analog Current Converter (IDAC)
  - Low-Energy Sensor Interface (LESENSE)
  - Multi-channel Capacitive Sense Interface (CSEN)
  - Up to 31 pins connected to analog channels (APORT) shared between analog peripherals
  - Up to 31 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2 × 16-bit Timer/Counter
    - 3 or 4 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter
    - 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 16-bit Pulse Counter with asynchronous operation
  - 2 × Watchdog Timer with dedicated RC oscillator
  - 3 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^{2}S)
  - Low Energy UART (LEUART™)
  - 2 × I^{2}C interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - Standard (-40 °C to 85 °C) and Extended (-40 °C to 125 °C) temperature grades available
- **Support for Internet Security**
  - General Purpose CRC
  - True Random Number Generator
  - 2 × Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **QFN32 5x5 mm Package**
- **QFN48 7x7 mm Package**

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Frequency Band @ Max TX Power	Flash (kB)	RAM (kB)	GPIO	Package	Temp Range
EFR32MG13P733F512GM48-C	• Bluetooth Low Energy • Zigbee • Thread • Proprietary • Multiproto-col	• 2.4 GHz @ 19 dBm • Sub-GHz @ 20 dBm	512	64	28	QFN48	-40 to +85°C
EFR32MG13P733F512IM48-C	• Bluetooth Low Energy • Zigbee • Thread • Proprietary • Multiproto-col	• 2.4 GHz @ 19 dBm • Sub-GHz @ 20 dBm	512	64	28	QFN48	-40 to +125°C
EFR32MG13P732F512GM48-C	• Bluetooth Low Energy • Zigbee • Thread • Proprietary • Multiproto-col	2.4 GHz @ 19 dBm	512	64	31	QFN48	-40 to +85°C
EFR32MG13P732F512IM48-C	• Bluetooth Low Energy • Zigbee • Thread • Proprietary • Multiproto-col	2.4 GHz @ 19 dBm	512	64	31	QFN48	-40 to +125°C
EFR32MG13P732F512GM32-C	• Bluetooth Low Energy • Zigbee • Thread • Proprietary • Multiproto-col	2.4 GHz @ 19 dBm	512	64	16	QFN32	-40 to +85°C
EFR32MG13P732F512IM32-C	• Bluetooth Low Energy • Zigbee • Thread • Proprietary • Multiproto-col	2.4 GHz @ 19 dBm	512	64	16	QFN32	-40 to +125°C

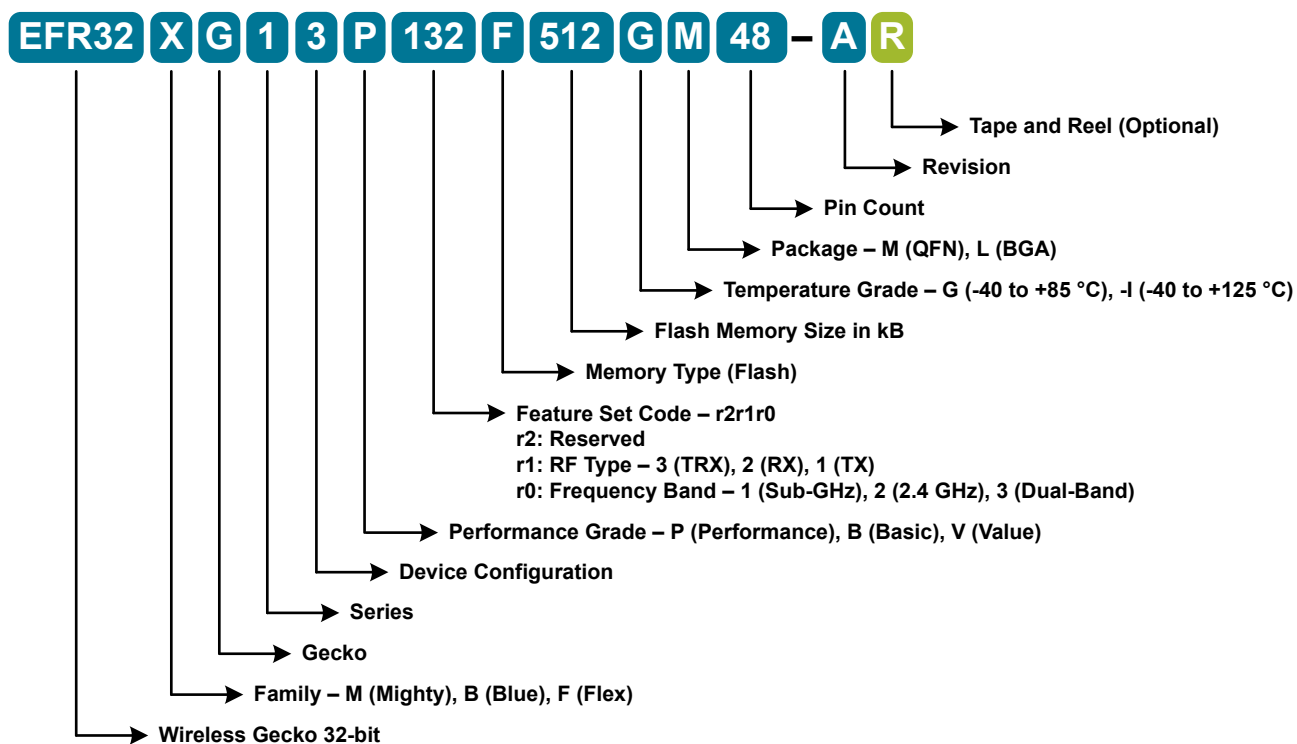| Ordering Code	Protocol Stack	Frequency Band @ Max TX Power	Flash (kB)	RAM (kB)	GPIO	Package	Temp Range
EFR32MG13P632F512GM48-C	• Bluetooth Low Energy • Zigbee • Thread • Proprietary • Multiproto-col	2.4 GHz @ 10 dBm	512	64	31	QFN48	-40 to +85°C
EFR32MG13P632F512GM32-C	• Bluetooth Low Energy • Zigbee • Thread • Proprietary • Multiproto-col	2.4 GHz @ 10 dBm	512	64	16	QFN32	-40 to +85°C

EFR32 X G 1 3 P 132 F 512 G M 48 – A R

Tape and Reel (Optional)

Revision

Pin Count

Package – M (QFN), L (BGA)

Temperature Grade – G (-40 to +85 °C), -I (-40 to +125 °C)

Flash Memory Size in kB

Memory Type (Flash)

Feature Set Code – r2r1r0
r2: Reserved
r1: RF Type – 3 (TRX), 2 (RX), 1 (TX)
r0: Frequency Band – 1 (Sub-GHz), 2 (2.4 GHz), 3 (Dual-Band)

Performance Grade – P (Performance), B (Basic), V (Value)

Device Configuration

Series

Gecko

Family – M (Mighty), B (Blue), F (Flex)

Wireless Gecko 32-bit

Figure 2.1. Ordering Code Key

Table of Contents

3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a highly integrated radio transceiver. The devices are well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32xG13 Reference Manual.

A block diagram of the EFR32MG13 family is shown in Figure 3.1 Detailed EFR32MG13 Block Diagram on page 8. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.
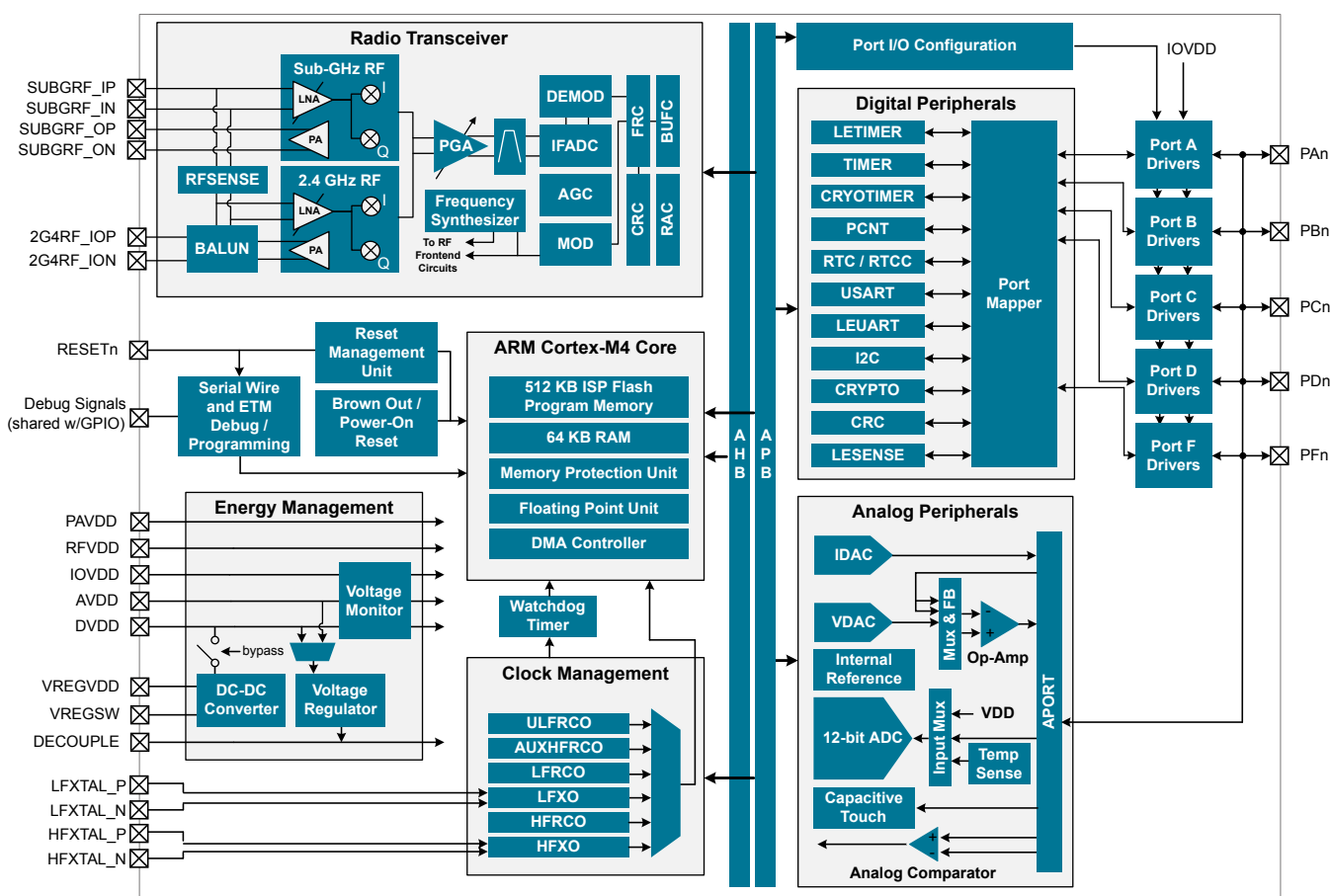

Figure 3.1. Detailed EFR32MG13 Block Diagram

3.2 Radio

The Mighty Gecko family features a highly configurable radio transceiver supporting a wide range of wireless protocols.

3.2.1 Antenna Interface

The EFR32MG13 family includes devices which support both single-band and dual-band RF communication over separate physical RF interfaces.

The 2.4 GHz antenna interface consists of two pins (2G4RF_IOP and 2G4RF_ION) that interface directly to the on-chip BALUN. The 2G4RF_ION pin should be grounded externally.

The sub-GHz antenna interface consists of a differential transmit interface (pins SUBGRF_OP and SUBGRF_ON) and a differential receive interface (pinsSUBGRF_IP and SUBGRF_IN).

The external components and power supply connections for the antenna interface typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32MG13 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency used by the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance combined with frequency resolution better than 100 Hz, with low energy consumption. The synthesizer has fast frequency settling which allows very short receiver and transmitter wake up times to optimize system energy consumption.

3.2.3 Receiver Architecture

The EFR32MG13 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer, employing a crystal reference. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance. The sub-GHz radio can be calibrated on-demand by the user for the desired frequency band.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS) for 2.4 GHz and sub-GHz bands.

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

The EFR32MG13 features integrated support for antenna diversity to mitigate the problem of frequency-selective fading due to multipath propagation and improve link budget. Support for antenna diversity is available for specific PHY configurations in 2.4 GHz and sub-GHz bands. Internal configurable hardware controls an external switch for automatic switching between antennae during RF receive detection operations.

Note: Due to the shorter preamble of 802.15.4 and BLE packets, RX diversity is not supported.

3.2.4 Transmitter Architecture

The EFR32MG13 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32MG13. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Wake on Radio

The Wake on Radio feature allows flexible, autonomous RF sensing, qualification, and demodulation without required MCU activity, using a subsystem of the EFR32MG13 including the Radio Controller (RAC), Peripheral Reflex System (PRS), and Low Energy peripherals.

3.2.6 RFSENSE

The RFSENSE module generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.2.7 Flexible Frame Handling

EFR32MG13 has an extensive and flexible frame handling support for easy implementation of even complex communication protocols. The Frame Controller (FRC) supports all low level and timing critical tasks together with the Radio Controller and Modulator/Demodulator:

- Highly adjustable preamble length
- Up to 2 simultaneous synchronization words, each up to 32 bits and providing separate interrupts
- Frame disassembly and address matching (filtering) to accept or reject frames
- Automatic ACK frame assembly and transmission
- Fully flexible CRC generation and verification:
  - Multiple CRC values can be embedded in a single frame
  - 8, 16, 24 or 32-bit CRC value
  - Configurable CRC bit and byte ordering
- Selectable bit-ordering (least significant or most significant bit first)
- Optional data whitening
- Optional Forward Error Correction (FEC), including convolutional encoding / decoding and block encoding / decoding
- Half rate convolutional encoder and decoder with constraint lengths from 2 to 7 and optional puncturing
- Optional symbol interleaving, typically used in combination with FEC
- Symbol coding, such as Manchester or DSSS, or biphase space encoding using FEC hardware
- UART encoding over air, with start and stop bit insertion / removal
- Test mode support, such as modulated or unmodulated carrier output
- Received frame timestamping

3.2.8 Packet and State Trace

The EFR32MG13 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.9 Data Buffering

The EFR32MG13 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.10 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32MG13. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.2.11 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The EFR32MG13 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFR32MG13 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.3.3 Power Domains

The EFR32MG13 has two peripheral power domains for operation in EM2 and lower. If all of the peripherals in a peripheral power domain are configured as unused, the power domain for that group will be powered off in the low-power mode, reducing the overall current consumption of the device.

Table 3.1. Peripheral Power Subdomains

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	CSEN
ADC0	VDAC0
LETIMER0	LEUART0
LESENSE	I2C0
APORT	I2C1
-	IDAC

3.4 General Purpose Input/Output (GPIO)

EFR32MG13 has up to 31 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32MG13. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal and External Oscillators

The EFR32MG13 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.6.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for application software.

3.6.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:
- ISO7816 SmartCards
- IrDA
- I^2S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART[TM] provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.7.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE^{TM} is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO1 block is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention.

CRYPTO also provides trigger signals for DMA read and write operations.

3.8.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.8.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.9.5 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 µA and 64 µA with several ranges consisting of various step sizes.

3.9.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.9.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32MG13. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:
- ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 512 kB flash program memory
- Up to 64 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The EFR32MG13 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

Figure 3.2. EFR32MG13 Memory Map — Core Peripherals and Code Space

0x400e6000	PRS
0x400e5400	RMU
0x400e5000	CMU
0x400e4400	EMU
0x400e4000	LDMA
0x400e3400	FPUEH
0x400e3000	MSC
0x400e2000	RFSENSE
0x400e1400	AGC
0x400e1000	MODEM
0x400e0800	PROTIMER
0x400e0000	RAC
0x40088400	SYNTH
0x40088000	CRC
0x40087400	BUFC
0x40087000	FRC
0x40086800	LESENSE
0x40086000	WDOG1
0x40085400	WDOG0
0x40085000	PCNT0
0x40084400	LEUART0
0x40084000	LETIMER0
0x40083400	PRORTC
0x40083000	RTCC
0x40082400	SMU
0x40082000	CSEN
0x40081400	CRYOTIMER
0x40081000	TRNG0
0x40080400	GPCRC
0x40080000	WTIMER0
0x40055400	TIMER1
0x40055000	TIMER0
0x40052800	USART2
0x40052400	USART1
0x40052000	USART0
0x4004e400	I2C1
0x4004e000	I2C0
0x4004a400	GPIO
0x4004a000	VDAC0
0x40046400	IDAC0
0x40046000	ADC0
0x40044400	ACMP1
0x40044000	ACMP0

Additional addresses:
0x40042400
0x40042000
0x40022400
0x40022000
0x4001f400
0x4001f000
0x4001e400
0x4001e000
0x4001d400
0x4001d000
0x4001c400
0x4001c000
0x4001a400
0x4001a000
0x40018800
0x40018400
0x40018000
0x40010c00
0x40010800
0x40010400
0x40010000
0x4000c800
0x4000c400
0x4000c000
0x4000b000
0x4000a000
0x40008400
0x40008000
0x40006400
0x40006000
0x40002400
0x40002000
0x40000800
0x40000400
0x40000000

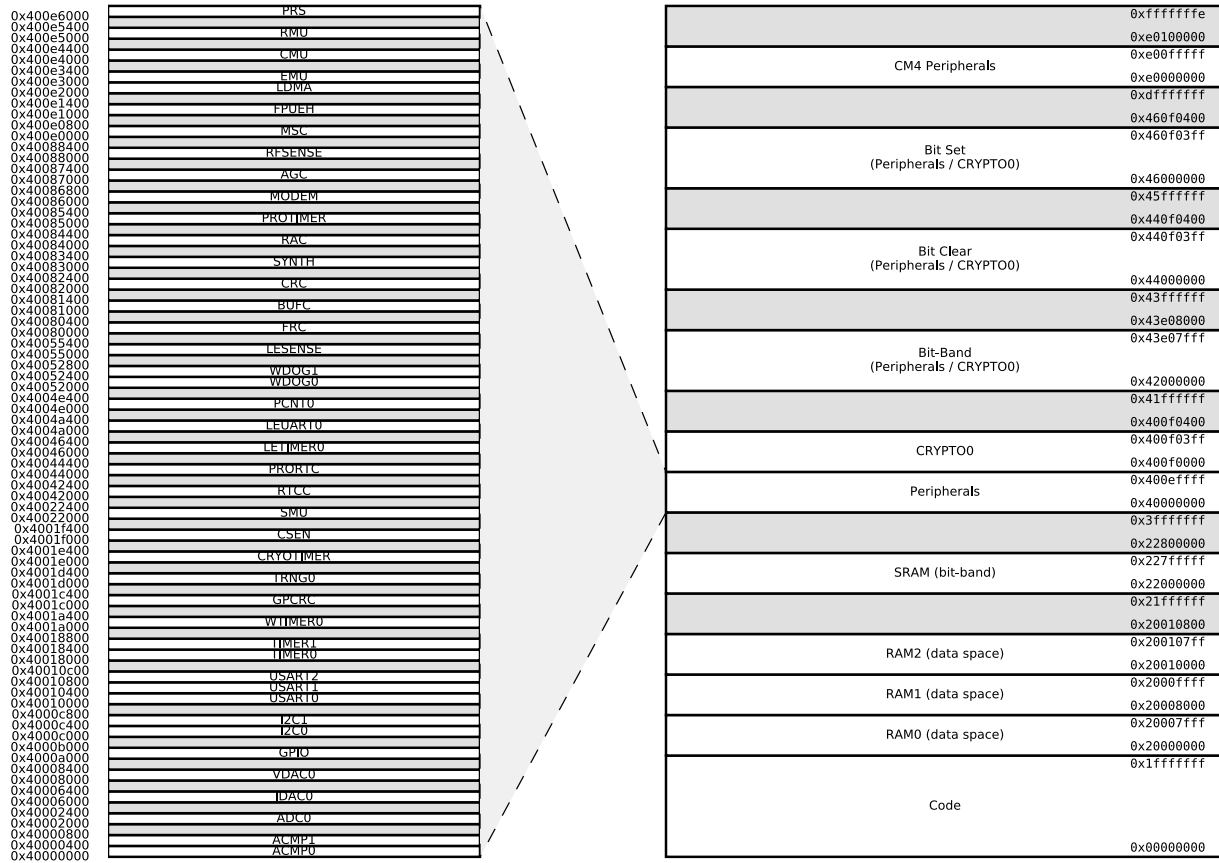| 0xffffffffe | |
0xe0100000	
0xe00fffff	CM4 Peripherals
0xe0000000	
0xdfffffff	
0x460f0400	
0x460f03ff	Bit Set (Peripherals / CRYPTO0)
0x46000000	
0x45ffffff	
0x440f0400	
0x440f03ff	Bit Clear (Peripherals / CRYPTO0)
0x44000000	
0x43ffffff	
0x43e08000	
0x43e07fff	Bit-Band (Peripherals / CRYPTO0)
0x42000000	
0x41ffffff	
0x400f0400	
0x400f03ff	CRYPTO0
0x400f0000	
0x400effff	Peripherals
0x40000000	
0x3fffffff	
0x22800000	
0x227fffff	SRAM (bit-band)
0x22000000	
0x21ffffff	
0x20010800	
0x200107ff	RAM2 (data space)
0x20010000	
0x2000ffff	RAM1 (data space)
0x20008000	
0x20007fff	RAM0 (data space)
0x20000000	
0x1fffffff	
	Code
0x00000000	

Figure 3.3. EFR32MG13 Memory Map — Peripherals

3.13 Configuration Summary

The features of the EFR32MG13 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	I^2S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	IrDA SmartCard	US2_TX, US2_RX, US2_CLK, US2_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	-	TIM1_CC[3:0]
WTIMER0	with DTI	WTIM0_CC[2:0], WTIM0_CDTI[2:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω source or load.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to 4.1.2.1 General Operating Conditions for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1	V / µs
DC voltage on any GPIO pin	V_{DIGPIN}	5V tolerant GPIO pins[1] [2] [3]	-0.3	—	Min of 5.25 and IOVDD +2	V
		Standard GPIO pins	-0.3	—	IOVDD+0.3	V
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.4	V
Input RF level on pins 2G4RF_IOP and 2G4RF_ION	$P_{RFMAX2G4}$		—	—	10	dBm
Voltage differential between RF pins (2G4RF_IOP - 2G4RF_ION)	$V_{MAXDIFF2G4}$		-50	—	50	mV
Absolute voltage on RF pins 2G4RF_IOP and 2G4RF_ION	V_{MAX2G4}		-0.3	—	3.3	V
Absolute voltage on Sub-GHz RF pins	$V_{MAXSUBG}$	Pins SUBGRF_OP and SUBGRF_ON	-0.3	—	3.3	V
		Pins SUBGRF_IP and SUBGRF_IN,	-0.3	—	0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA
Junction temperature	T_J	-G grade devices	-40	—	105	°C
		-I grade devices	-40	—	125	°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

2. Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.

3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD, RFVDD, PAVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD
- RFVDD ≤ AVDD
- PAVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range[6]	T_A	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage[2]	V_{AVDD}		1.8	3.3	3.8	V
VREGVDD operating supply voltage[2][1]	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	$I_{VREGVDD}$	DCDC in bypass, T ≤ 85 °C	—	—	200	mA
		DCDC in bypass, T > 85 °C	—	—	100	mA
RFVDD operating supply voltage	V_{RFVDD}		1.62	—	$V_{VREGVDD}$	V
DVDD operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
PAVDD operating supply voltage	V_{PAVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage	V_{IOVDD}	All IOVDD pins[5]	1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor[3][4]	$C_{DECOUPLE}$		0.75	1.0	2.75	µF
Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD)[2]	dV_{DD}		—	—	0.1	V
HFCORECLK frequency	f_{CORE}	VSCALE2, MODE = WS1	—	—	40	MHz
		VSCALE0, MODE = WS0	—	—	20	MHz
HFCLK frequency	f_{HFCLK}	VSCALE2	—	—	40	MHz
		VSCALE0	—	—	20	MHz

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.
6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - (THETA$_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and THETA$_{JA}$.