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Cortina Systems® LXT973 10/100 Mbps Dual-Port Fast Ethernet PHY Transceiver

Datasheet

The Cortina Systems® LXT973 10/100 Mbps Dual-Port Fast Ethernet PHY Transceiver (LXT973 Transceiver) is an IEEE 802.3 compliant, dual-port, Fast Ethernet PHY transceiver that directly supports both 100BASE-TX and 10BASE-T applications. Each port provides a Media Independent Interface (MII) for easy attachment to 10 Mbps and 100 Mbps Media Access Controllers (MACs). The LXT973 Transceiver also provides a Low-Voltage Positive Emitter Coupled Logic (LVPECL) interface per port for use with 100BASE-FX fiber networks. The LXT973 Transceiver incorporates the auto MDI/MDIX feature, allowing it to automatically switch twisted-pair inputs and outputs.

The LXT973 Transceiver is an ideal building block for systems that require two Ethernet ports, such as Internet Protocol (IP) Telephones, Twisted-Pair (TX)-to-Fiber (FX) converter modules, and for telecom applications, such as Telecom Central Office (TCO) and Customer Premise Equipment (CPE) devices.

The LXT973 Transceiver supports full-duplex operation at both 10 Mbps and 100 Mbps. Its operating modes can be set using auto-negotiation, parallel detection, or manual control.

Applications

- Enterprise switches
- IP telephony switches
- Storage Area Networks
- Multi-port Network Interface Cards (NICs)

Product Features

- Dual-port Fast Ethernet PHY
- 2.5 Voperation
- 3.3 Voperation I/O compatibility
- Low power consumption; 250 mW per port typical
- Full dual-port MII interface with extended registers
- Auto MDI/MDIX switch over capability
- Signal Quality Error (SQE) enable/disable
- 100BASE-FX fiber-optic capability on both ports
- Supports both auto-negotiation systems and legacy systems without auto-negotiation capability
- Support for Next Page
- 20 MHz Register Access
- Configurable via MDIO port or external control pins
- Integrated termination resistors
- 100-pin Plastic Quad Flat Package (PQFP)
  - Commercial (0 °C to 70 °C ambient)
    SLXT973QC Transceiver
    EGLXT973QC Transceiver (RoHS Compliant)
  - (-40 °C to +85 °C ambient) (Extended)
    SLXT973QE Transceiver
    EGLXT973QE Transceiver (RoHS Compliant

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Revision History

Revision 7.0
Revision Date: 23 August 2011

- Changed the following signal names throughout the datasheet:

Changed From	Changed To
DPAP/N_0	DIFAP/N_0
DPBP/N_0	DIFBP/N_0
DPBP/N_1	DIFAP/N_1
DPAP/N_1	DIFBP/N_1

- The pair type on pins 67 and 68 were changed to “A” in Table 4.
- The pair type on pins 71 and 72 were changed to “B” in Table 4.

Revision 6.0
Revision Date: 13 July 2007

Updated the product top marking diagrams

Revision 5.0
Revision Date: 06 July 2007

First release of this document from Cortina Systems, Inc.

Revision#: 004
Revision Date: 29 November 2005

Modified Figure 2, *Pin Assignments*, on page 14.

Added Section 16.1, *Top Label Marking*, on page 92.

Modified Table 52, *Product Ordering Information*, on page 95.

Modified Figure 47, *Ordering Information – Sample*, on page 96.

Revision Number: 003
Revision Date: 20 January 2004

First paragraph:
Modified first sentence
Modified third sentence - Changed "pseudo-ECL" to "Low Voltage PECL
Removed bullet under Product Features: Integrated termination resistors.

Modified descriptions for pins 35, 36, 93, and 94 in Table 2 “LXT973 Port 0 Signal Descriptions”.

Changed the last word for SD0 and SD1 under Description from "Low" to “GND” in Table 4 “LXT973 Network Interface Signal Descriptions”.

Modified descriptions for pins 7 and 8 in Table 7 “LXT973 Per Port LED and Configuration Signal Descriptions”.

Changed PECL to LVPECL in second to last sentence in the first paragraph under Section 3.1, “Introduction”.

Replaced text under Section 3.2.1.3, “Fiber Interface”.

Modified text in second paragraph under Section 3.5.3, “Power-Down Mode”.

Modified bullets under Section 3.5.3.1, “Hardware Power-Down”.

Changed Register 11 to Register bit 0.11 under Section 3.5.3.2, “Software Power-Down”.

Changed PECL to LVPECL in third paragraph, first sentence under Section 3.8.1, “100BASE-X Network Operations”.

Modified Figure 10 “Protocol Sublayers” (changed "PECL Interface" to "LVPECL Interface".

Replaced text under Section 3.8.5, “Fiber PMD Sublayer”.

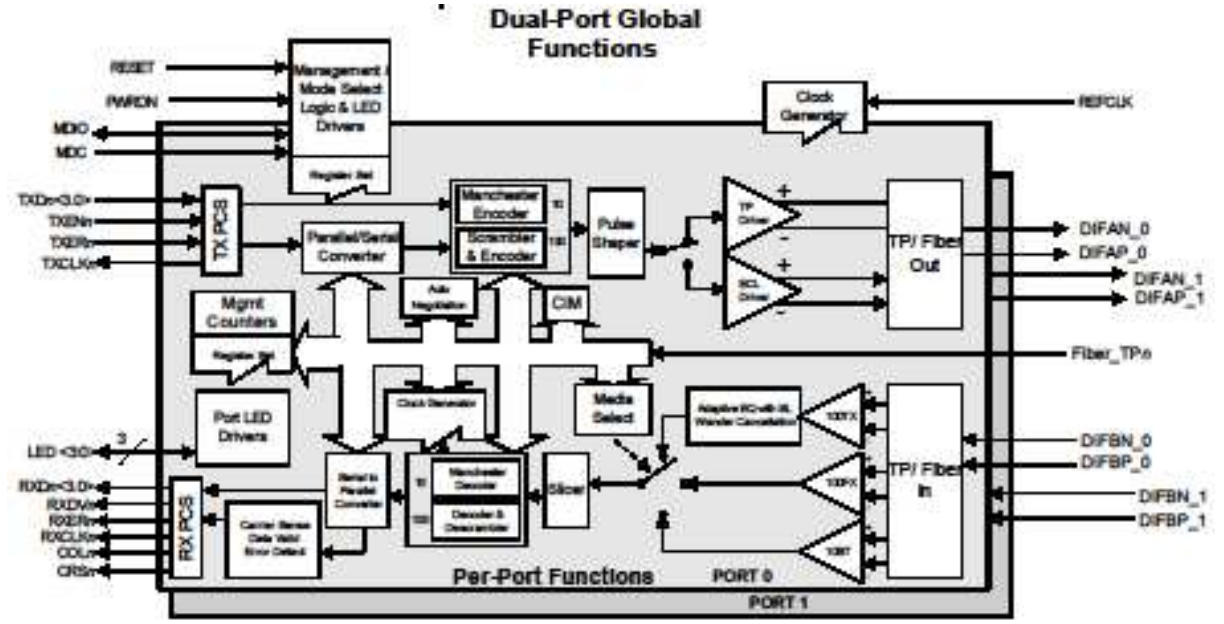
Revision Number: 003 Revision Date: 20 January 2004
Modified first sentence under Section 4.1.4, “MII Terminations”.
Replaced text under Section 4.1.5, “The Fiber Interface”.
Modified text under Section 4.1.7, “Magnetics Information”.
Replaced Figure 14 “Recommended LXT973-to-3.3 VFiber Transceiver Interface Circuitry”.
Added Figure 15 “Recommended LXT973-to-5 VFiber Transceiver Interface Circuitry”.
Added Figure 16 “ON Semiconductor* Triple PECL-to-LVPECL Logic Translator”.
Changed PECL to LVPECL in first paragraph, second sentence under Section 9.0, “Fiber Interface”.
Modified table note 2 in Table 29 “Port Configuration Register (Address 16)” (changed ”hardware pins” to “FIBER_TPn”.
Modified table note 2 in Table 41 “Digital Input/Output Characteristics2” – (changed “applies to all pins except MII...” to “applies to all pins except SD, MII...”.
Added Table 42 “Digital Input/Output Characteristics - SD Pins”.
In Table 46 “100BASE-TX Transceiver Characteristics”: Changed "Peak differential output voltage (single ended)" to "Peak-to-peak differential output voltage". Changed "VOP" to "$V_{diffp-p}$", and removed footnote #2 (and all references).
Modified Table 63 “Product Ordering Information”.

Revision Number: 002 Revision Date: June 2002
Figure 1 “LXT973 Block Diagram”: Added note to diagram.
Under Section 3.8.4, “PMA Sublayer”: Removed Table 10: 4B/5B Coding.
Section 3.10.1, “Monitoring Auto-Negotiation”: Removed paragraphs 3 and 4, and Figure 11.
Under Section 8.1, “Displaying Symbol Errors”: Removed Table 16: 4B/5B Coding.
Section 12.0, “Register Definitions” Removed “multiple 11-bit registers, with” from first sentence.
Table 20 “PHY Identification Register 2 (Address 3)”: Changed default for Register bits 3.9:4 from “001110” to “100001”.
Table 29 “Absolute Maximum Ratings” Modified Power Supply: added VccA, Vcc, VCCPECL, VCCIO information. Added three table notes.
Table 31 “Digital Input/Output Characteristics2”Modified table note 2.
Table 32 “Digital Input/Output Characteristics - MII Pins” Removed “Driver Output Impedance.”
Table 34 “LED Pin Characteristics” Added MAX value to Output High Current.
Table 35 “100BASE-TX Transceiver Characteristics” Added Typ values.
Table 36 “10BASE-T Transceiver Characteristics” Added/replaced Typ values. Removed “Receiver Input Impedance.”
Table 37 “100BASE-FX Transceiver Characteristics” Added Typ values
Table 38 “10BASE-T Link Integrity Timing Characteristics” Added Typ value for Link Pulse Width
Added Table 39 “Twisted-Pair Pins”.
Modified Table 40 on page 77 through Table 49 on page 85.

Revision Number: 002 Revision Date: June 2002
Added Figure 39 “Power-Up Timing” and Table 50 “Power-Up Timing Parameters”.
Added Figure 40 “RESET Pulse Width and Recovery Timing” and Table 51 “RESET Pulse Width and Recovery Timing Parameters”
Section A, “Product Ordering Information”: Added product ordering information table and diagram.

Revision Number: 001 Revision Date: May 2001
Initial Release (Preliminary datasheet)

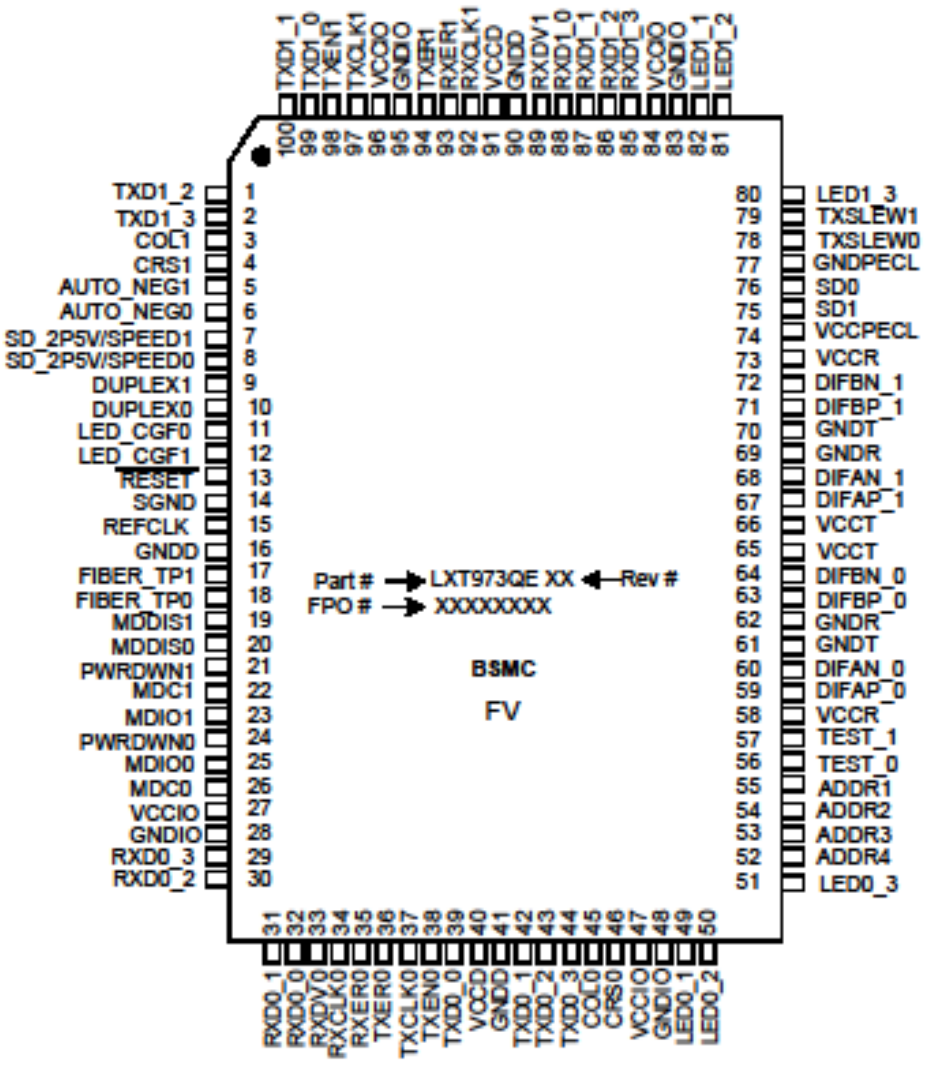
Figure 1 Block diagram



Note: See Table 4, *Network Interface Signal Descriptions*, on page 20 and Table 5, *Global Control & Configuration Signal Descriptions*, on page 21 for complete network interface signal configurations

1.0 Pin Assignments and Signal Descriptions

Figure 2 Pin Assignments



Package Topside Markings

Marking	Definition
Part #	LXT973 Transceiver is the unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” (Refer to Specification Update for additional stepping information.)
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

Table 1 PQFP Pin List (Sheet 1 of 3)

Pin	Signal Names	Type[1]	Reference for Full Description
1	TXD1_2	I	Table 3 on page 19
2	TXD1_3	I	Table 3 on page 19
3	COL1	O, TS	Table 3 on page 19
4	CRS1	O, TS	Table 3 on page 19
5	AUTO_NEG1	I	Table 7 on page 22
6	AUTO_NEG0	I	Table 7 on page 22
7	SD_2P5V/SPEED1	I	Table 7 on page 22
8	SD_2P5V/SPEED0	I	Table 7 on page 22
9	DUPLEX1	I	Table 7 on page 22
10	DUPLEX0	I	Table 7 on page 22
11	LED_CGF0	I	Table 5 on page 21
12	LED_CGF1	I	Table 5 on page 21
13	RESET	I	Table 5 on page 21
14	SGND	–	Table 6 on page 22
15	REFCLK	I	Table 5 on page 21
16	GNDD	–	Table 6 on page 22
17	FIBER_TP1	I	Table 7 on page 22
18	FIBER_TP0	I	Table 7 on page 22
19	MDDIS1	I	Table 3 on page 19
20	MDDIS0	I	Table 2 on page 18
21	PWRDWN1	I	Table 7 on page 22
22	MDC1	I	Table 3 on page 19
23	MDIO1	I/O	Table 3 on page 19
24	PWRDWN0	I	Table 7 on page 22
25	MDIO0	I/O	Table 2 on page 18
26	MDC0	I	Table 2 on page 18
27	VCCIO	–	Table 6 on page 22
28	GNDIO	–	Table 6 on page 22
29	RXD0_3	O, TS	Table 2 on page 18
30	RXD0_2	O, TS	Table 2 on page 18
31	RXD0_1	O, TS	Table 2 on page 18
32	RXD0_0	O, TS	Table 2 on page 18
33	RXDV0	O, TS	Table 2 on page 18

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-down.

Table 1 PQFP Pin List (Sheet 2 of 3)

Pin	Signal Names	Type[1]	Reference for Full Description
34	RXCLK0	O, TS	Table 2 on page 18
35	RXER0	O, TS	Table 2 on page 18
36	TXER0	I	Table 2 on page 18
37	TXCLK0	O, TS	Table 2 on page 18
38	TXEN0	I	Table 2 on page 18
39	TXD0_0	I	Table 2 on page 18
40	VCCD	–	Table 6 on page 22
41	GNDD	–	Table 6 on page 22
42	TXD0_1	I	Table 2 on page 18
43	TXD0_2	I	Table 2 on page 18
44	TXD0_3	I	Table 2 on page 18
45	COL0	O, TS	Table 2 on page 18
46	CRS0	O, TS	Table 2 on page 18
47	VCCIO	–	Table 6 on page 22
48	GNDIO	–	Table 6 on page 22
49	LED0_1	O, OD	Table 7 on page 22
50	LED0_2	O, OD	Table 7 on page 22
51	LED0_3	O, OD	Table 7 on page 22
52	ADDR4	I	Table 5 on page 21
53	ADDR3	I	Table 5 on page 21
54	ADDR2	I	Table 5 on page 21
55	ADDR1	I	Table 5 on page 21
56	TEST_0	I	Table 5 on page 21
57	TEST_1	I	Table 5 on page 21
58	VCCR	–	Table 6 on page 22
59	DIFAP_0	AI/AO, SL	Table 4 on page 20
60	DIFAN_0	AI/AO, SL	Table 4 on page 20
61	GNDT	–	Table 6 on page 22
62	GNDR	–	Table 6 on page 22
63	DIFBP_0	AI/AO, SL	Table 4 on page 20
64	DIFBN_0	AI/AO, SL	Table 4 on page 20
65	VCCT	–	Table 6 on page 22
66	VCCT	–	Table 6 on page 22
67	DIFAP_1	AI/AO, SL	Table 4 on page 20
68	DIFAN_1	AI/AO, SL	Table 4 on page 20

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-down.

Table 1 PQFP Pin List (Sheet 3 of 3)

Pin	Signal Names	Type[1]	Reference for Full Description
69	GNDR	–	Table 6 on page 22
70	GNDT	–	Table 6 on page 22
71	DIFBP_1	AI/AO, SL	Table 4 on page 20
72	DIFBN_1	AI/AO, SL	Table 4 on page 20
73	VCCR	–	Table 6 on page 22
74	VCCPECL	–	Table 6 on page 22
75	SD1	I	Table 4 on page 20
76	SD0	I	Table 4 on page 20
77	GNDPECL	–	Table 6 on page 22
78	TxSLEW0	I	Table 5 on page 21
79	TxSLEW1	I	Table 5 on page 21
80	LED1_3	O. OD	Table 7 on page 22
81	LED1_2	O, OD	Table 7 on page 22
82	LED1_1	O, OD	Table 7 on page 22
83	GNDIO	–	Table 6 on page 22
84	VCCIO	–	Table 6 on page 22
85	RXD1_3	O, TS	Table 3 on page 19
86	RXD1_2	O, TS	Table 3 on page 19
87	RXD1_1	O, TS	Table 3 on page 19
88	RXD1_0	O, TS	Table 3 on page 19
89	RXDV1	O, TS	Table 3 on page 19
90	GNDD	–	Table 6 on page 22
91	VCCD	–	Table 3 on page 19
92	RXCLK1	O, TS	Table 3 on page 19
93	RXER1	O, TS	Table 3 on page 19
94	TXER1	I	Table 6 on page 22
95	GNDIO	–	Table 6 on page 22
96	VCCIO	–	Table 3 on page 19
97	TXCLK1	O, TS	Table 3 on page 19
98	TXEN1	I	Table 3 on page 19
99	TXD1_0	I	Table 3 on page 19
100	TXD1_1	I	Table 3 on page 19

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-down.

2.0 Signal Descriptions

Table 2 Port 0 Signal Descriptions (Sheet 1 of 2)

Pin #	Signal Names	Type[1]	Signal Description
44 43 42 39	TXD0_3 TXD0_2 TXD0_1 TXD0_0	I	**Transmit Data**. TXD0_*n* is a bundle of parallel data signals driven by the MAC controller, which TXD0<3:0> transition synchronously with respect to the TXCLK0. TXD0<0> is the least significant bit. TXD0<3:0> are monitored in normal mode only.
38	TXEN0	I	**Transmit Enable.** The MAC asserts TXEN0 when it drives data on TXD0*n*. This signal must be synchronized to TXCLK0.
36	TXER0	I	**Transmit Error.** TXER0 is a 100 Mbps only signal. The MAC asserts this input when an error has occurred in the transmit data stream. When operating at 100 Mbps, the LXT973 Transceiver responds by sending "H symbols" on the line.
37	TXCLK0	O, TS	**Transmit Clock.** TXCLK0 is sourced by the LXT973 Transceiver in both 10 Mbps and 100 Mbps modes. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.
29 30 31 32	RXD0_3 RXD0_2 RXD0_1 RXD0_0	O, TS	**Receive Data.**The LXT973 Transceiver drives received data on these outputs, synchronous to RXCLK0.
33	RXDV0	O, TS	**Receive Data Valid.** The LXT973 Transceiver asserts this signal when it drives valid data on RXD0*n*. This output is synchronous to RXCLK0.
35	RXER0	O, TS	**Receive Error.** The LXT973 Transceiver asserts this output when it receives invalid symbols from the network. RXER0 is synchronous to RXCLK0.
34	RXCLK0	O, TS	**Receive Clock.** RXCLK0 is sourced by the LXT973 Transceiver in both 10 Mbps and 100 Mbps modes. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.
45	COL0	O, TS	**Collision Detected.** The LXT973 Transceiver asserts this output when a collision is detected. This output remains High for the duration of the collision. COL0 is asynchronous and is inactive during full-duplex operation.
46	CRS0	O, TS	**Carrier Sense.** During half-duplex operation, the LXT973 Transceiver asserts this output when either the transmit or receive medium is non-idle. During full-duplex operation, CRS0 is asserted only when receive medium is non-idle.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-down.

Table 2 Port 0 Signal Descriptions (Sheet 2 of 2)

Pin #	Signal Names	Type[1]	Signal Description
20	MDDIS0	I	**Management Disable**. When MDDIS0 is tied High, the MDIO port is completely disabled and the Hardware Control Interface pins set their respective bits at power-up and reset. When MDDIS0 is pulled Low at power-up or reset via the internal pull-down resistor or by tying it to ground, the Hardware Control Interface Pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.
26	MDC0	I	**Management Data Clock.** Clock for MDIO0 serial channel. Maximum frequency is 20 MHz.
25	MDIO0	I/O	**Management Data Input/Output.** Bi-directional serial data channel for PHY/STA communication.
1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-down.			

Table 3 Port 1 Signal Descriptions (Sheet 1 of 2)

Pin #	Signal Names	Type[1]	Signal Description
2 1 100 99	TXD1_3 TXD1_2 TXD1_1 TXD1_0	I	**Transmit Data.** TXD1_n is a bundle of parallel data signals driven by the MAC controller. TXD1<3:0> transition synchronously with respect to the TXCLK1. TXD1<0> is the least significant bit. In normal mode, only TXD1<3:0> are monitored.
98	TXEN1	I	**Transmit Enable.** The MAC asserts TXEN1 when it drives data on TXD0*n*. This signal must be synchronized to TXCLK1.
94	TXER1	I	**Transmit Error.** (TXER1 is a 100 Mbps only signal.**)** The MAC asserts this input when an error has occurred in the transmit data stream. When operating at 100 Mbps, the LXT973 Transceiver responds by sending "H Symbols" on the line.
97	TXCLK1	O, TS	**Transmit Clock.** TXCLK1 is sourced by the LXT973 Transceiver in both 10 Mbps and 100 Mbps modes. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.
85 86 87 88	RXD1_3 RXD1_2 RXD1_1 RXD1_0	O, TS	**Receive Data.**The LXT973 Transceiver drives received data on these outputs, synchronous to RXCLK1.
89	RXDV1	O, TS	**Receive Data Valid.** The LXT973 Transceiver asserts this signal when it drives valid data on RXD0*n*. This output is synchronous to RXCLK1.
93	RXER1	O, TS	**Receive Error.** The LXT973 Transceiver asserts this output when it receives invalid symbols from the network. RXER1 is synchronous to RXCLK1.
92	RXCLK1	O, TS	**Receive Clock.** RXCLK1 is sourced by the LXT973 Transceiver in both 10 Mbps and 100 Mbps modes. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.
1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down			

Table 3 Port 1 Signal Descriptions (Sheet 2 of 2)

Pin #	Signal Names	Type[1]	Signal Description
3	COL1	O, TS	**Collision Detected.** The LXT973 Transceiver asserts this output when a collision is detected. This output remains High for the duration of the collision. COL is asynchronous and is inactive during full-duplex operation.
4	CRS1	O, TS	**Carrier Sense.** During half-duplex operation, the LXT973 Transceiver asserts this output when either the transmit or receive medium is non-idle. During full-duplex operation, CRS1 is asserted only when receive medium is non-idle.
19	MDDIS1	I	**Management Disable**. When MDDIS is tied High, the MDIO port is completely disabled and the Hardware Control Interface pins set their respective bits at power-up and reset. When MDDIS is pulled Low at power-up or reset via the internal pull-down resistor or by tieing it to ground, the Hardware Control Interface Pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.
22	MDC1	I	**Management Data Clock.** Clock for MDIO1 serial channel. Maximum frequency is 20 MHz. (**Note:** 20 MHz value to be verified prior to final production release of product.)
23	MDIO1	I/O	**Management Data Input/Output.** Bidirectional serial data channel for PHY/STA communication.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 4 Network Interface Signal Descriptions (Sheet 1 of 2)

Pin #	Signal Names	TP Op	Fiber Op	Port	Pair Type	Type[1]	Signal Description
59 60	DIFAP_0 DIFAN_0	TX+ TX-	RX+ RX-	0 0	A A	AI/AO, SL	**Twisted-Pair/Fiber Pair A, Positive & Negative - Port 0.** Differential pair produces or receives IEEE 802.3-compliant pulses for either 100BASE-TX or 10BASE-T. Also acts as receiver in Fiber mode.
63 64	DIFBP_0 DIFBN_0	RX+ RX-	TX+ TX-	0 0	B B	AI/AO, SL	**Twisted-Pair/Fiber Pair B, Positive & Negative - Port 0.** Differential pair produces or receives IEEE 802.3-compliant pulses for either 100BASE-TX or 10BASE-T. Also acts as transmitter in Fiber mode.
76	SD0	–	–	–	–	I	**Signal Detect.** This signal is used for signal quality indication in Fiber mode. In twisted-pair mode, this pin should be tied to GND.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 4 Network Interface Signal Descriptions (Sheet 2 of 2)

Pin #	Signal Names	TP Op	Fiber Op	Port	Pair Type	Type[1]	Signal Description
67 68	DIFAP_1 DIFAN_1	TX+ TX-	TX- TX+	1 1	A A	AI/AO, SL	**Twisted-Pair/Fiber Pair B, Positive & Negative - Port 1.** Differential pair produces or receives IEEE 802.3-compliant pulses for either 100BASE-TX or 10BASE-T. Also acts as transmitter in Fiber mode.
71 72	DIFBP_1 DIFBN_1	RX+ RX-	RX- RX+	1 1	B B	AI/AO, SL	**Twisted-Pair/Fiber Pair A, Positive & Negative - Port 1.** Differential pair produces or receives IEEE 802.3-compliant pulses for either 100BASE-TX or 10BASE-T. Also acts as receiver in Fiber mode.
75	SD1	–	–	–	–	I	**Signal Detect.** This signal is used for signal quality indication in Fiber mode. In twisted-pair mode, this pin should be tied to GND.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 5 Global Control & Configuration Signal Descriptions

Pin #	Signal Names	Type[1]	Signal Description
78 79	TxSLEW0 TxSLEW1	I	**Tx Output Slew Controls 0 & 1.** These pins select the TX output slew rate (rise and fall time) for both cores in the LXT973 Transceiver. The various options are defined in Register bits 27.11:10. The TxSLEW pins set the power-on value of these register bits.
13	RESET	I	**Reset.** This active Low input is OR'd with Control Register bit 0.15.
52 53 54 55	ADDR4 ADDR3 ADDR2 ADDR1	I	**Address <4:1>.** Sets device Port 0 PHY address. Note that ADDR0 is set internally so that Port 1 is always "1" address higher than Port 0.
56 57	TEST_0 TEST_1	I	**Test Pins.** Tie Low for normal operation.
15	REFCLK	I	**Master Clock Input.** A 25 MHz, 50 ppm clock is input here to act as the master clock. Full clock requirements are detailed in the Clock Requirements section of the Functional Description. See Section 3.4.2, *Clock Requirements*, on page 30.
11 12	LED_CFG0 LED_CFG1	I	**LED Configuration 0 & 1.** These pins are used to select one of four LED modes. The decode or each mode is shown below:

LED_CFG0	LED_CFG1	LEDn_1	LEDn_2	LEDn_3
0	0	Speed	Link	Duplex
1	0	Speed	Link/Activity	Duplex/Collision
0	1	Link	Receive	Transmit
1	1	Speed	Link/MII Isolate	Duplex/Collision

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 6 Power Supply Signal Descriptions

Pin #	Signal Names	Type[1]	Signal Description
40, 91	VCCD	–	**Digital Power Supply - Core. +**2.5 V supply for core digital circuits.
27, 47, 84, 96	VCCIO	–	**Digital Power Supply - I/O Ring.** +2.5/3.3 V supply for digital I/O circuits. The digital input circuits running off this rail, having a TTL-level threshold and over-voltage protection, may be interfaced with 3.3/5.0V when the I/O supply is 3.3 V, and 2.5/3.3/5.0V when the I/O supply is 2.5 V.
74	VCCPECL	–	**Digital Power Supply - PECL Signal Detect Inputs.** +2.5/3.3 V supply for PECL Signal Detect input circuits. If Fiber Mode is not used, tie these pins to GNDPECL to save power.
58, 73	VCCR	–	**Analog Power Supply - Receive.** +2.5 V supply for all analog receive circuits.
65, 66	VCCT	–	**Analog Power Supply - Transmit.** +2.5 V supply for all analog transmit circuits.
16, 41, 90,	GNDD	–	**Digital Ground**. Ground return for core digital supplies (VCCD). All ground pins can be tied together using a single ground plane.
28, 48, 83, 95	GNDIO	–	**Digital GND - I/O Ring.** Ground return for digital I/O circuits (VCCIO).
77	GNDPECL	–	**Digital GND - PECL Signal Detect Inputs.** Ground return for PECL Signal Detect input circuits.
69, 62	GNDR	–	**Analog Ground - Receive**. Ground return for receive analog supply. All ground pins can be tied together using a single ground plane.
61, 70	GNDT	–	**Analog Ground - Transmit**. Ground return for transmit analog supply. All ground pins can be tied together using a single ground plane.
14	SGND	–	**Substrate Ground**. Ground for chip substrate. All ground pins can be tied together using a single ground plane.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 7 Per Port LED and Configuration Signal Descriptions (Sheet 1 of 2)

Pin #	Signal Names	Type[1]	Signal Description
49 50 51	LED0_1 LED0_2 LED0_3	OD, TS, SL, IP	**Port 0 LED Drivers 1-3.** These pins drive LED indicators for Port 0. Each LED can display one of several available status conditions as selected by the LED Configuration Register.
82 81 80	LED1_1 LED1_2 LED1_3	OD, TS, SL, IP	**Port 1 LED Drivers 1-3.** These pins drive LED indicators for Port 1. Each LED can display one of several available status conditions as selected by the LED Configuration Register.
6 5	AUTO_NEG0 AUTO_NEG1	I I	**Auto Negotiation Enable.** When this pin is High, auto-negotiation is enabled on the relevant port.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

Table 7 Per Port LED and Configuration Signal Descriptions (Sheet 2 of 2)

Pin #	Signal Names	Type[1]	Signal Description
8	SD_2P5V/SPEED0	I	**SD_2P5V.** In fiber mode, this pin selects between 2.5 V or 3.3 V fiber transceiver thresholds for both ports. High = 2.5 V Low = 3.3 V **Speed.** In copper mode, this pin sets the default speed of Port 0 in Hardware mode. High = 100 Mbps Low = 10 Mbps
7	SD_2P5V/SPEED1	I	**SD_2P5V.** In fiber mode, the speed of both ports defaults to 100BASE-FX. Pin 7 should be tied to ground. Speed. In copper mode, this pin sets the default speed of Port 1 in Hardware mode. High = 100 Mbps Low = 10 Mbps
10 9	DUPLEX0 DUPLEX1	I I	**Duplex.** Sets the duplex setting of the port in Hardware mode. High is full-duplex and Low is half-duplex.
18 17	FIBER_TP0 FIBER_TP1	I I	**Fiber/Twisted-Pair.** Sets the operating state of the port in Hardware mode. High is twisted-pair and Low is fiber.
24 21	PWRDWN0 PWRDWN1	I	**Power-Down.** When set High, this pin puts the relevant PHY into power-down mode.

1. AI = Analog Input, AO = Analog Output, I = Input, O = Output, OD = Open Drain output, ST = Schmitt Triggered input, TS = Three-State-able output, SL = Slew-rate Limited output, IP = Weak Internal Pull-up, ID = Weak Internal Pull-Down

3.0 Functional Description

3.1 Introduction

The Cortina Systems® LXT973 10/100 Mbps Dual-Port Fast Ethernet PHY Transceiver (LXT973 Transceiver) is an IEEE-compliant, dual-port, Fast Ethernet PHY transceiver that directly supports both 100BASE-TX and 10BASE-T applications. The device incorporates full Media Independent Interface (MII), enabling each individual network port to connect with 10/100 Mbps MACs. Each port directly drives either a 100BASE-TX line or a 10BASE-T line (up to 160 meters). The LXT973 Transceiver also supports 100BASE-FX operation via an LVPECL interface. The device uses a 100-pin QFP package.

3.1.1 Comprehensive Functionality

The LXT973 Transceiver performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X specification. This device also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

On power-up, the LXT973 Transceiver reads its configuration inputs to check for forced operation settings. If not configured for forced operation, each port uses auto-negotiation/parallel detection to automatically determine line operating conditions. If the link partner supports auto-negotiation, the LXT973 Transceiver auto-negotiates with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT973 Transceiver automatically detects (parallel detection) the presence of either link pulses (10 Mbps PHY) or IDLE symbols (100 Mbps PHY) and sets its operating conditions accordingly. When parallel detection is used to establish link, the resulting link is at half-duplex. The LXT973 Transceiver provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

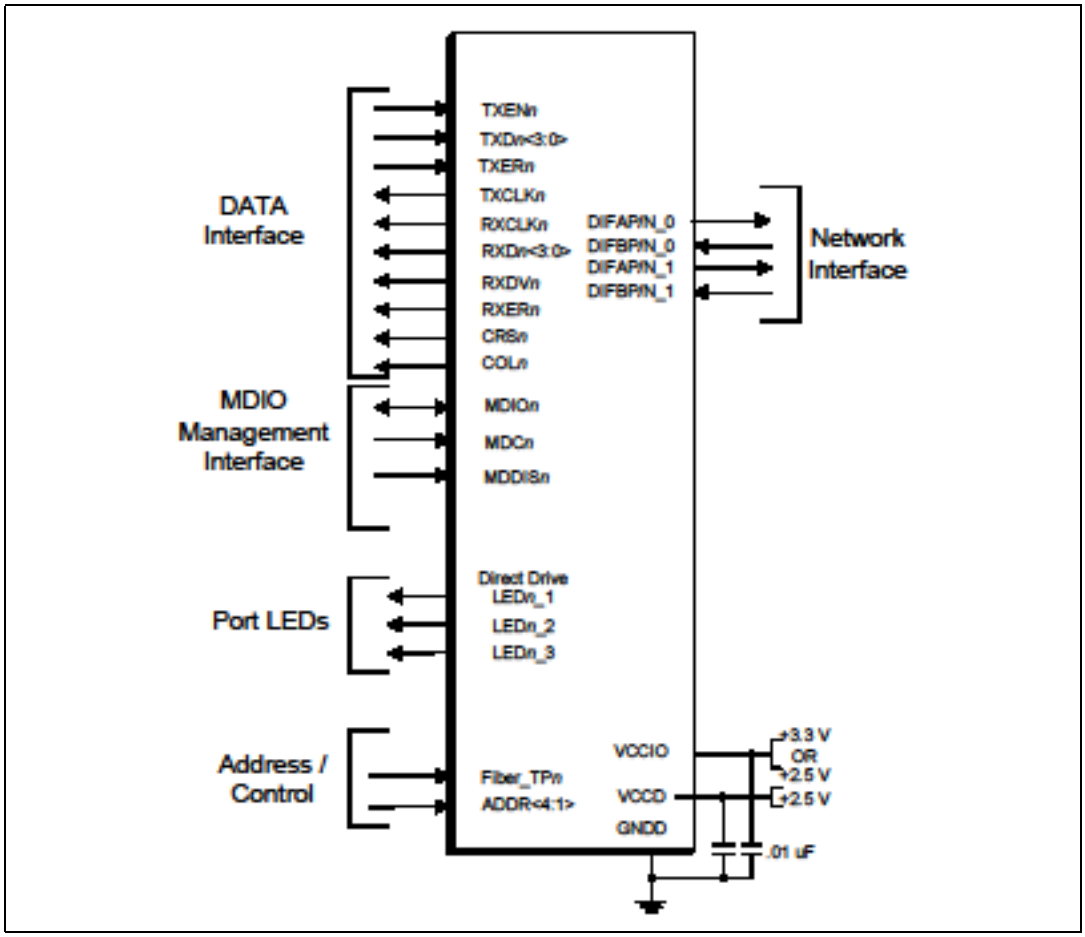
3.2 Interface Descriptions

3.2.1 10/100 Mbps Network Interface

The LXT973 Transceiver supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair, or 100 Mbps Ethernet over fiber media (100BASE-FX). Each network interface port consists of four external pins (two differential signal pairs). The pins are shared between twisted-pair and fiber.

The LXT973 Transceiver output drivers generate either 100BASE-TX, 10BASE-T, or 100BASE-FX output. When not transmitting data, the device generates IEEE 802.3-compliant link pulses or IDLE code. Input signals are decoded either as a 100BASE-TX, 100BASE-FX, or 10BASE-T input, depending on the mode selected. Auto-negotiation/parallel detection or manual control is used to determine the speed of this interface. Polarity is determined by the MDI crossover function.

Figure 3 Interfaces



3.2.1.1 Twisted-Pair Interface

The LXT973 Transceiver supports either 100BASE-TX or 10BASE-T connections over 100Ω, Category 5, Unshielded Twisted-Pair (UTP). Only a transformer, RJ-45, and bypass capacitors are required to complete this interface. The transmitter shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings allow the designer to match the output waveform to the magnetic characteristics. Both transmit and receive terminations are built into the LXT973 Transceiver. Therefore, no external components are required between the LXT973 Transceiver and the external transformer. The transmitter uses a transformer with a center tap to help reduce power consumption.

When operating at 100 Mbps, MLT3 symbols are continuously transmitted and received. When not transmitting data, the LXT973 Transceiver generates “IDLE” symbols.

During 10 Mbps operation, LXT973 Transceiver encoded data is exchanged. When no data is exchanged, the line transmits normal link pulses to maintain link.