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KCU105 Board

User Guide

UG917 (v1.7) January 12, 2017

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/12/2017	1.7	Revised Programmable User Clock Source, FMC HPC Connector J22, FMC LPC Connector J2, and Switches. Revised Figure A-1.
03/31/2016	1.6	Updated Table 1-11.
03/24/2016	1.5	Updated Figure 1-21. Changed the IOSTANDARD LVCMOS18 line in KCU105 Board Constraints File Listing on page 120. Added board thickness to Dimensions. Updated the Declaration of Conformity.
09/25/2015	1.4	Updated FMC HPC Connector J22. Revised Figure 1-23. Updated the binary format for I2C EEPROM in Table 1-19. Updated the clocks constraints file listing in Appendix D, Master Constraints File Listing.
06/27/2015	1.3	Updated connectivity information for Quad 226, Quad 227, and Quad 228 in GTH Transceivers. Updated Figure 1-21 and Figure 1-36. Updated HDMI Video Output, including updating Figure 1-22 and Table 1-18.
05/20/2015	1.2.1	Made typographical edits.
05/07/2015	1.2	Updated Table 1-17, Table 1-21, and Figure 1-22.
04/07/2015	1.1	Changed the Si5328C clock multiplier/jitter attenuator to Si5328B throughout, including updating the frequency range. Added impedance and insertion loss information to GTH SMA Clock Input, GTH TX and RX SMA Differential Pairs, PCI Express Endpoint Connectivity, SFP/SFP+ Module Connectors, FMC HPC Connector J22, and FMC LPC Connector J2. Updated Figure 1-2, Figure 1-8, Figure 1-9, Figure 1-22, Figure 1-23, Figure 1-29, Figure 1-34, Figure 1-36, Figure A-1, Figure C-1, and Figure C-2. Changed IIC to I2C throughout. Updated Table 1-4 and Table 1-25. Added Table 1-26, Maxim Power Tool GUI Regulator Settings. Updated information for J11, J47, and J49 in Table A-2. Updated callout number in KCU105 Board Zynq-7000 AP SoC XC7Z010 System Controller. Added instructions for accessing the system controller main menu in Appendix C, System Controller. Updated Clock Menu section. Updated the KCU105 Board Constraints File Listing in Appendix D. Updated the KCU105 evaluation kit master answer record number.
12/18/2014	1.0	Initial Xilinx release.

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KCU105 Evaluation Board Features

Overview

The KCU105 evaluation board for the Xilinx® Kintex® UltraScale™ FPGA provides a hardware environment for developing and evaluating designs targeting the UltraScale XCKU040-2FFVA1156E device. The KCU105 evaluation board provides features common to many evaluation systems, including a DDR4 component memory, a high definition multimedia interface (HDMI™), two small form-factor pluggable (SFP+) connectors, an eight-lane PCI Express® interface, an Ethernet PHY, general purpose I/O, and two UART interfaces. Other features can be added by using VITA-57 FPGA mezzanine cards (FMCs) attached to the low pin count (LPC) FMC and high pin count (HPC) FMC connectors.

KCU105 Evaluation Board Features

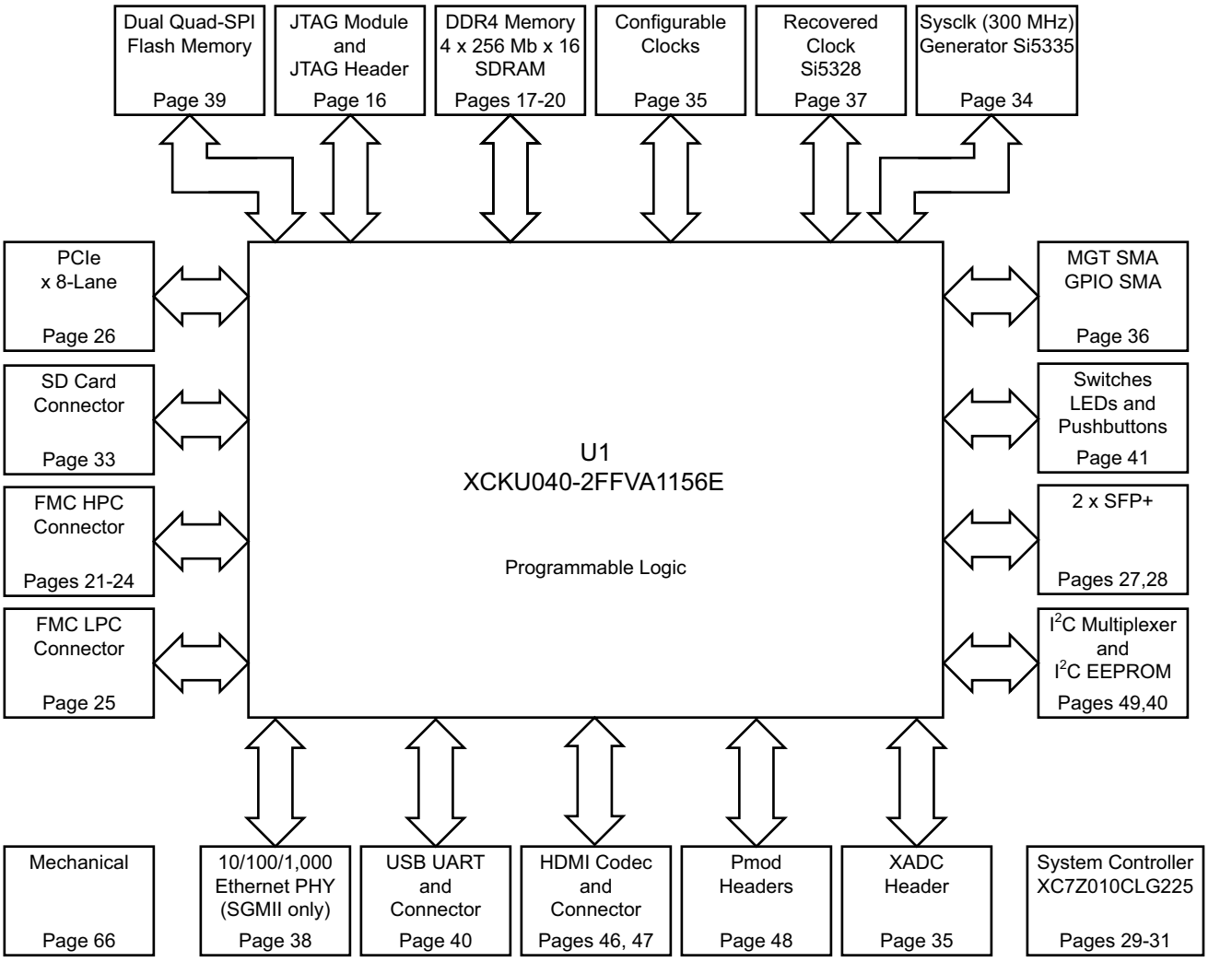
The KCU105 evaluation board features are listed here. Detailed information for each feature is provided in Feature Descriptions.

- Kintex UltraScale XCKU040-2FFVA1156E device
- Zynq® AP SoC XC7Z010 based system controller
- 2 GB DDR4 component memory (four [256 Mb x 16] devices)
- Dual 256 Mb Quad serial peripheral interface flash memory (Dual Quad SPI)
- Micro secure digital (SD) connector
- USB JTAG interface via Digilent module with micro-B USB connector
- Clock sources:
  - Si5335A quad fixed frequency clock generator (300 MHz, 125 MHz, 90 MHz, 33.333 MHz)
  - Si5328B clock multiplier and jitter attenuator (8 kHz - 808 MHz)
  - Si570 I2C programmable LVDS clock generator (10 MHz - 810 MHz)
  - Subminiature version A (SMA) connectors (differential)
- 20 GTH transceivers (five Quads)
  - FMC HPC connector (eight GTH transceivers)

  - FMC LPC connector (one GTH transceiver)
  - 8-Lane PCI Express (eight GTH transceivers)
  - Two SFP+ connectors (two GTH transceivers)
  - TX and RX pair SMA connectors (one GTH transceiver)
- PCI Express endpoint connectivity
  - Gen1 8-lane (x8)
  - Gen2 8-lane (x8)
  - Gen3 8-lane (x8)
- Two SFP+ connectors
- Ethernet PHY SGMII interface with RJ-45 connector
- Dual USB-to-UART bridge with micro-B USB connector
- HDMI codec with HDMI connector
- I2C bus
- Status LEDs
- User I/O
- Program_B pushbutton
- Pmod Headers
- VITA 57.1 FMC HPC connector J22
- VITA 57.1 FMC LPC connector J2
- Power on/off slide switch SW1
- Power management with PMBus voltage monitoring through Maxim power controllers and GUI, current monitoring via the FPGA SYSMON block
- Single 10-bit 0.2 MSPS SYSMON analog-to-digital converter
- Configuration options:
  - Dual Quad-SPI flash memory
  - USB JTAG configuration port (Digilent module)
  - Platform cable header J3 JTAG configuration port
  - System controller micro-SD card

Board Diagram

The KCU105 board diagram is shown in Figure 1-1



Note: Page numbers reference the page number of schematic 0381556

X18365-113016

Figure 1-1: **KCU105 Evaluation Board Block Diagram**

Feature Descriptions

Figure 1-2 shows the KCU105 board. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1 with a link to detailed information provided under Feature Descriptions.

IMPORTANT: *Figure 1-2 is for visual reference only and might not reflect the current revision of the board.*

CAUTION! *The KCU105 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.*

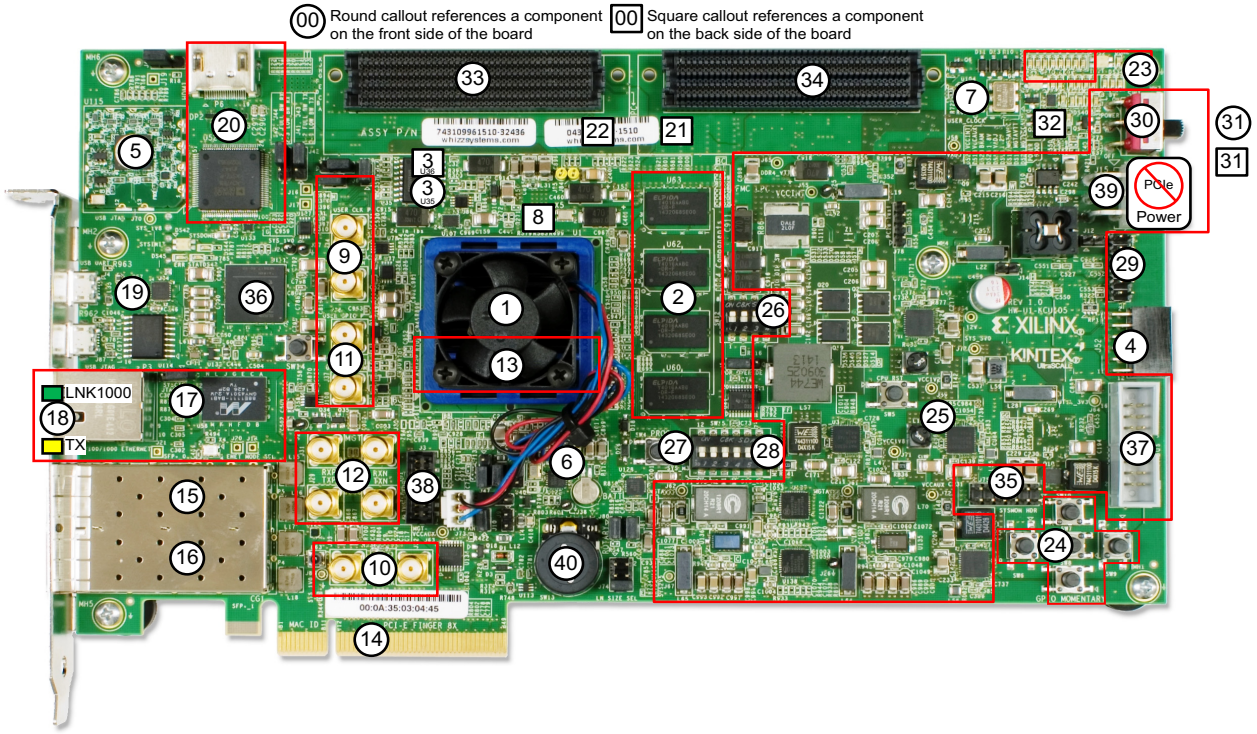


Figure 1-2: **KCU105 Evaluation Board Components**

Table 1-1: **KCU105 Board Component Descriptions**

Callout	Component Description	Notes	Schematic[1] 0381556 Page Number
1	Kintex UltraScale XCKU040-2FFVA1156E Device	XCKU040-2FFVA1156E	
	With fan-sink on top of the FPGA soldered on the board	Radian FB95+K52B+T710	
2	DDR4 Component Memory, DDR4 Memory 2GB (4x512M U60-U63)	Micron MT40A256M16HA-083E	17-20
3	Dual Quad-SPI Flash Memory, Dual Quad-SPI Flash (2x256Mb) (U35-U36)	Micron N25Q256A11ESF40F U35 on top, U36 on bottom of board	39
4	Micro-SD Card Interface, Micro SD Card Interface Connector (J83)	Molex 5025700893	33
5	USB JTAG Interface, w/Micro-B Connector	Digilent USB JTAG Module	16
6	Clock Generation, SYSCLK and other clocks, 1.8V LVDS (U122)	Si5335A-B02436-GM, 4 outputs: 300MHz, 125MHz, 90MHz, 33.33MHz	34
7	Programmable User Clock Source, I2C Prog. User Clock 3.3V LVDS (U32) with 1-to-2 LVDS buffer (U104)	Silicon Labs Si570BAB0000544DG (default 156.250MHz) with Si53340 buffer	35
8	Jitter Attenuated Clock, Jitter Attenuated Clock (U57)	Silicon Labs Si5328B-C-GM	37
9	User SMA Clock Input, User Differential SMA Clock P/N (J34/J35)	Rosenberger 32K10K-400L5	36
10	GTH SMA Clock Input, SMA_MGT_REFCLK_P/N (J33/J32)	Rosenberger 32K10K-400L5	36
11	User SMA GPIO, User SMA GPIO Connectors P/N (J36/J37)	Rosenberger 32K10K-400L5	36
12	GTH TX and RX SMA Differential Pairs, User SMA TX and RX_P/N (J31/J30, J29/J28)	Rosenberger 32K10K-400L5	36
13	GTH Transceivers	Embedded within FPGA U1	10
14	PCI Express Endpoint Connectivity, PCI Express Connector (P1)	8-lane card edge connector	26
15	SFP/SFP+ Module Connectors, SFP/SFP+ Module Connector SFP0(P5)	Molex 74441-0010	27
16	SFP/SFP+ Module Connectors, SFP/SFP+ Module Connector SFP1 (P4)	Molex 74441-0010	28
17	10/100/1000 Mb/s Tri-Speed Ethernet PHY, SGMII Mode Only (U58,P3)	Marvell M88E1111-BAB1C000 with Halo HFJ11-1G01E-L12RL RJ45	38
18	Ethernet PHY Status LEDs, LEDs are integrated into P3 bezel	Halo HFJ11-1G01E-L12RL RJ45 integrated Status LEDs (Rev B)	38

Table 1-1: **KCU105 Board Component Descriptions *(Cont'd)***

Callout	Component Description	Notes	Schematic[1] 0381556 Page Number
19	Dual USB-to-UART Bridge, Bridge device (U34) with Mini-B Connector (J4)	Silicon Labs CP2105-F01-GM bridge, Hirose ZX62D-AB-5P8 connector	40
20	HDMI Video Output, HDMI Controller (U52), HDMI Connector (P6)	Analog Devices ADV7511KSTZ-P, Molex 47151-001	46, 47
21	I2C Bus, Topology, and Switches, I2C Bus MUX (U28)	TI TCA9548APWR bottom of board	49
22	I2C Bus, Topology, and Switches, I2C Bus MUX (U80)	TI PCA9544ARGYR bottom of board	50
23	Status and User LEDs, User LEDs (DS6-DS10, DS31-DS33)	GPIO LEDs, GREEN 0603 Lumex SML-LX0603GW-TR	41
24	User Pushbuttons, User Pushbuttons, active-High (SW6-SW10)	E-Switch TL3301EF100QG in North, South, East, West, Center pattern	41
25	User Pushbuttons, User CPU RESET, active-High (SW5)	E-Switch TL3301EF100QG	41
26	GPIO DIP Switch, GPIO DIP Switch (SW12)	4-pole C&K SDA04H1SBD	41
27	Program_B Pushbutton Switch, FPGA PROG Pushbutton (SW4)	E-Switch TL3301EF100QG	41
28	FPGA Configuration DIP Switch, DIP Switch (SW15)	6-pole C&K SDA06H1SBD	32
29	User PMOD GPIO Headers, PMOD Hdrs. (J52,J53) w/Level-Shifters (U41,U42)	2x6 0.1 inch male header Sullins PBC36DAAN; TI TXS0108EPWR	48
30	Power On/Off Slide Switch SW1, Power On/Off Switch (SW1)	C&K 1201M2S3AQE2	51
31	KCU105 Board Power System, Power Management System (top and bottom)	Maxim MAX15301 and MAX15303 Digital P.O.L. Controllers	52 - 65
32	SYSMON Power System Measurement SYSMON External Circuitry	Analog Devices MUX ADG707BRUZ TI Op Amps INA333AIDGKR	44 - 45
33	FMC HPC Connector J22, FMC HPC connector (J22)	Samtec ASP_134486_01	21 - 24
34	FMC LPC Connector J2, FMC LPC connector (J2)	Samtec ASP_134603_01	25
35	SYSMON Power System Measurement, SYSMON Header (J75)	2x6 0.1inch male header, part of breakaway 2x36 Sullins PBC36DAAN	43
36	KCU105 Board Zynq-7000 AP SoC XC7Z010 System Controller, Zynq-7000 AP SoC XC7Z010CLG225 (U111)	XC7Z010CLG225	29 - 31

Table 1-1: **KCU105 Board Component Descriptions *(Cont'd)***

Callout	Component Description	Notes	Schematic[1] 0381556 Page Number
37	2x8 shrouded PMBus connector J39, see Monitoring Voltage and Current	ASSMAN AWHW16G-0202	50
38	2x7 2mm shrouded JTAG cable connector J82, see Monitoring Voltage and Current	MOLEX 87832-1420	32
39	12V power input 2x3 connector (J15), see Power On/Off Slide Switch SW1	MOLEX-39-30-1060	51
40	Rotary Switch, Active-High (SW13)	PANASONIC EVQ-WK4001	41

Notes:

1. The KCU105 board schematics are available for download. See the KCU105 Evaluation Kit website.
2. The KCU105 board jumper header locations are shown in Figure A-1.

Kintex UltraScale XCKU040-2FFVA1156E Device

[Figure 1-2, callout 1]

The KCU105 board is populated with the Kintex UltraScale XCKU040-2FFVA1156E device. For more information on Kintex UltraScale FPGAs, see *Kintex UltraScale Data Sheet: DC and AC Switching Characteristics* (DS892) [Ref 1].

FPGA Configuration

The UltraScale FPGA is configured using either the master SPI or JTAG mode as determined by the configuration DIP switch SW15.

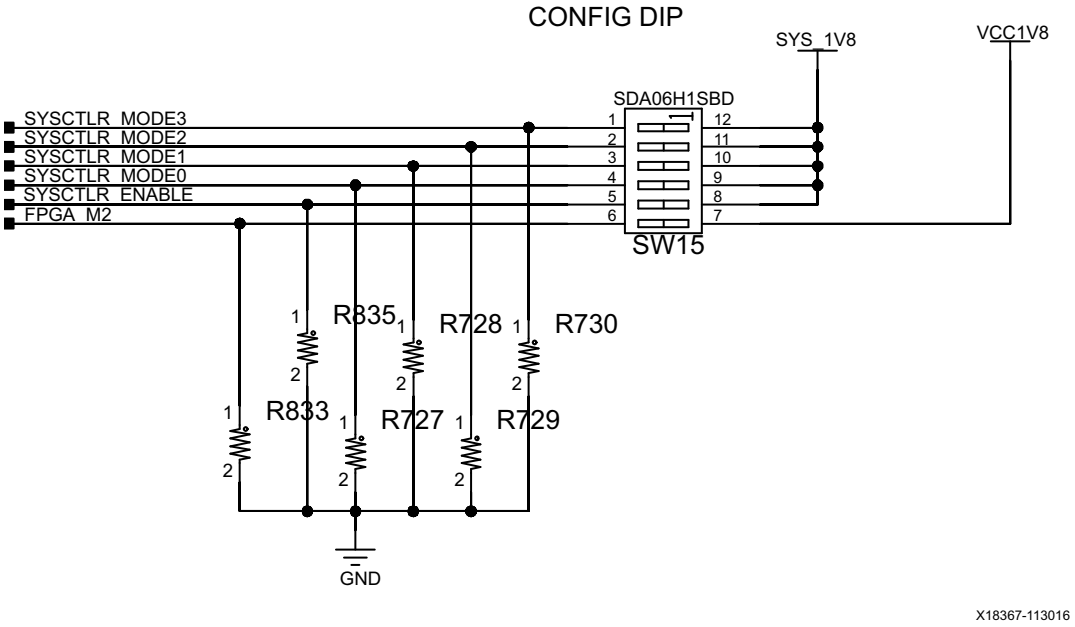


Figure 1-3: **Configuration DIP Switch**

Interfaces supporting these configuration modes are:

- Master SPI: Quad SPI flash memory (U35 and U36)
- JTAG:
  - Digilent USB-to-JTAG configuration module (U115)
  - Platform cable header (J3)
  - System controller (U111)

Each configuration interface corresponds to one or more configuration modes and bus widths, as listed in Table 1-2. The FPGA mode pins M1 and M0 are hard-wired to logic 0 and 1, respectively. FPGA mode pin M2 is wired to SW15 pin 6 position 6, which has a default setting of OPEN, enabling the M2 net to be pulled down to logic 0 (for example, the FPGA default mode setting M[2:0] = 001, selecting Quad SPI configuration mode).

Table 1-2: **Configuration Modes**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output
JTAG	101	x1	Not Applicable

Prior to KCU105 board power-up, the UltraScale FPGA U1 configuration method is selected with DIP switch SW15 switch settings:

- Master SPI Mode
  - With both SW15.6 (FPGA_M2) and SW15.5 (SYSCTLR_ENABLE) in the OFF (disable the SYSCTLR_ENABLE) position, a bitstream programmed into the dual-QSPI flash devices (U35, U36) is used to configure the UltraScale FPGA U1.
- JTAG Mode
  - With switch SW15.6 ON and SW15.5 in the OFF position, either the USB JTAG Digilent U115 or the JTAG cable header J3 can be used.

  With both switches SW15.6 and SW15.5 in the ON position, the Xilinx integrated configuration engine is used to configure the UltraScale FPGA U1 over JTAG with one of several bitstreams stored on a micro-SD card inserted in to the SD card connector J83. Selecting the bitstream to use for this JTAG configuration is accomplished by setting SW15.1 (MSB) through SW15.4 (LSB) to one of the sixteen possible binary values. The technical reference design (TRD) files are available on the KCU105 Evaluation Kit website.

Once the board is powered up or when the system controller POR pushbutton (SW14) is pressed, the system controller menu, accessed through the USB UART (J4), is available for user initiated configuration of the UltraScale FPGA. The "Configure UltraScale FPGA from micro-SD card" option (see CONFIG Menu Options) utilizes the Xilinx integrated configuration engine to prompt for one of sixteen micro-SD card resident bitstreams to configure the UltraScale FPGA (U1). When configuration is initiated through the system controller menu, the bitstream number entered at the text prompt determines the selected bitstream. DIP switch SW15 positions 1 to 4 do not determine the selected bitstream.

See Appendix C, System Controller for information on installing and using the user interface.

For complete details on configuring the FPGA, see *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2].

Encryption Key Battery Backup Circuit

The XCKU040 device U1 implements bitstream encryption key technology. The KCU105 board provides the encryption key backup battery circuit shown in Figure 1-4. The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCKU040 device U1 VBATT pin AD7. The battery supply current I_{BATT} specification is described in the *Kintex UltraScale Architecture Data Sheet: DC and AC Switching Characteristics* (DS892) [Ref 1]. The battery provides backup power to a RAM-based encryption key when the board power is off. B1 is charged from the SYS_1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 KΩ current limit resistor. The nominal charging voltage is 1.42V. The VBATT is only required for use with encrypted bitstreams as it provides backup power to a RAM-based encryption key in the absence of powering the entire FPGA. The stored key is used for decrypting an encrypted bitstream during configuration.

See *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2] for more details about Xilinx UltraScale bitstream encryption solutions.

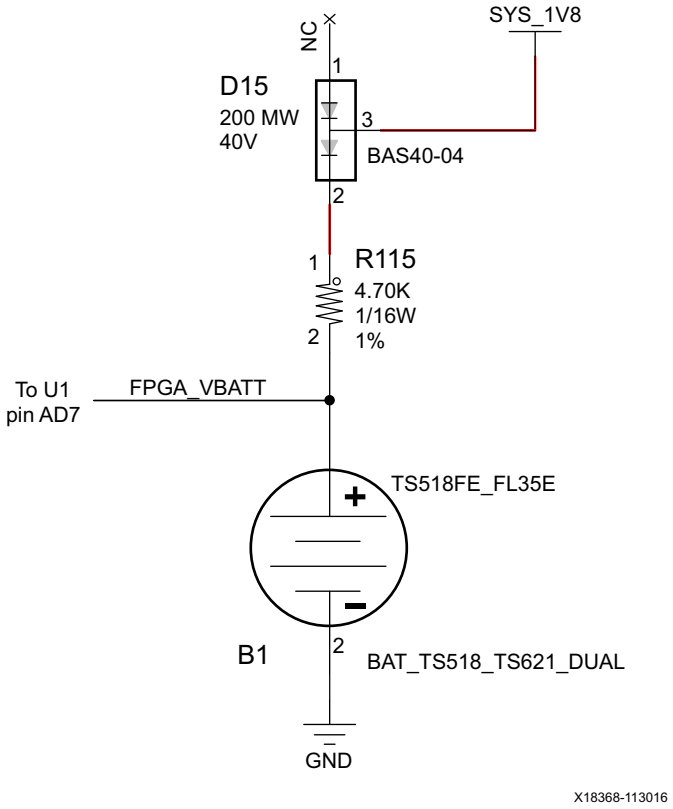


Figure 1-4: **Encryption Key Backup Circuit**

I/O Voltage Rails

There are ten I/O banks available on the KCU040 device and the KCU105 board. The voltages applied to the FPGA I/O banks (shown in Figure 1-5) used by the KCU105 board are listed in Table 1-3.

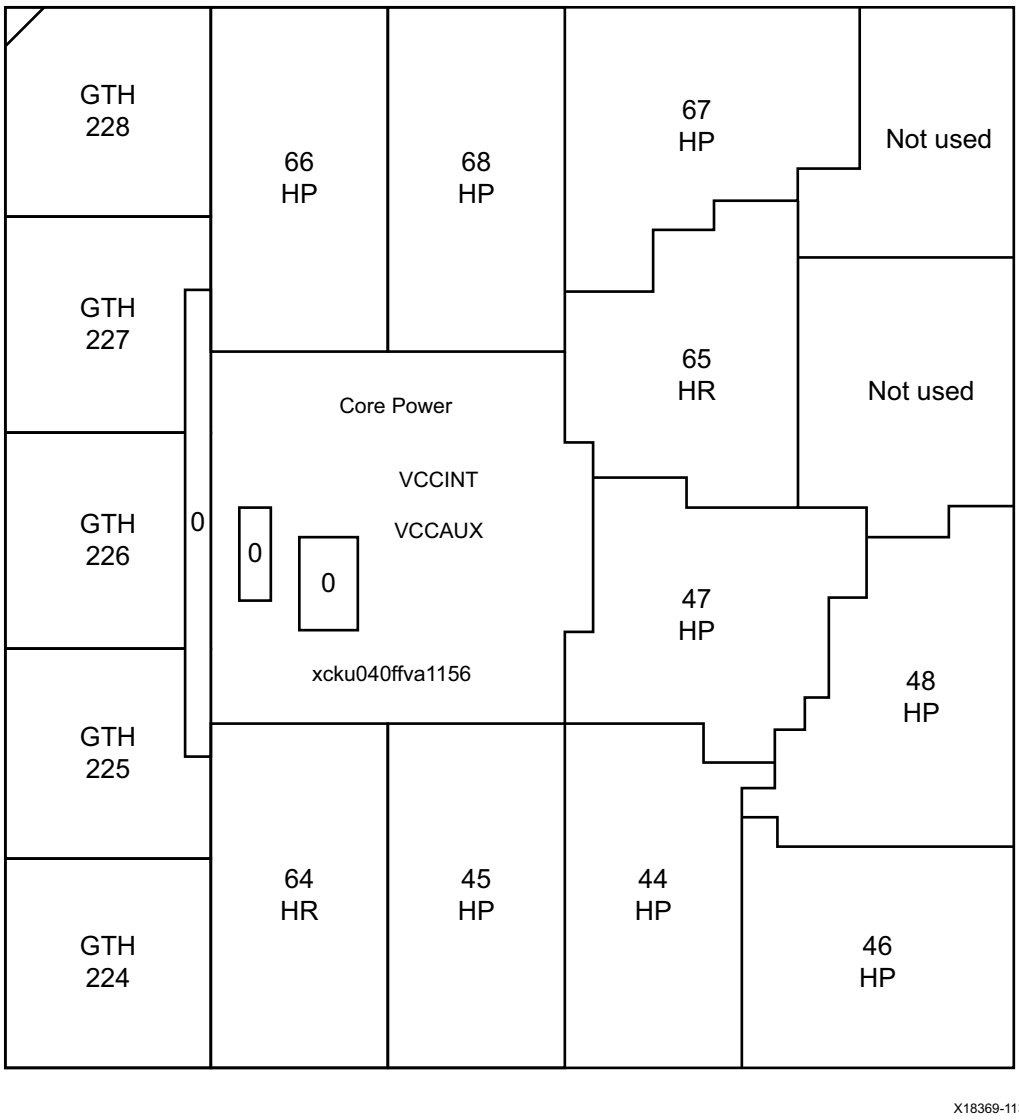


Figure 1-5: **UltraScale XCKU040 Bank Locations**

Table 1-3: **I/O Bank Voltage Rails**

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
Bank 0	VCC1V8_FPGA	1.8V
HP Bank 44	VCC1V2_FPGA	1.2V
HP Bank 45	VCC1V2_FPGA	1.2V
HP Bank 46	VCC1V2_FPGA	1.2V
HP Bank 47	VADJ_1V8_FPGA	1.8V
HP Bank 48	VADJ_1V8_FPGA	1.8V
HR Bank 64	VCC1V8_FPGA	1.8V
HR Bank 65	VCC1V8_FPGA	1.8V
HP Bank 66	VADJ_1V8_FPGA	1.8V
HP Bank 67	VADJ_1V8_FPGA	1.8V
HP Bank 68	VADJ_1V8_FPGA	1.8V

DDR4 Component Memory

[Figure 1-2, callout 2]

The 2 GB DDR4 component memory system is comprised of four 256 Mb x 16 DDR4 SDRAM devices (Micron EDY4016AABG-DR-F-D) located at U60-U63. This memory system is connected to the XCKU040 HP banks 44, 45, and 46. The DDR4 0.6V VTT termination voltage (net DDR4_VTT) is sourced from the TI TPS51200DR linear regulator U24. The connections between the DDR4 component memories and the XCKU040 banks 44, 45, and 46 are listed in Table 1-4.

Table 1-4: **DDR4 Memory Connections to the FPGA**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
AE23	DDR4_DQ0	POD12_DCI	G2	DQL0	U60
AG20	DDR4_DQ1	POD12_DCI	F7	DQL1	U60
AF22	DDR4_DQ2	POD12_DCI	H3	DQL2	U60
AF20	DDR4_DQ3	POD12_DCI	H7	DQL3	U60
AE22	DDR4_DQ4	POD12_DCI	H2	DQL4	U60
AD20	DDR4_DQ5	POD12_DCI	H8	DQL5	U60
AG22	DDR4_DQ6	POD12_DCI	J3	DQL6	U60
AE20	DDR4_DQ7	POD12_DCI	J7	DQL7	U60
AJ24	DDR4_DQ8	POD12_DCI	A3	DQU0	U60
AG24	DDR4_DQ9	POD12_DCI	B8	DQU1	U60
AJ23	DDR4_DQ10	POD12_DCI	C3	DQU2	U60

Table 1-4: **DDR4 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
AF23	DDR4_DQ11	POD12_DCI	C7	DQU3	U60
AH23	DDR4_DQ12	POD12_DCI	C2	DQU4	U60
AF24	DDR4_DQ13	POD12_DCI	C8	DQU5	U60
AH22	DDR4_DQ14	POD12_DCI	D3	DQU6	U60
AG25	DDR4_DQ15	POD12_DCI	D7	DQU7	U60
AG21	DDR4_DQS0_T	DIFF_POD12_DCI	G3	DQSL_T	U60
AH21	DDR4_DQS0_C	DIFF_POD12_DCI	F3	DQSL_C	U60
AH24	DDR4_DQS1_T	DIFF_POD12_DCI	B7	DQSU_T	U60
AJ25	DDR4_DQS1_C	DIFF_POD12_DCI	A7	DQSU_C	U60
AD21	DDR4_DM0	POD12_DCI	E7	DML_B/DBIL_B	U60
AE25	DDR4_DM1	POD12_DCI	E2	DMU_B/DBIU_B	U60
AL22	DDR4_DQ16	POD12_DCI	G2	DQL0	U61
AL25	DDR4_DQ17	POD12_DCI	F7	DQL1	U61
AM20	DDR4_DQ18	POD12_DCI	H3	DQL2	U61
AK23	DDR4_DQ19	POD12_DCI	H7	DQL3	U61
AK22	DDR4_DQ20	POD12_DCI	H2	DQL4	U61
AL24	DDR4_DQ21	POD12_DCI	H8	DQL5	U61
AL20	DDR4_DQ22	POD12_DCI	J3	DQL6	U61
AL23	DDR4_DQ23	POD12_DCI	J7	DQL7	U61
AM24	DDR4_DQ24	POD12_DCI	A3	DQU0	U61
AN23	DDR4_DQ25	POD12_DCI	B8	DQU1	U61
AN24	DDR4_DQ26	POD12_DCI	C3	DQU2	U61
AP23	DDR4_DQ27	POD12_DCI	C7	DQU3	U61
AP25	DDR4_DQ28	POD12_DCI	C2	DQU4	U61
AN22	DDR4_DQ29	POD12_DCI	C8	DQU5	U61
AP24	DDR4_DQ30	POD12_DCI	D3	DQU6	U61
AM22	DDR4_DQ31	POD12_DCI	D7	DQU7	U61
AJ20	DDR4_DQS2_T	DIFF_POD12_DCI	G3	DQSL_T	U61
AK20	DDR4_DQS2_C	DIFF_POD12_DCI	F3	DQSL_C	U61
AP20	DDR4_DQS3_T	DIFF_POD12_DCI	B7	DQSU_T	U61
AP21	DDR4_DQS3_C	DIFF_POD12_DCI	A7	DQSU_C	U61
AJ21	DDR4_DM2	POD12_DCI	E7	DML_B/DBIL_B	U61
AM21	DDR4_DM3	POD12_DCI	E2	DMU_B/DBIU_B	U61
AH28	DDR4_DQ32	POD12_DCI	G2	DQL0	U62

Table 1-4: **DDR4 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
AK26	DDR4_DQ33	POD12_DCI	F7	DQL1	U62
AK28	DDR4_DQ34	POD12_DCI	H3	DQL2	U62
AM27	DDR4_DQ35	POD12_DCI	H7	DQL3	U62
AJ28	DDR4_DQ36	POD12_DCI	H2	DQL4	U62
AH27	DDR4_DQ37	POD12_DCI	H8	DQL5	U62
AK27	DDR4_DQ38	POD12_DCI	J3	DQL6	U62
AM26	DDR4_DQ39	POD12_DCI	J7	DQL7	U62
AL30	DDR4_DQ40	POD12_DCI	A3	DQU0	U62
AP29	DDR4_DQ41	POD12_DCI	B8	DQU1	U62
AM30	DDR4_DQ42	POD12_DCI	C3	DQU2	U62
AN28	DDR4_DQ43	POD12_DCI	C7	DQU3	U62
AL29	DDR4_DQ44	POD12_DCI	C2	DQU4	U62
AP28	DDR4_DQ45	POD12_DCI	C8	DQU5	U62
AM29	DDR4_DQ46	POD12_DCI	D3	DQU6	U62
AN27	DDR4_DQ47	POD12_DCI	D7	DQU7	U62
AL27	DDR4_DQS4_T	DIFF_POD12_DCI	G3	DQSL_T	U62
AL28	DDR4_DQS4_C	DIFF_POD12_DCI	F3	DQSL_C	U62
AN29	DDR4_DQS5_T	DIFF_POD12_DCI	B7	DQSU_T	U62
AP30	DDR4_DQS5_C	DIFF_POD12_DCI	A7	DQSU_C	U62
AH26	DDR4_DM4	POD12_DCI	E7	DML_B/DBIL_B	U62
AN26	DDR4_DM5	POD12_DCI	E2	DMU_B/DBIU_B	U62
AH31	DDR4_DQ48	POD12_DCI	G2	DQL0	U63
AH32	DDR4_DQ49	POD12_DCI	F7	DQL1	U63
AJ34	DDR4_DQ50	POD12_DCI	H3	DQL2	U63
AK31	DDR4_DQ51	POD12_DCI	H7	DQL3	U63
AJ31	DDR4_DQ52	POD12_DCI	H2	DQL4	U63
AJ30	DDR4_DQ53	POD12_DCI	H8	DQL5	U63
AH34	DDR4_DQ54	POD12_DCI	J3	DQL6	U63
AK32	DDR4_DQ55	POD12_DCI	J7	DQL7	U63
AN33	DDR4_DQ56	POD12_DCI	A3	DQU0	U63
AP33	DDR4_DQ57	POD12_DCI	B8	DQU1	U63
AM34	DDR4_DQ58	POD12_DCI	C3	DQU2	U63
AP31	DDR4_DQ59	POD12_DCI	C7	DQU3	U63
AM32	DDR4_DQ60	POD12_DCI	C2	DQU4	U63

Table 1-4: **DDR4 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
AN31	DDR4_DQ61	POD12_DCI	C8	DQU5	U63
AL34	DDR4_DQ62	POD12_DCI	D3	DQU6	U63
AN32	DDR4_DQ63	POD12_DCI	D7	DQU7	U63
AH33	DDR4_DQS6_T	DIFF_POD12_DCI	G3	DQSL_T	U63
AJ33	DDR4_DQS6_C	DIFF_POD12_DCI	F3	DQSL_C	U63
AN34	DDR4_DQS7_T	DIFF_POD12_DCI	B7	DQSU_T	U63
AP34	DDR4_DQS7_C	DIFF_POD12_DCI	A7	DQSU_C	U63
AJ29	DDR4_DM6	POD12_DCI	E7	DML_B/DBIL_B	U63
AL32	DDR4_DM7	POD12_DCI	E2	DMU_B/DBIU_B	U63
AE17	DDR4_A0	SSTL12_DCI	P3	A0	U60-U62
AH17	DDR4_A1	SSTL12_DCI	P7	A1	U60-U62
AE18	DDR4_A2	SSTL12_DCI	R3	A2	U60-U62
AJ15	DDR4_A3	SSTL12_DCI	N7	A3	U60-U62
AG16	DDR4_A4	SSTL12_DCI	N3	A4	U60-U62
AL17	DDR4_A5	SSTL12_DCI	P8	A5	U60-U62
AK18	DDR4_A6	SSTL12_DCI	P2	A6	U60-U62
AG17	DDR4_A7	SSTL12_DCI	R8	A7	U60-U62
AF18	DDR4_A8	SSTL12_DCI	R2	A8	U60-U62
AH19	DDR4_A9	SSTL12_DCI	R7	A9	U60-U62
AF15	DDR4_A10	SSTL12_DCI	M3	A10/AP	U60-U62
AD19	DDR4_A11	SSTL12_DCI	T2	A11	U60-U62
AJ14	DDR4_A12	SSTL12_DCI	M7	A12/BC_B	U60-U62
AG19	DDR4_A13	SSTL12_DCI	T8	A13	U60-U62
AD16	DDR4_A14_WE_B	SSTL12_DCI	L2	WE_B/A14	U60-U62
AG14	DDR4_A15_CAS_B	SSTL12_DCI	M8	CAS_B/A15	U60-U62
AF14	DDR4_A16_RAS_B	SSTL12_DCI	L8	RAS_B/A16	U60-U62
AF17	DDR4_BA0	SSTL12_DCI	N2	BA0	U60-U62
AL15	DDR4_BA1	SSTL12_DCI	N8	BA1	U60-U62
AG15	DDR4_BG0	SSTL12_DCI	M2	BG0	U60-U62
AH14	DDR4_ACT_B	SSTL12_DCI	L3	ACT_B	U60-U62
AH16	DDR4_TEN	SSTL12_DCI	N9	TEN	U60-U62
AJ16	DDR4_ALERT_B	SSTL12_DCI	P9	ALERT_B	U60-U62
AD18	DDR4_PAR	SSTL12_DCI	T3	PAR	U60-U62
AJ18	DDR4_ODT	SSTL12_DCI	K3	ODT	U60-U62

Table 1-4: **DDR4 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin #	Pin Name	Ref. Des.
AL19	DDR4_CS_B	SSTL12_DCI	L7	CS_B	U60-U62
AD15	DDR4_CKE	SSTL12_DCI	K2	CKE	U60-U62
AL18	DDR4_RESET_B	LVCMOS12	P1	RESET_B	U60-U62
AE16	DDR4_CK_T	DIFF_SSTL12_DCI	K7	CK_T	U60-U62
AE15	DDR4_CK_C	DIFF_SSTL12_DCI	K8	CK_C	U60-U62

The KCU105 board DDR4 memory component interface adheres to the constraints guidelines documented in the DDR4 Design Guidelines section of *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 3] and in *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide (Vivado Design Suite)* (PG150) [Ref 4]. The KCU105 board DDR4 memory component interface is a 40Ω impedance implementation. For more details about the Micron DDR4 component memory, see the Micron EDY4016AABG-DR-F-D data sheet at the Micron website [Ref 5].

Dual Quad-SPI Flash Memory

[Figure 1-2, callout 3]

The Quad-SPI flash memory located at U35 and U36 provides 2 x 256 Mb of nonvolatile storage that can be used for configuration and data storage. For details on FPGA configuration operation and implementation related to the dual Quad-SPI interfaces, see *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2].

- Part number: N25Q256A11ESF40F (Micron)
- Supply voltage: 1.8V
- Datapath width: 4 bits
- Data rate: various depending on single/dual/quad mode

The connections between the SPI flash memories and the XCKU040 device are listed in Table 1-5.

Table 1-5: **Quad-SPI Flash Memory Connections to FPGA U1**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Pin #	Pin Name	Ref. Des.
AC7	QSPI0_IO0	LVCMOS18	15	SI_IO0	U35
AB7	QSPI0_IO1	LVCMOS18	8	SI_IO1	U35
AA7	QSPI0_IO2	LVCMOS18	9	SI_IO2	U35
Y7	QSPI0_IO3	LVCMOS18	1	SI_IO3	U35
AA9	FPGA_CCLK	NA(1)	16	SCK	U35, U36
U7	QSPI0_CSB	LVCMOS18	7	CS_B	U35
M20	QSPI1_IO0	LVCMOS18	15	SI_IO0	U36
L20	QSPI1_IO1	LVCMOS18	8	SI_IO1	U36
R21	QSPI1_IO2	LVCMOS18	9	SI_IO2	U36
R22	QSPI1_IO3	LVCMOS18	1	SI_IO3	U36
G26	QSPI1_CSB	LVCMOS18	7	CS_B	U36

Notes:

1. CCLK is a dedicated pin and does not require an IOSTANDARD or LOC attribute.

Figure 1-6 shows the connections of the linear Quad-SPI flash memory on the KCU105 evaluation board. For more details, see the Micron N25Q256A11ESF40F data sheet at the Micron website [Ref 5].

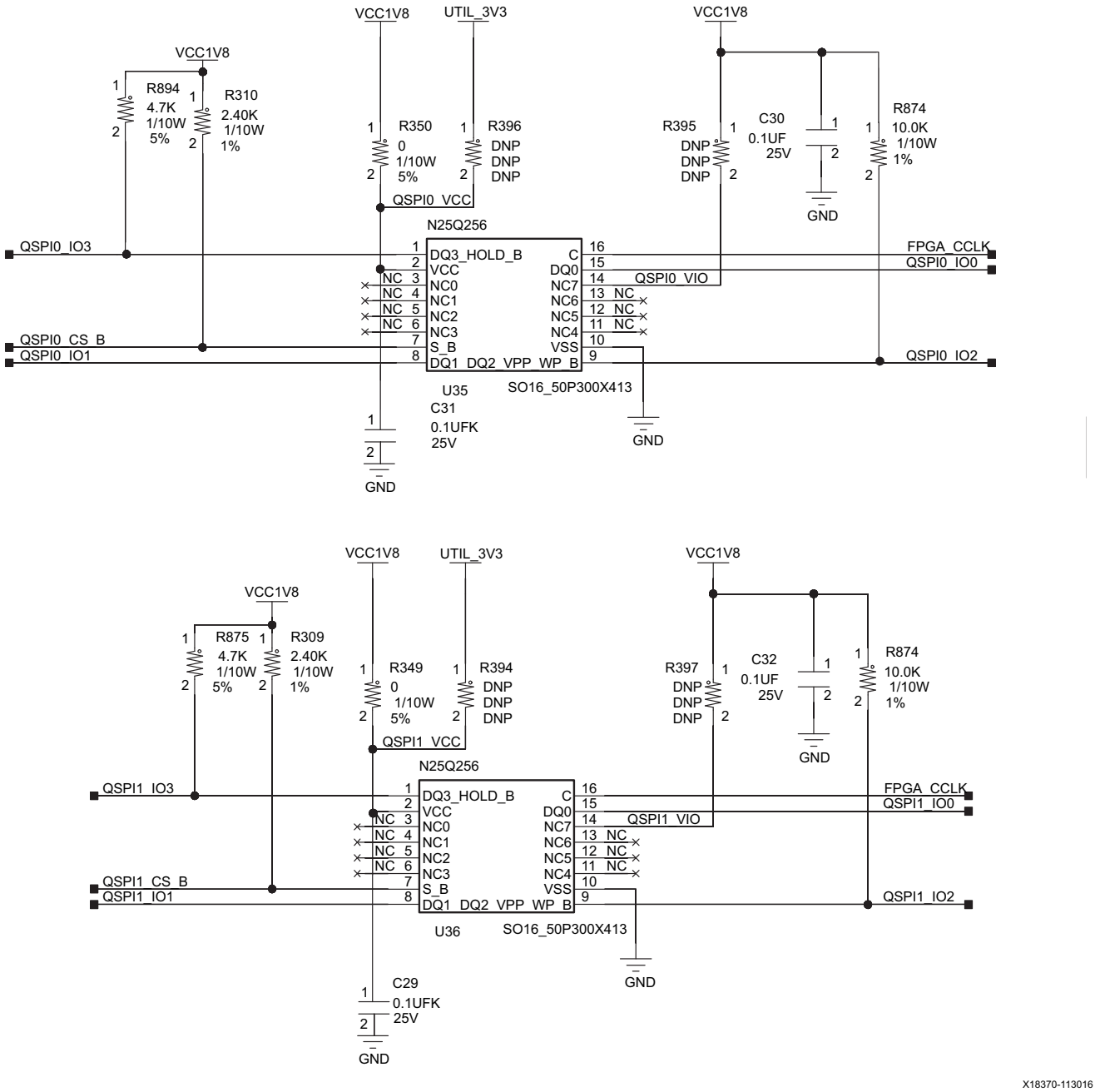


Figure 1-6: **Dual Quad-SPI 256 Mb Flash Memory**

Micro-SD Card Interface

[Figure 1-2, callout 4]

The KCU105 board includes a secure digital input/output (SDIO) interface to provide access to general purpose nonvolatile micro-SD memory cards and peripherals. The micro-SD card slot supports 50 MHz high-speed micro-SD cards. The SDIO signals are connected to I/O bank 64, which has its VCCO set to 1.8V. Fairchild FSSD07 (U107) and STMicroelectronics STG3220 (U110) 2:1 multiplexers are used between the FPGA and the micro-SD card connector (J83), and the XC7Z010 system controller (U111), and the micro-SD card connector (J83). Table 1-6 shows the connections of the SD card interface to the FPGA (U1) on the KCU105 board.

Table 1-6: **SDIO Connections to FPGA U1**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	SD MUX/Level-Shifter (U107)				Schematic Net Name	SDIO Connector (J83)	
			Pin #	Pin Name	Pin #	Pin Name		Pin #	Pin Name
AD9	SDIO_CMD_FPGA	LVCMOS18	13	2CMD	2	CMD	SDIO_CMD_HDR	3	CMD
AL10	SDIO_CLK_FPGA	LVCMOS18	11	2CLK	5	CLK	SDIO_CLK_HDR	5	CLK
AH9	SDIO_DATA2_FPGA	LVCMOS18	15	2DAT_2	24	DAT_2	SDIO_DATA2_HDR	1	DAT2
AN9	SDIO_DATA1_FPGA	LVCMOS18	9	2DAT_1	7	DAT_1	SDIO_DATA1_HDR	8	DAT1
AP9	SDIO_DATA0_FPGA	LVCMOS18	10	2DAT_0	6	DAT_0	SDIO_DATA0_HDR	7	DAT0
AH8	SDIO_DATA3_FPGA	LVCMOS18	14	2DAT_3	1	DAT_3	SDIO_DATA3_HDR	2	CD_DAT3
			DUAL SPDT CMOS SWITCH (U110)						
			Pin #	Pin Name	Pin #	Pin Name			
AM10	SDIO_CD_FPGA	LVCMOS18	4	2S1	6	D2	SDIO_CD_HDR	13	DETECT

Figure 1-7 shows the connections of the SD card interface on the KCU105 board.

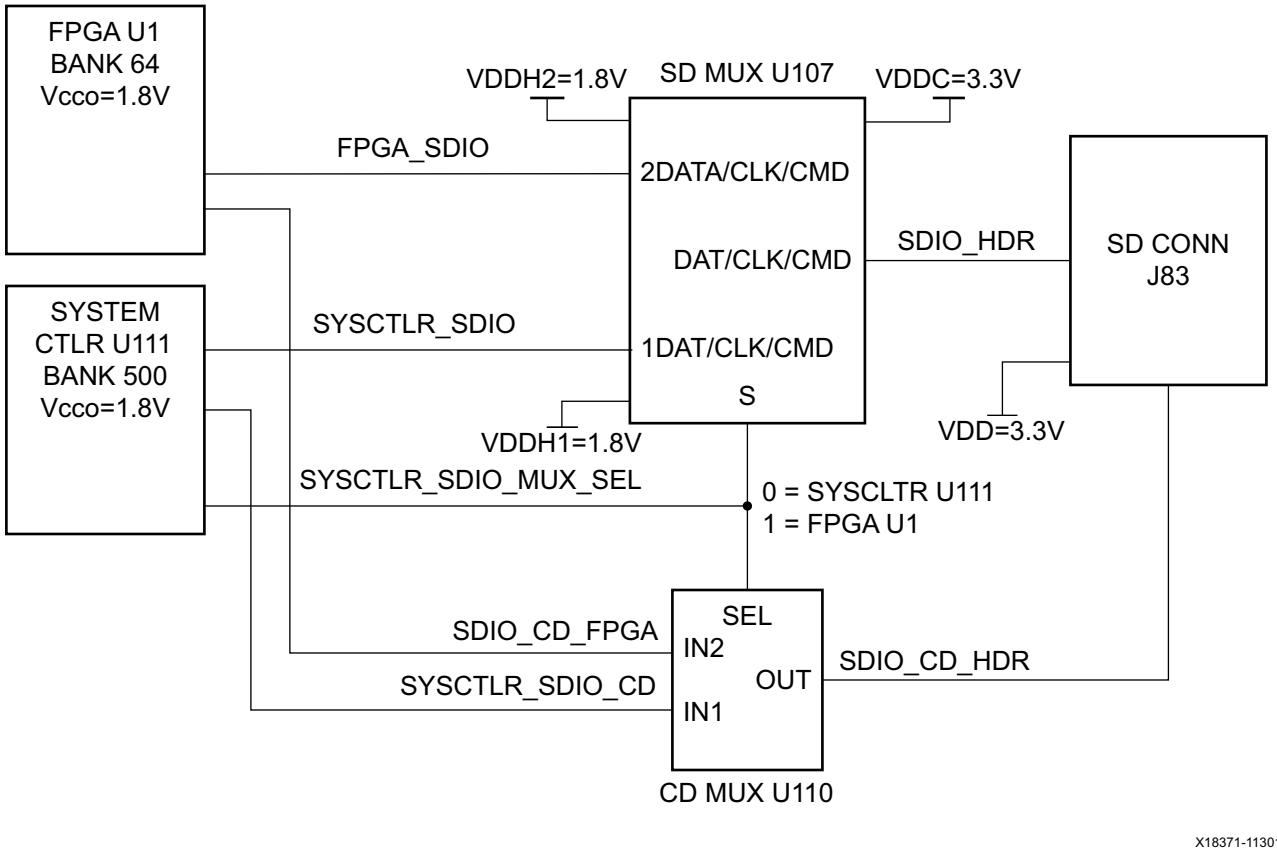


Figure 1-7: **SD Connector Circuit Topology**

For more details about the multiplexer devices, see the Fairchild FSSD07 data sheet at the Fairchild Semiconductor website [Ref 6] and the STMicroelectronics STG3220 data sheet at the STMicroelectronics website [Ref 7]. For more information on Secure Digital nonvolatile memory card technology, see the SanDisk Corporation website [Ref 8] and the SD Association website [Ref 9].