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ZCU104 Evaluation Board

User Guide

UG1267 (v1.0) April 4, 2018

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/04/2018	1.0	Initial Xilinx release.

Table of Contents

Introduction

Overview

The embedded vision low cost (EVLC) development kit enables automotive, AR/VR, drones, machine vision, and industrial vision developers to build, prototype, and test their designs on a Zynq® UltraScale+™ MPSoC XCZU7EV-2FFVC1156 device. The ZU7EV device integrates a quad core ARM® Cortex™-A53 processing system (PS) and a dual-core ARM Cortex-R5 real-time processor, which provides application developers an unprecedented level of heterogeneous multiprocessing. The ZCU104 evaluation board provides a flexible prototyping platform with high-speed DDR4 memory interfaces, an FMC expansion port, multi-gigabit per second serial transceivers, a variety of peripheral interfaces, and FPGA fabric for customized designs. The ZCU104 reVISION package provides out-of-box SDSoC™ software development flow with OpenCV libraries, machine learning framework, and live sensor support.

Additional Resources

See Appendix D, Additional Resources and Legal Notices for references to documents, files, and resources relevant to the ZCU104 evaluation board.

Block Diagram

The ZCU104 board block diagram is shown in Figure 1-1.

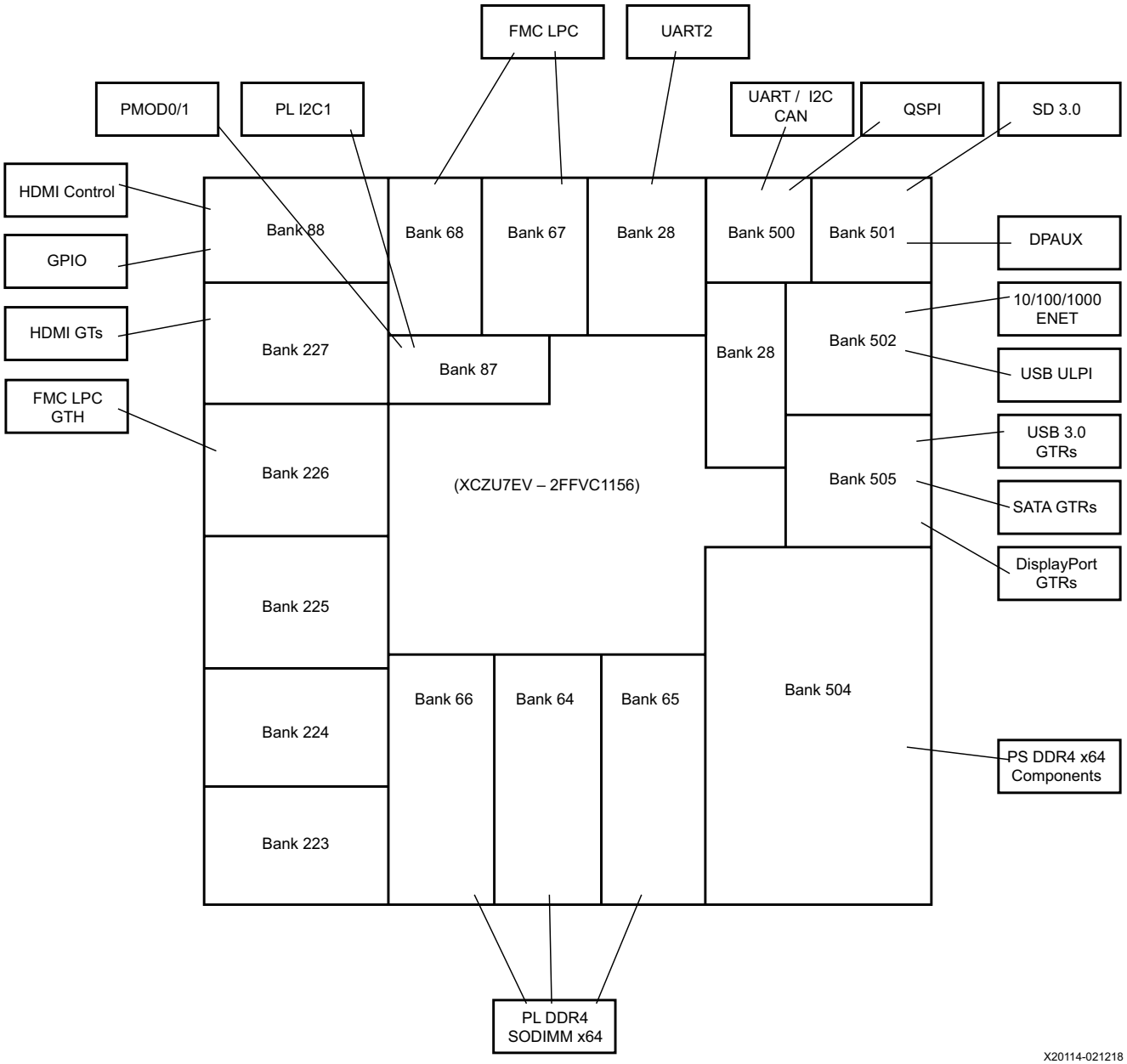

Figure 1-1: **ZCU104 Evaluation Board Block Diagram**

Board Features

The ZCU104 evaluation board features are listed here. Detailed information for each feature is provided in Component Descriptions in Chapter 3.

- XCZU7EV-2, FFVC1156 package
- PL V_{CCINT} for range in data sheet
- Rectangular form factor for benchtop use
- Configuration from Quad SPI
- Configuration from SD card
- Configuration over JTAG with platform cable USB header
- Configuration over USB-to-JTAG bridge
- IDT 8T49N287A clock chip
  - HDMI_DRU_CLOCK
  - PS_REF_CLK
  - GTR_REF_CLK_USB3
  - GTR_REF_CLK_DP
  - CLK_300
  - GTR_REF_CLK_SATA
  - CLK_125
- PS DDR4 64-bit component (4x16-bit)
- PL DDR4 64-bit SODIMM socket
- PS GTR assignment
  - DisplayPort (two GTRs)
  - USB3 (one GTR)
  - SATA (one GTR)
- PL GTH transceiver assignment (4 of 20 used)
  - High-definition multimedia interface (HDMI®) (three GTH transceivers)
  - FMC LPC DP (one GTH transceiver)
- PL FMC LPC connectivity - full LA bus
- PS MIO: single Quad SPI
- PS MIO: two channels of quad-UART bridge

- PS MIO: CAN
- PS MIO: I2C shared across PS and PL
- PS MIO: SD
- PS MIO: DisplayPort
- PS MIO: Ethernet
- PS MIO: USB3
- PS-side user LED (one)
- PL-side user LEDs (four)
- PL-side user DIP switch (4-position)
- PL-side user pushbuttons (four)
- PL-side CPU reset pushbutton
- PL-side PMOD headers
- PL-side bank 0 PROG_B pushbutton
- Security - PSBATT button battery backup
- Operational switches (power on/off, PROG_B, boot mode DIP switch)
- Operational status LEDs (power status, INIT, DONE, PG, DDR power good)
- Power management

The ZCU104 provides a rapid prototyping platform for the embedded vision low cost (EVLC) market using the XCZU7EV-2FFVC1156 device. The ZU7EV contains PS hard block peripherals exposed through the multi-use I/O (MIO) interface and several FPGA programmable logic (PL), high-density (HD), and high-performance (HP) banks. Table 1-1 lists the resources available within the ZU7EV. See the *Zynq UltraScale+ MPSoC Data Sheet: Overview* (DS891) [Ref 1] for a feature set overview, description, and ordering information.

Table 1-1: **Zynq UltraScale+ MPSoC ZU7EV Features and Resources**

Feature	Resource Count
Quad core ARM Cortex-A53 MPCore	1
Dual core ARM Cortex-R5 MPCore	1
Mali-400 MP2 GPU	1
H.264/H.265 VCU	1
HD banks	Two banks, total of 48 pins
HP banks	Six banks, total of 312 pins
MIO banks	Three banks, total of 78 pins
PS-GTR transceivers (6 Gb/s)	Four PS-GTR transceivers
GTH transceivers (16.3 Gb/s)	20 GTH transceivers
System logic cells	504K
CLB flip-flops	461K
Maximum distributed RAM	6.2 Mb
Total block RAM	11 Mb
UltraRAM	27 Mb
DSP slices	1,728

Board Specifications

Dimensions

Height: 5.90 inch (14.98 cm)

Length: 7.05 inch (17.91 cm)

Thickness: 0.062 inch ±0.005 inch (0.157 cm ±0.0127 cm)

Note: A 3D model of this board is not available.

See ZCU104 board documentation for XDC listing, schematics, layout files, board outline drawings, etc.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Board Setup and Configuration

Board Component Location

Figure 2-1 shows the ZCU104 board component locations. Each numbered component shown in the figure is keyed to Table 2-1. Table 2-1 identifies the components, references the respective schematic (0381794) page numbers, and links to a detailed functional description of the components and board features in Chapter 3.

IMPORTANT: *Figure 2-1 is for visual reference only and might not reflect the current revision of the board.*

IMPORTANT: *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific ZCU104 version of interest for such details.*

CAUTION! *The ZCU104 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.*

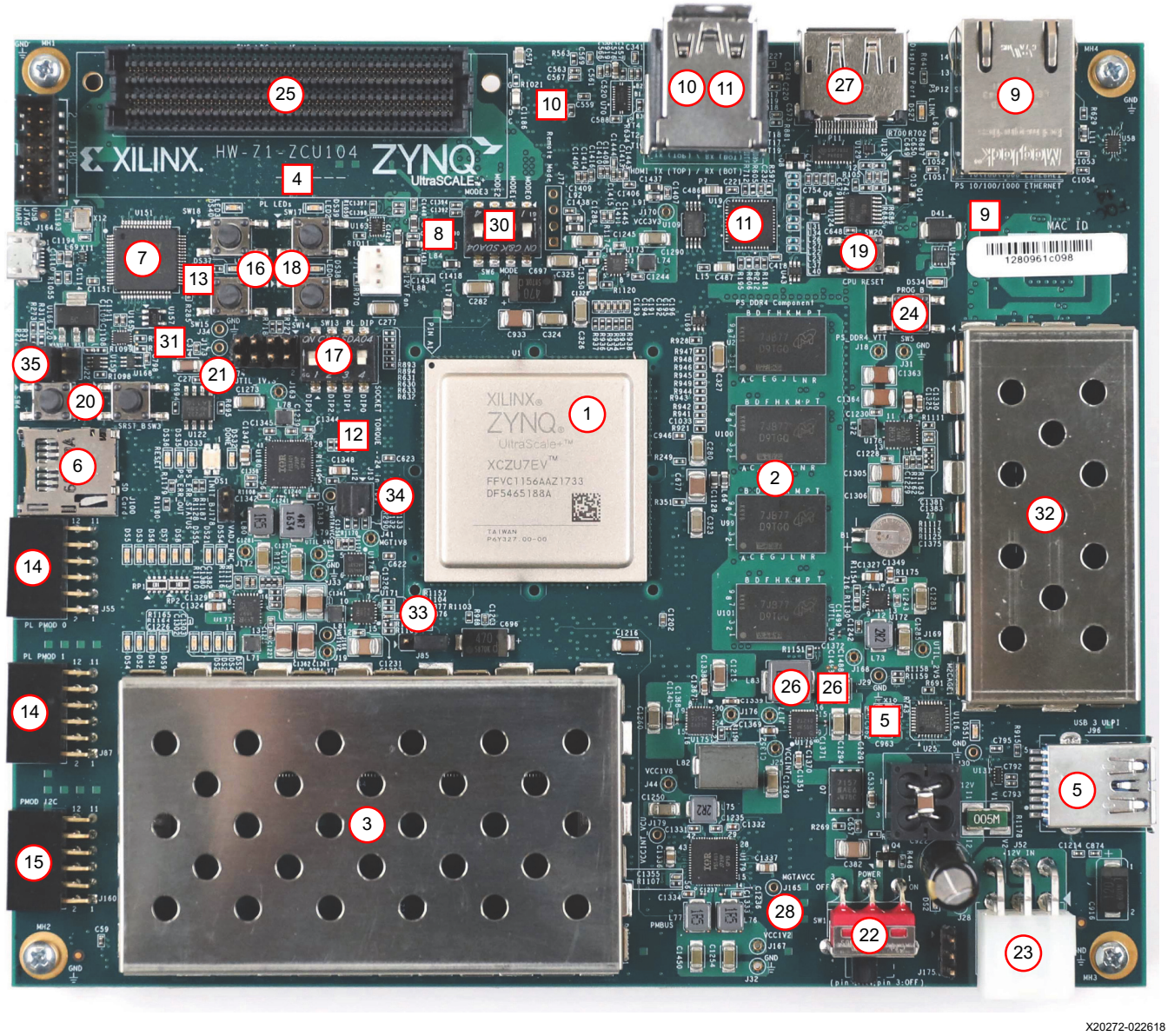

Figure 2-1: **ZCU104 Evaluation Board Components**

Table 2-1: **ZCU104 Board Component Locations**

Callout Number	Ref. Des.	Feature ([B] = bottom of board)	Notes	Schematic Page
1	U1	Zynq UltraScale+ XCZU7EV MPSoC with Radian fan sink	XCZU7EV-2FFVC1156 FA35+K52B+T725	3–18
2	U2, U99-U101	PS-Side: DDR4 Component Memory, (2 GB total)	Micron MT40A256M16GE-083E (DDR4-2400)	24–27
3	J1	PL-Side: DDR4 SODIMM Socket DDR4 SODIMM (not provided)	LOTES ADDR0067-P001A, supports MICRON MTA8ATF51264HZ-2G6B1	22
4	U119	Quad SPI Flash Memory (MIO 0–5) (512 Mb) [B]	Micron MT25QU512ABB8ESF-0SIT	36
5	U116, J96	USB 3.0 Transceiver and USB 2.0 ULPI PHY USB Micro-AB connector	SMSC USB3320-EZK, KYCON KMMX-AB10-SMT1SB30TR	40
6	J100	SD Card Interface connector	Hirose DMIAA-SF-PET(21)	37
7	U151, J164	Programmable Logic JTAG Programming Options	FTDI FT4232HL_64LQFP, Hirose ZX62D-AB-5P8	21
8	U182	IDT8T49N287 FemtoClock NG Octal Universal Frequency Translator [B]	IDT 8T49N287A-501NLGI	32
9	U98, P12	10/100/1000 MHz Tri-Speed Ethernet PHY [B], RJ45 with magnetics	TI DP83867IRPAP, Bel Fuse L829-1J1T-43	41
10	U94, P7	HDMI Video Output [B]	TI SN65DP159RGZ, TE Connectivity 1888811-1	29
11	U19, P7	HDMI Video Output	TI TMDS181IRGZT, TE Connectivity 1888811-1	30
12	U97	I2C1 (MIO 16-17) [B]	TI TCA6416APWR	44
13	U34	I2C1 (MIO 16-17) [B]	TI TCA9548APWR	45
14	J55, J87	User PMOD GPIO Connectors	SULLINS PPPC062LJBN-RC	43
15	J160	User I2C1 Receptacle	SULLINS PPPC062LJBN-RC	43
16	DS37-DS40	User I/O (4 x green 0603 LED)	LUMEX SML-LX0603GW	42
17	SW13	User I/O (4-pos. DIP switch)	CTS 218-4LPSTRF	42
18	SW14, 15, 17, 18	User I/O (4 X SPST pushbutton)	E-switch TL3301EP100QG	42
19	SW20	User I/O (CPU reset SPST pushbutton)	E-switch TL3301EP100QG	42
20	SW3, SW4	Switches (2 x SPST pushbutton, POR)	E-switch TL3301EP100QG	12
21	U122, J98	User I2C1 Receptacle	TI SN65HVD232, SULLINS PBC36DAAN	39

Table 2-1: **ZCU104 Board Component Locations *(Cont'd)***

Callout Number	Ref. Des.	Feature ([B] = bottom of board)	Notes	Schematic Page
22	SW1	Switches Power on/off slide switch)	C&K 1201M2S3AQE2	46
23	J52	Switches (2 x 3 mini-fit receptacle)	MOLEX 39-30-1060	46
24	SW5	Switches (PROG_B SPST pushbutton)	E-switch TL3301EP100QG	12
25	J5	FMC LPC Connector J5	Samtec ASP_134603_01	28
26	–	Board Power System (top and bottom of board)	Maxim Regulators	47–60
27	P11	DPAUX (MIO 27-30)	MOLEX 0472720001	34
28	J175	Monitoring Voltage and Current	Sullins PBC36SAAN (1x3 0.1 male pin header)	44
29	U181	HDMI Clock Recovery [B]	IDT8T49N241-994NLGI	31
30	SW6	Switches (MODE 4-pole DIP)	4-pole C&K SDA04H1SBD	12
31	U23	I2C1 (MIO 16-17) [B] (8 Kb EEPROM)	ST MICRO M24C08-WDW6TP	33
32	U170	PS M.2 SATA Connector	Amphenol MDT420M02001	38
33	J85	Jumpers (POR Override Sel)	Sullins PBC36SAAN (1x3 0.1 male pin header	3
34	J12, J13	Jumpers (SYSMON I2C ADDR)	Sullins PBC36SAAN (1x3 0.1 male pin header	3
35	J20, J21, J22	Jumpers (POR circuit)	Sullins PBC36SAAN (1x3 0.1 male pin header	12

Default Jumper and Switch Settings

Figure 2-1 shows the ZCU104 board jumper header and DIP switch locations. Each numbered component shown in the figure is keyed to Table 2-2 (for default jumper settings) or Table 2-3 (for default switch settings). Both tables reference the respective schematic page numbers.

Jumpers

Table 2-2: **Default Jumper Settings**

Number	Ref. Des.	Function	Default	Schematic Page
33	J85	POR_OVERRIDE • 1-2: Enable • 2-3: Disable	2-3	3
34	J12	SYSMON I2C address • Open: SYSMON_VP_R floating • 1-2: SYSMON_VP_P pulled down	1-2	3
34	J13	SYSMON I2C address • Open: SYSMON_VN_R floating • 1-2: SYSMON_VP_N pulled down	1-2	3
35	J20	Reset sequencer PS_POR_B • Open: Sequencer does not control PS_POR_B • 1-2: Sequencer can control PS_POR_B	1-2	12
35	J21	Reset sequencer PS_SRST_B • Open: Sequencer does not control PS_SRST_B • 1-2: Sequencer can control PS_SRST_B	1-2	12
35	J22	Reset sequencer inhibit • Open: Sequencer normal operation • 1-2: Sequencer inhibit (resets stay asserted)	Open	12

Switches

Table 2-3: **Default Switch Settings**

Number	Ref. Des.	Function	Default	Schematic Page
30	SW6	4-pole DIP switch PS_MODE select = [0010]		12
		(ON = pull down, OFF = pull up = 1)		
		4: PS_MODE3 PS_MODE[3:0] = 0010	On	
		3: PS_MODE2 = QSPI32 boot default	On	
		2: PS_MODE1	Off	
		1: PS_MODE0	On	
17	SW13	4-pole DIP switch GPIO	All Off	42
22	SW1	Main power slide switch	Off	46

MPSoC Device Configuration

Zynq UltraScale+ XCZU7EV MPSoC devices use a multi-stage boot process as described in the "Boot and Configuration" chapter of the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2]. Switch SW6 configuration option settings are listed in Table 2-4.

Table 2-4: **Switch SW6 Configuration Option Settings**

Boot Mode	Mode Pins [3:0]	Mode SW6 [4:1]
JTAG	0000/0x0	ON,ON,ON,ON
QSPI32	0010/0x2(1)	ON,ON,OFF,ON
SD1	1110/0xE	OFF,OFF,OFF,ON

Notes:

1. Default switch setting.

JTAG

Vivado®, SDK, or third-party tools can establish a JTAG connection to the Zynq UltraScale+ MPSoC device through the FT4232 Quad USB to multipurpose UART (U151) with micro-USB connector (J164).

Quad SPI

To boot from the dual Quad SPI nonvolatile configuration memory:

1. Store a valid Zynq UltraScale+ MPSoC boot image in the Quad SPI flash device (U119) connected to the MIO Quad SPI interface.
2. Set the boot mode pins SW6 [4:1] PS_MODE[3:0] as indicated in Table 2-4 for Quad SPI32.
3. Either power-cycle or press the power-on reset (POR) pushbutton SW4. SW4 is callout 20 in Figure 2-1.

SD

To boot from an SD card:

1. Store a valid Zynq UltraScale+ MPSoC boot image file on to an SD card (plugged into SD socket J100) connected to the MIO SD interface.
2. Set the boot mode pins SW6 [4:1] PS_MODE[3:0] as indicated in Table 2-4 for SD1.
3. Either power-cycle or press the power-on reset (POR) pushbutton SW4. SW4 is callout 20 in Figure 2-1.

See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more information about Zynq UltraScale+ MPSoC configuration options.

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. Table 2-1, page 13 identifies the components, references the respective schematic (0381794) page numbers, and links to the corresponding detailed functional description in this chapter. Component locations are shown in Table 2-1, page 13.

Component Descriptions

Zynq UltraScale+ XCZU7EV MPSoC

[Figure 2-1, callout 1]

The ZCU104 board is populated with the Zynq UltraScale+ XCZU7EV-2FFVC1156 MPSoC, which combines a powerful processing system (PS) and programmable logic (PL) in the same device. The PS in a Zynq UltraScale+ MPSoC features the ARM® flagship Cortex®-A53 64-bit quad-core processor and Cortex-R5 dual-core real-time processor. Support of multiple speed grades requires voltage adjustments.

The V_{CCINT} supplies are user adjustable via the PMBus with the voltage ranges listed in Table 3-1 to support multiple Zynq UltraScale+ MPSoC speed grades.

Table 3-1: **Recommended Operating Conditions**

Symbol	Description	Min	Typ	Max	Units
Processing System					
$V_{CC\_PSINTFP}$	PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS full-power domain supply voltage.	0.873	0.900	0.927	V
$V_{CC\_PSINTLP}$	PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS low-power domain supply voltage.	0.873	0.900	0.927	V
Programmable Logic					
V_{CCINT}	PL internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: PL internal supply voltage.	0.873	0.900	0.927	V

The top-level block diagram is shown in Figure 3-1.

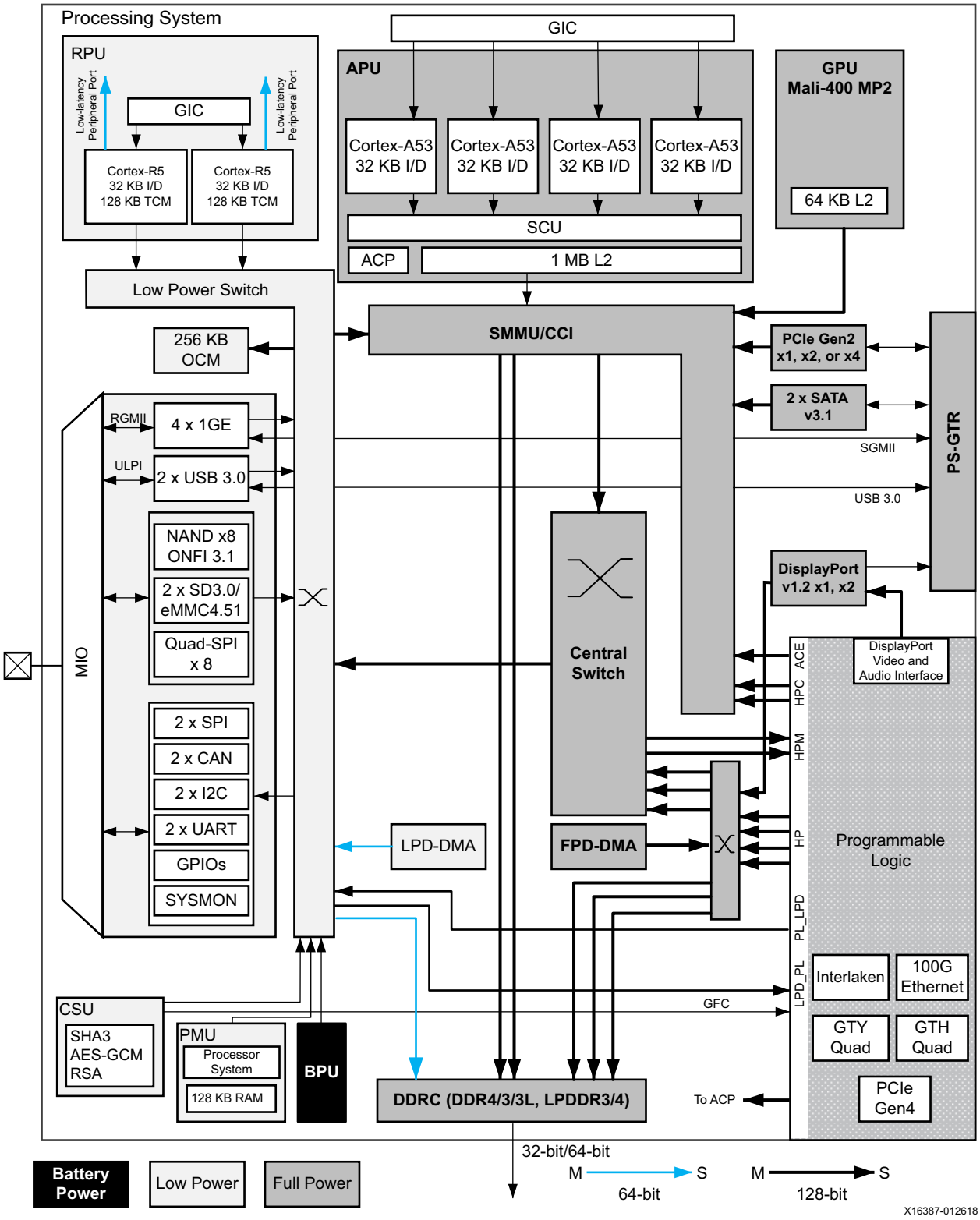

Figure 3-1: **Top-Level Block Diagram**

The Zynq UltraScale+ MPSoC PS block has three major processing units:

- Cortex-A53 application processing unit (APU)-ARM v8 architecture-based 64-bit quad-core multiprocessing CPU.
- Cortex-R5 real-time processing unit (RPU)-ARM v7 architecture-based 32-bit dual real-time processing unit with dedicated tightly coupled memory (TCM).
- Mali-400 graphics processing unit (GPU)-graphics processing unit with pixel and geometry processor and 64 KB L2 cache.

The Zynq UltraScale+ MPSoC PS has four high-speed serial I/O (HSSIO) interfaces supporting these protocols:

- Integrated block for PCI Express® interface-PCIe™ base specification version 2.1 compliant.
- SATA 3.1 specification compliant interface.
- DisplayPort interface-implements a DisplayPort source-only interface with video resolution up to 4K x 2K-30 (300 MHz pixel rate).
- USB 3.0 interface-compliant to USB 3.0 specification implementing a 5 Gb/s line rate.
- Serial GMII interface-supports a 1 Gb/s SGMII interface.

The PS and PL can be coupled with multiple interfaces and other signals to effectively integrate user-created hardware accelerators and other functions in the PL logic that are accessible to the processors. They can also access memory resources in the PS. The PS I/O peripherals, including the static/flash memory interfaces share a multiplexed I/O (MIO) of up to 78 MIO pins. Zynq UltraScale+ MPSoCs can also use the I/O in the PL domain for many of the PS I/O peripherals. This is done through an extended multiplexed I/O interface (EMIO).and boots at power-up or reset.

For additional information on Zynq UltraScale+ MPSoC devices, see the *Zynq UltraScale+ MPSoC Data Sheet: Overview* (DS891) [Ref 1]. See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more information about Zynq UltraScale+ MPSoC configuration options.

Encryption Key Battery Backup Circuit

The XCZU7EV MPSoC U1 implements bit stream encryption key technology. The ZCU104 board provides the encryption key backup battery circuit shown in Figure 3-2.

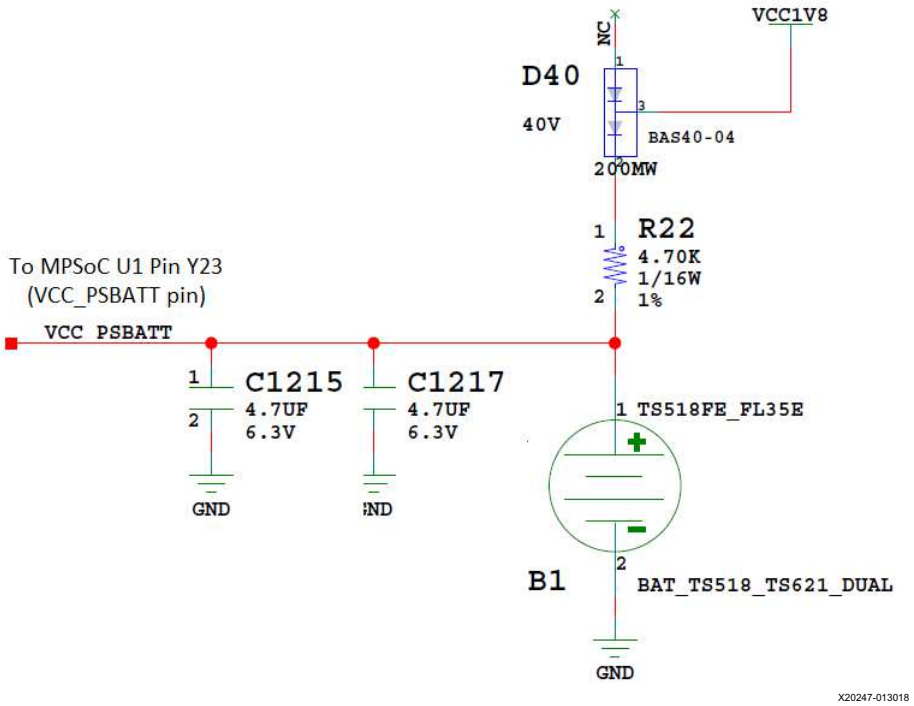

Figure 3-2: **Encryption Key Backup Circuit**

The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCZU7EV MPSoC U1 V_{CC_PSBATT} pin Y23. The battery supply current I_{BATT} specification is 150 nA maximum when board power is off. B1 is charged from the UTIL_1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 ΩK current limit resistor. The nominal charging voltage is 1.42V.

I/O Voltage Rails

The XCZU7EV MPSoC PL I/O bank voltages on the ZCU104 board are listed in Figure 3-2.

Table 3-2: **I/O Voltage Rails**

XCZU7EV	Power Net Name	Voltage	Connected To
PL Bank 28	V_{CC1V8}	1.8V	UART2 only (mostly NC pins)
PL Bank 64	V_{CC1V2}	1.2V	DDR4 SODIMM DQ[0:31] (PL)
PL Bank 65	V_{CC1V2}	1.2V	DDR4 SODIMM DQ[32:63] (PL)
PL Bank 66	V_{CC1V2}	1.2V	DDR4 SODIMM ADDR/CTRL (PL)
PL Bank 67	V_{ADJ_FMC}(1)	1.8V	FMC_LPC LA BUS
PL Bank 68	V_{ADJ_FMC}(1)	1.8V	FMC_LPC LA BUS
PL Bank 87	V_{CC3V3}	3.3V	PMOD0, PMOD1, HDMI CTRL, PL_I2C1
PL Bank 88	V_{CC3V3}	3.3V	HDMI, GPIO LED/DIP SW/PB SW
PS Bank 500	V_{CC1V8}	1.8V	CAN, UART0/1, I2C0/1, QSPI LWR
PS Bank 501	V_{CC1V8}	1.8V	SDIO, DP
PS Bank 502	V_{CC1V8}	1.8V	ENET, USB_DATA[0:7], USB_CTRL
PS Bank 503	V_{CC1V8}	1.8V	PS CONFIG I/F
PS Bank 504	V_{CC1V2}	1.2V	DDR4 (4x16-BIT) 64-BIT COMPONENT I/F (PS)

Notes:

1. The ZCU104 board is shipped with V_{ADJ_FMC} set to 1.8V.

PS-Side: DDR4 Component Memory

[Figure 2-1, callout 2]

The PS-side memory is wired to the Zynq UltraScale+ DDRC bank 504 hard memory controller. PS-side memory is a 2 GB, 64-bit wide DDR4 memory system comprised of four 256 Mb x 16 SDRAMs (Micron MT40A256M16HA-083E) U2, and 99-101. The DDR4 0.6V VTT termination voltage is supplied from sink-source regulator U178. The connections between the DDR4 memory and the U1 XCZU7EV bank 504 are listed in Table 3-3.

Table 3-3: **DDR4 Component Memory Connection to XCZU7EV PS Bank 504**

XCZU7EV (U1) Pin	Net Name	DDR4 Component Memory		
		Pin #	Pin Name	Ref. Des.
AN34	DDR4_A0	P3	A0	U2,U99-U101
AM34	DDR4_A1	P7	A1	U2,U99-U101
AM33	DDR4_A2	R3	A2	U2,U99-U101
AL34	DDR4_A3	N7	A3	U2,U99-U101
AL33	DDR4_A4	N3	A4	U2,U99-U101
AK33	DDR4_A5	P8	A5	U2,U99-U101
AK30	DDR4_A6	P2	A6	U2,U99-U101
AJ30	DDR4_A7	R8	A7	U2,U99-U101
AJ31	DDR4_A8	R2	A8	U2,U99-U101
AH31	DDR4_A9	R7	A9	U2,U99-U101
AG31	DDR4_A10	M3	A10/AP	U2,U99-U101
AF31	DDR4_A11	T2	A11	U2,U99-U101
AG30	DDR4_A12	M7	A12/BC_B	U2,U99-U101
AF30	DDR4_A13	T8	A13	U2,U99-U101
AE27	DDR4_BA0	N2	BA0	U2,U99-U101
AE28	DDR4_BA1	N8	BA1	U2,U99-U101
AD27	DDR4_BG0	M2	BG0	U2,U99-U101
AP27	DDR4_DQ0	G2	DQL0	U101
AP25	DDR4_DQ1	F7	DQL1	U101
AP26	DDR4_DQ2	H3	DQL2	U101
AM26	DDR4_DQ3	H7	DQL3	U101
AP24	DDR4_DQ4	H2	DQL4	U101
AL25	DDR4_DQ5	H8	DQL5	U101
AM25	DDR4_DQ6	J3	DQL6	U101
AM24	DDR4_DQ7	J7	DQL7	U101
AM28	DDR4_DQ8	A3	DQU0	U101

Table 3-3: **DDR4 Component Memory Connection to XCZU7EV PS Bank 504 *(Cont'd)***

XCZU7EV (U1) Pin	Net Name	DDR4 Component Memory		
		Pin #	Pin Name	Ref. Des.
AN28	DDR4_DQ9	B8	DQU1	U101
AP29	DDR4_DQ10	C3	DQU2	U101
AP28	DDR4_DQ11	C7	DQU3	U101
AM31	DDR4_DQ12	C2	DQU4	U101
AP31	DDR4_DQ13	C8	DQU5	U101
AN31	DDR4_DQ14	D3	DQU6	U101
AM30	DDR4_DQ15	D7	DQU7	U101
AF25	DDR4_DQ16	G2	DQL0	U99
AG25	DDR4_DQ17	F7	DQL1	U99
AG26	DDR4_DQ18	H3	DQL2	U99
AJ25	DDR4_DQ19	H7	DQL3	U99
AG24	DDR4_DQ20	H2	DQL4	U99
AK25	DDR4_DQ21	H8	DQL5	U99
AJ24	DDR4_DQ22	J3	DQL6	U99
AK24	DDR4_DQ23	J7	DQL7	U99
AH28	DDR4_DQ24	A3	DQU0	U99
AH27	DDR4_DQ25	B8	DQU1	U99
AJ27	DDR4_DQ26	C3	DQU2	U99
AK27	DDR4_DQ27	C7	DQU3	U99
AL26	DDR4_DQ28	C2	DQU4	U99
AL27	DDR4_DQ29	C8	DQU5	U99
AH29	DDR4_DQ30	D3	DQU6	U99
AL28	DDR4_DQ31	D7	DQU7	U99
AB29	DDR4_DQ32	G2	DQL0	U100
AB30	DDR4_DQ33	F7	DQL1	U100
AC29	DDR4_DQ34	H3	DQL2	U100
AD32	DDR4_DQ35	H7	DQL3	U100
AC31	DDR4_DQ36	H2	DQL4	U100
AE30	DDR4_DQ37	H8	DQL5	U100
AC28	DDR4_DQ38	J3	DQL6	U100
AE29	DDR4_DQ39	J7	DQL7	U100
AC27	DDR4_DQ40	A3	DQU0	U100
AA27	DDR4_DQ41	B8	DQU1	U100
AA28	DDR4_DQ42	C3	DQU2	U100