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ZCU106 Evaluation Board

User Guide

UG1244 (v1.0) March 28, 2018

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/28/2018	1.0	Initial Xilinx release.

Table of Contents

Appendix D: Additional Resources and Legal Notices

Introduction

Overview

The ZCU106 is a general purpose evaluation board for rapid-prototyping based on the ZU7EV silicon part and package in the 16 nm FinFET Zynq® UltraScale+™ MPSoC. The ZU7EV device integrates a quad core ARM® Cortex™-A53 processing system (PS) and a dual core ARM Cortex-R5 real-time processor, which provides application developers an unprecedented level of heterogeneous multiprocessing. The ZCU106 evaluation board provides a flexible prototyping platform with high-speed DDR4 memory interfaces, FMC expansion ports, multi-gigabit per second serial transceivers, video codec unit (VCU), several peripheral interfaces, and FPGA fabric for customized designs.

Additional Resources

See Appendix D, Additional Resources and Legal Notices for references to documents, files, and resources relevant to the ZCU106 evaluation board.

Block Diagram

The ZCU106 board block diagram is shown in Figure 1-1.

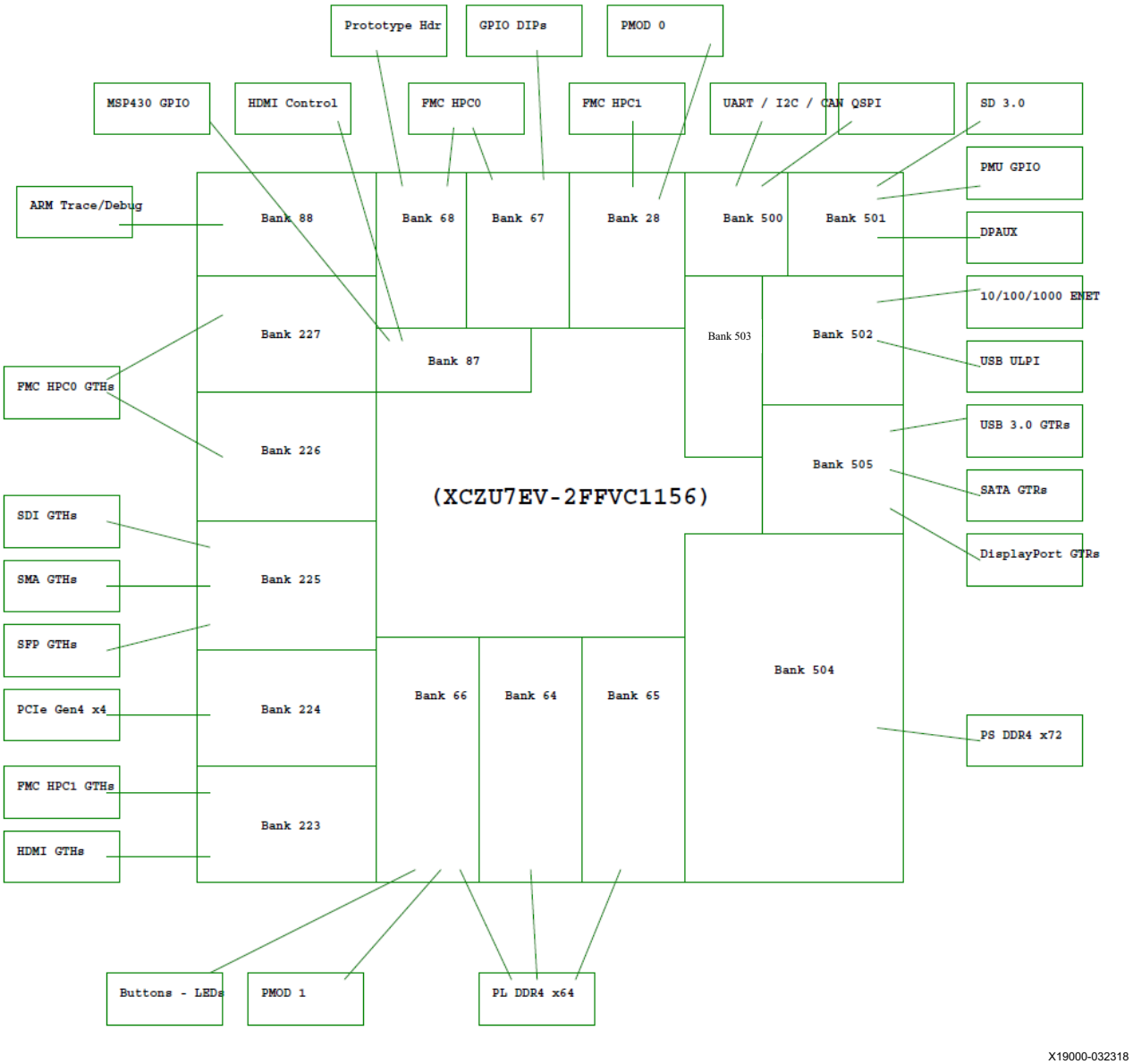

Figure 1-1: **ZCU106 Evaluation Board Block Diagram**

Board Features

The ZCU106 evaluation board features are listed here. Detailed information for each feature is provided in Component Descriptions in Chapter 3.

- XCZU7EV-2, FFVC1156 package
- PL V_{CCINT} for range in data sheet
- Form factor for PCIe® Gen[1-3]x4 endpoint (PL GTH transceiver), Micro-ATX chassis footprint
- Configuration from Quad SPI
- Configuration from SD card
- Configuration over JTAG with platform cable USB header
- Configuration over JTAG with ARM 20-pin header
- Configuration over USB-to-JTAG bridge
- Clocks
  - USER_MGT_SI570
  - PL_74.25M, PL_125M, PL_300M
  - USER_SMA_MGT
  - GTR_DP, GTR_USB3, GTR_SATA
  - PS_REF_CLK
- PS DDR4 72-bit SODIMM (includes ECC)
- PL DDR4 64-bit component (4x16-bit)
- PS-GTR assignment
  - DisplayPort (two GTRs)
  - USB3 (one GTR)
  - SATA (one GTR)
- PL GTH transceiver assignment (20 total)
  - High-definition multimedia interface (HDMI®) (three GTH transceivers)
  - FMC HPC1 DP (one GTH transceiver)
  - PCIe (four GTH transceivers)
  - SDI (one GTH transceiver)
  - SMA (one GTH transceiver)

    - SFP+ (two GTH transceivers)
    - FMC HPC0 DP (eight GTH transceivers)
- PL FMC HPC0 connectivity - full LA bus
- PL FMC HPC1 connectivity - partial LA bus
- PS MIO: dual Quad SPI
- PS MIO: two channels of quad-UART bridge
- PS MIO: CAN
- PS MIO: I2C shared across PS and PL
- PS MIO: SD
- PS MIO: DisplayPort
- PS MIO: system controller I/F
- PS MIO: Ethernet
- PS MIO: USB3
- PS-side user LED (one)
- PS-side user pushbutton (one)
- PL-side user LEDs (eight)
- PL-side user DIP switch (8-position)
- PL-side user pushbuttons (five)
- PL-side CPU reset pushbutton
- PL-side PMOD headers
- PL-side bank 0 PROG_B pushbutton
- Security - PSBATT button battery backup
- SYSMON (previously XADC), prototype header
- Operational switches (power on/off, PROG_B, boot mode DIP switch)
- Operational status LEDs (power status, INIT, DONE, PG, JTAG status, DDR power good)
- Power management

The ZCU106 provides designers a rapid prototyping platform using the XCZU7EV-2FFVC1156 device. The ZU7EV contains many PS hard block peripherals exposed through the multi-use I/O (MIO) interface and several FPGA programmable logic (PL), high-density (HD), and high-performance (HP) banks. Table 1-1 lists a summary of the resources available within the ZU7EV. A feature set overview, description, and ordering information is provided in the *Zynq UltraScale+ MPSoC Data Sheet: Overview* (DS891) [Ref 1].

Table 1-1: **Zynq UltraScale+ MPSoC ZU7EV Features and Resources**

Feature	Resource Count
HD banks	Two banks, total of 48 pins
HP banks	Six banks, total of 312 pins
MIO banks	Three banks, total of 78 pins
PS-GTR transceivers (6 Gb/s)	Four PS-GTR transceivers
GTH transceivers (16.3 Gb/s)	20 GTH transceivers
VCU	One
PCIe hard block Gen1/2/3/4 x4	Two
Logic cells	504 K
CLB flip-flops	460.8 K
Distributed RAM	6.2 Mb
Total block RAM	11 Mb
UltraRAM	27 Mb
DSP slices	1728

Board Specifications

Dimensions

Height: 7.323 inch (18.60 cm)

Length: 9.5 inch (24.13 cm)

Thickness: 0.062 inch ±0.005 inch (0.157 cm ±0.0127 cm)

Note: A 3D model of this board is not available.

IMPORTANT: *The ZCU106 board height exceeds the standard 4.376 inch (11.15 cm) height of a PCI Express® card.*

See ZCU106 board documentation for XDC listing, schematics, layout files, board outline drawings, etc.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Board Setup and Configuration

Board Component Location

Figure 2-1 shows the ZCU106 board component locations. Each numbered component shown in the figure is keyed to Table 2-1. Table 2-1 identifies the components, references the respective schematic (0381770) page numbers, and links to a detailed functional description of the components and board features in Chapter 3.

IMPORTANT: *Figure 2-1 is for visual reference only and might not reflect the current revision of the board.*

IMPORTANT: *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific ZCU106 version of interest for such details.*

CAUTION! *The ZCU106 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.*

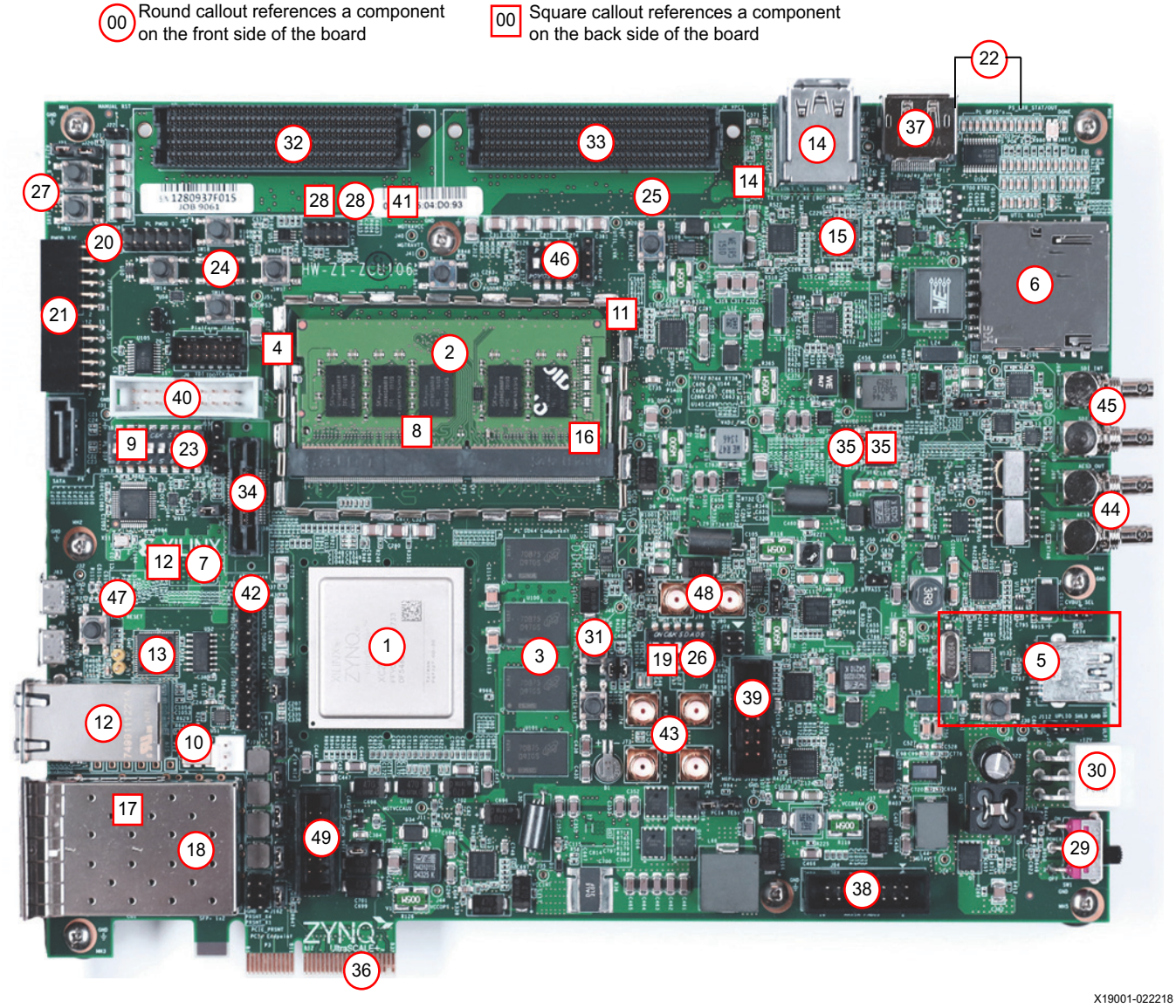

Figure 2-1: **ZCU106 Evaluation Board Components**

Table 2-1: **ZCU106 Board Component Locations**

Callout Number	Ref. Des.	Feature ([B] = bottom of board)	Notes	Schematic Page
1	U1	Zynq UltraScale+ XCZU7EV MPSoC, GTH Transceivers, PS GTR Transceivers	XCZU7EV-2FFVC1156	
2	J1	PS-Side: DDR4 SODIMM Socket	LOTESADDR0067-P001A/KINGSTON KVR21SE15S8/4	24
3	U2, U99-U101	DDR4 Component Memory, (4 Gb)	Micron MT40A256M16GE-075E	26-29
4	U119, U120	Quad SPI Flash Memory (MIO 0–12) [B]	Micron MT25QU512ABB8ESF-0SIT	53
5	U116, J96	USB 3.0 Transceiver and USB 2.0 ULPI PHY (USB 3.0 A connector)	SMSC USB3320-EZK, KYCON KMMX-AB10-SMT1SB30TR	58
6	J100	SD Card Interface	Hirose DMIAA-SF-PET(21)	54
7	U152, J2	Programmable Logic JTAG Programming Options	FTDI FT232HL-REEL, Hirose ZX62D-AB-5P8	22
8	U69	SI5341B 10 Independent Output Any-Frequency Clock Generator [B]	Silicon Labs SI5341B-B05071-GM	44
9	U42	Programmable User Clock [B]	Silicon Labs SI570BAB001614DG	45
10	U56	Programmable User MGT Clock, Cooling Fan Connector	Silicon Labs SI570BAB000544DG	45
11	U20	SFP/SFP+ Clock Recovery [B]	Silicon Labs SI5328B-C-GMR	46
12	U98, P12	GEM3 Ethernet (MIO 64-77), 10/100/1000 MHz Tri-Speed Ethernet PHY	TI DP83867IRPAP, Halo HFJ11-1G01E-L12RL	59
13	U40, J83	CP2108 USB UART Interface	Silicon Labs CP2108-B02-GM, Hirose ZX62D-AB-5P8	47
14	U94, P7	HDMI Video Output [B]	TI SN65DP159RGZ, TE Connectivity 1888811-1	40
15	U19, P7	HDMI Video Output	TI TMDS181IRGZT, TE Connectivity 1888811-1	41
16	U60, U61, U97	I2C0 (MIO 14-15), I2C0 bus switch and two expanders [B]	TI PCA9544ARGYR, Two each TI TCA6416APWR	64
17	U34, U135	I2C1 (MIO 16-17), I2C1 bus switches [B]	Two each TI TCA9548APWR	65
18	P1, P2	SFP/SFP+ Connectors	Molex 74441-0010	38-39
19	U41	TI MSP430 System Controller [B]	TI MSP430F5342	43
20	J87	User PMOD GPIO Headers	SULLINS PBC36DAAN	62
21	J160, J55	User PMOD GPIO Headers	SULLINS PPPC062LJBN-RC	56
22	DS37-DS44	User I/O, Power and Status LEDs	GPIO LEDs, GREEN 0603	60
23	SW13	User I/O DIP switch	C&K SDA08H1SBD	60

Table 2-1: **ZCU106 Board Component Locations *(Cont'd)***

Callout Number	Ref. Des.	Feature ([B] = bottom of board)	Notes	Schematic Page
24	SW14-SW18	User I/O pushbuttons	E-switch TL3301EP100QG placed in N,S,W,E,C pattern	60
25	SW20	User I/O reset pushbutton switch	E-switch TL3301EP100QG	60
26	SW8	Switches system controller DIP	5-pole C&K SDA05H1SBD	43
27	SW3, SW4	System Reset Pushbuttons	E-switch TL3301EP100QG	12
28	U122, J98	CAN1 (MIO 24-25) [B], 2X4 male header	TI SN65HVD232, SULLINS PBC36DAAN	57
29	SW1	Power On/Off Slide Switch	C&K 1201M2S3AQE2	66
30	J52	Power On/Off Slide Switch	MOLEX 39-30-1060	66
31	SW5	Program_B Pushbutton	E-switch TL3301EP100QG	12
32	J5	FPGA Mezzanine Card Interface, FMC HPC0 Connector J5	Samtec ASP_134486_01	30-33
33	J4	FPGA Mezzanine Card Interface, FMC HPC1 Connector J4	Samtec ASP_134486_01	34-37
34	P6	EMIO ARM Trace Port	MICTOR 2-5767004-2	61
35	–	Board Power System	Maxim regulators	67-92
36	P3	PCI Express Endpoint Connectivity	FCI 10061913-101CLF	48
37	P11	DisplayPort DPAUX (MIO 27-30)	MOLEX 0472720001	51-52
38	J84	Monitoring Voltage and Current	ASSMANN AWHW16G-0202-T-R	64
39	J92	Programmable Logic JTAG Programming Options	TYCO 5103308-2	43
40	J6	Programmable Logic JTAG Programming Options	ASSMANN AWHW20G-0202-T-R	23
41	U108	HDMI Clock Recovery [B]	Silicon Labs SI5324C-C-GMR	42
42	J3	Prototype Header	SULLINS PBC36DAAN	63
43	J74/J73, J72/J42	SMA, MGTH interface RX, TX SMA connectors	ROSENBERGER 32K10K-400L5	45
44	J69, J70	AES3 Audio	Samtec HDBNC–J–P–GN–RA–BH2	50
45	J10, J68	SDI Video	Samtec HDBNC–J–P–GN–RA–BH2	49
46	SW6	Switches MPSoC PS mode DIP	4-pole C&K SDA04H1SBD	12
47	SW9	Ethernet PHY Reset	E-switch TL3301EP100QG	59
48	J79/J80	User SMA MGT Clock	ROSENBERGER 32K10K-400L5	45
49	J93	SYSMON 2X6 vertical male pin header	SULLINS PBC36DAAN	3

Default Jumper and Switch Settings

Figure 2-2 shows the ZCU106 board jumper header and DIP switch locations. Each numbered component shown in the figure is keyed to Table 2-2 or Table 2-3 (for default switch settings). Both tables reference the respective schematic (0381770) page numbers.

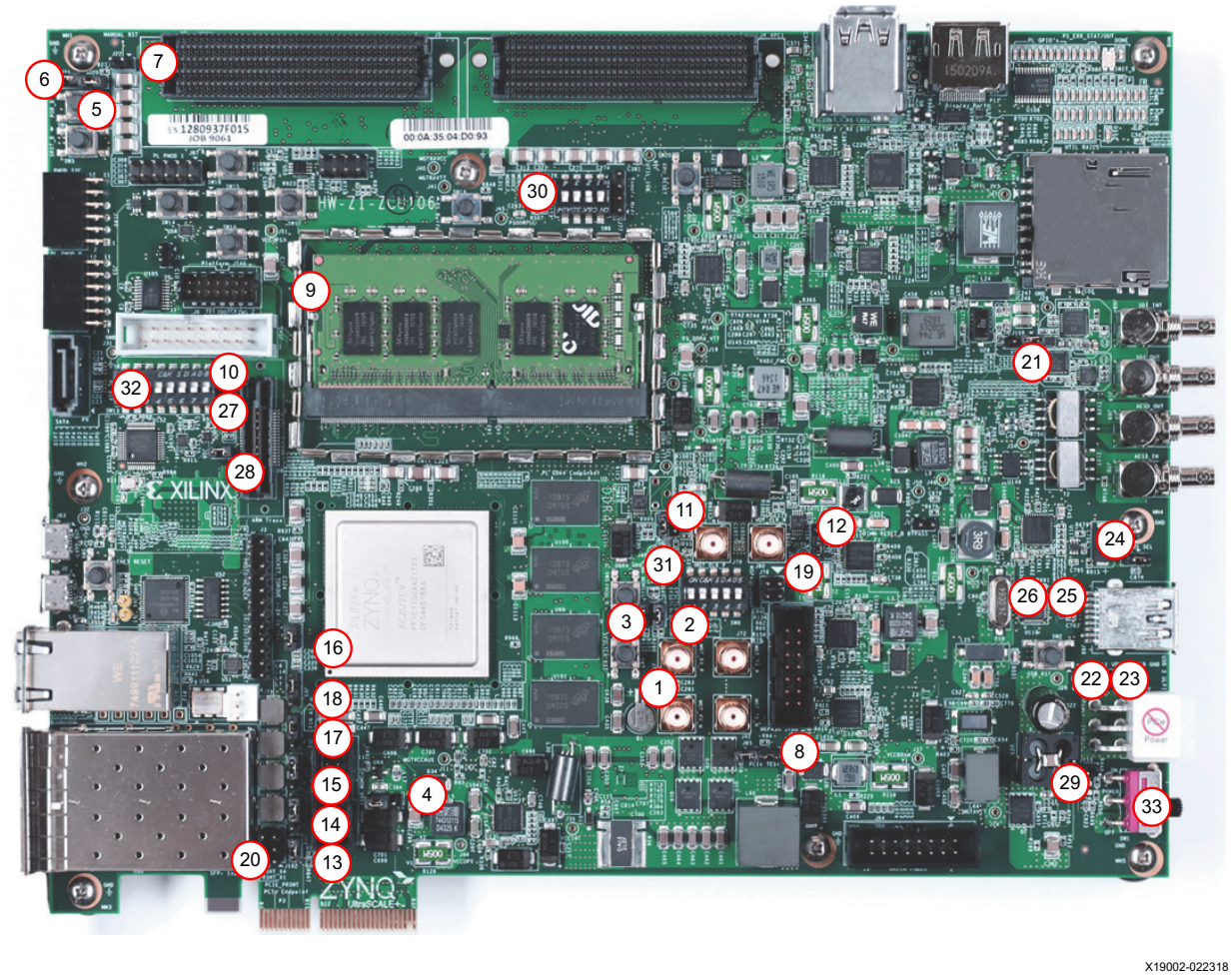

Figure 2-2: **Board Jumper Header and DIP Switch Locations**

Jumpers

Table 2-2: **Default Jumper Settings**

Number	Ref. Des.	Function	Default	Schematic Page
1	J85	POR_OVERRIDE • 1-2: Enable • 2-3: Disable	2-3	3
2	J12	SYSMON I2C address • Open: SYSMON_VP_R floating • 1-2: SYSMON_VP_P pulled down	1-2	3
3	J13	SYSMON I2C address • Open: SYSMON_VN_R floating • 1-2: SYSMON_VP_N pulled down	1-2	3
4	J90	SYSMON VREFP • 1-2:1.25V VREFP connected to FPGA • 2-3: VREFP connected to GND	1-2	3
5	J20	Reset sequencer PS_POR_B • Open: Sequencer does not control PS_POR_B • 1-2: Sequencer can control PS_POR_B	1-2	12
6	J21	Reset sequencer PS_SRST_B • Open: Sequencer does not control PS_SRST_B • 1-2: Sequencer can control PS_SRST_B	1-2	12
7	J22	Reset sequencer inhibit • Open: Sequencer normal operation • 1-2: Sequencer inhibit (resets stay asserted)	Open	12
8	J75	VCCINT_VCU power • Open: VCCINT_VCU not powered • 1-2, 3-4, 5-6: VCCINT_VCU powered	1-2 3-4 5-6	16
9	J14	ARM® debug VTREF • Open: VTREF floating • 1-2: VTREF = VCCOPS3 (1.8V)	1-2	22
10	J15	ARM debug VSUPPLY • Open: VSUPPLY floating • 1-2: VSUPPLY = VCCOPS3 (1.8V)	Open	22
11	J56	VCCO_PSDDR_504 select • 1-2: Switched DDR4 VDDQ • 3-4: Direct DDR4 VDDQ	1-2	24
12	J159	DDR4 reset suspend enable • 1-2: Suspend disabled (gate bypass) • 2-3: Suspend enabled	1-2	24

Table 2-2: **Default Jumper Settings *(Cont'd)***

Number	Ref. Des.	Function	Default	Schematic Page
13	J16	SFP0 enable	1-2	37
14	J62	SFP0 TX bandwidth • 1-2: Full bandwidth • 2-3: Low bandwidth	2-3	37
15	J63	SFP0 TX bandwidth • 1-2: Full bandwidth • 2-3: Low bandwidth	2-3	37
16	J17	SFP1 enable	1-2	38
17	J64	SFP1 TX bandwidth • 1-2: Full bandwidth • 2-3: Low bandwidth	2-3	38
18	J65	SFP1 TX bandwidth • 1-2: Full bandwidth • 2-3: Low bandwidth	2-3	38
19	J76	MSP430 programming • 1-2: Reset to GPIO • 3-4: Test to GPIO	Open	42
20	J162	PCIe PRSNT select • 1-2: x1 • 3-4: x4 • 5-6: GND • Open: card defined	Open	47
21	J108	SD level shifter internal reference • 1-2: 3.3V reference • 2-3: GND	1-2	53
22	J110	CVBUS select • 1-2: Device or OTG mode • 2-3: Host mode	1-2	57
23	J109	ID select • 1-2: Connector ID • 2-3: VDD33 ID	2-3	57
24	J112	Shield GND select • 1-2: Capacitor • 2-3: GND	1-2	57
25	J7	Device or host select • 1-2: Host/OTG • Open: Device	Open	57

Table 2-2: **Default Jumper Settings *(Cont'd)***

Number	Ref. Des.	Function	Default	Schematic Page
26	J113	Device/host or OTG select • 1-2: Device or host • 2-3: OTG	1-2	57
27	J88	ARM trace VTREF • 1-2: 3.3V • Open: 0V	Open	60
28	J38	ARM trace power • 1-2: 3.3V • Open: 0V	1-2	60
29	J153	Power inhibit • Open: Rails power on normally • 1-2: All rails (except UTIL) OFF	1-2	65

Switches

Table 2-3: **Default Switch Settings**

Number	Ref. Des.	Function	Default	Schematic Page
30	SW6 ***Note:*** For this DIP switch, in relation to the arrow, moving the switch toward the label ON is a 0. DIP switch labels 1 through 4 are equivalent to mode pins 0 through 3.	Switch PS_MODE select		12
		(ON = pull down, OFF = pull up)		
		1: PS_MODE0	On	
		2: PS_MODE1	On	
		3: PS_MODE2	On	
		4: PS_MODE3	On	
31	SW8 ***Note:*** For this DIP switch, in relation to the arrow, moving the switch toward the label ON is a 0. 1 through 5 are tied to MSP430 U41 GPIO[1:5].	MSP430 GPIO		42
		1: SW0	Off	
		2: SW1	Off	
		3: SW2	Off	
		4: SW3	Off	
		5: SW4	Off	
32	SW13	GPIO	All Off	59
33	SW1	Main power switch	Off	65

Installing the ZCU106 Board in a PC Chassis

Installation of the ZCU106 board inside a computer chassis is required when developing or testing PCI Express® functionality. When the ZCU106 board is installed in the PCIe® slot, power is provided from the ATX power supply 4-pin peripheral connector through the ATX adapter cable (Figure 2-3), which is plugged into J52 on the ZCU106 board. The Xilinx® part number for this cable is 2600304. See [Ref 25] for ordering information.

Figure 2-3: **ATX Power Supply Adapter Cable**

To install the ZCU106 board in a PC chassis:

1. On the ZCU106 board, remove the seven screws retaining the six rubber feet with their standoffs, and the PCIe bracket. Reinstall the PCIe bracket using two of the previously removed screws.
2. Power down the host computer and remove the power cord from the PC.
3. Open the PC chassis following the instructions provided with the PC.
4. Select a vacant PCIe expansion slot and remove the expansion cover (at the back of the chassis) by removing the screws on the top and bottom of the cover.

IMPORTANT: *The ZCU106 board height exceeds the standard PCIe board dimension, so the PC chassis top cover should remain off while using the ZCU106.*

5. Plug the ZCU106 board into an open PCIe expansion slot.
6. Install the top mounting bracket screw into the PC expansion cover retainer bracket to secure the ZCU106 board in its slot.
7. Connect the ATX power supply to the ZCU106 board using the ATX power supply adapter cable shown in Figure 2-3.
   a. Plug the 6-pin 2 x 3 Molex connector on the adapter cable into J52 on the ZCU106 board.
   b. Plug the 4-pin 1 x 4 peripheral power connector from the ATX power supply into the 4-pin adapter cable connector.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into the ZCU106 board power connector J52. The ATX 6-pin connector has a different pin out than J52. Connecting an ATX 6-pin connector into J52 damages the ZCU106 evaluation board and voids the board warranty.*

8. Slide the ZCU106 board power switch SW1 to the ON position. The PC can now be powered on.

MPSoC Device Configuration

Zynq UltraScale+ XCZU7EV MPSoC devices use a multi-stage boot process as described in the "Boot and Configuration" chapter of the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2]. Switch SW6 configuration option settings are listed in Table 2-4.

Table 2-4: **Switch SW6 Configuration Option Settings**

Boot Mode	Mode Pins [3:0]	Mode SW6 [4:1]
JTAG	0000	ON,ON,ON,ON
QSPI32	0010(1)	ON,ON,OFF,ON
SD	1110	OFF,OFF,OFF,ON

Notes:

1. Default switch setting.
2. For DIP SW6, in relation to the arrow, moving the switch toward the label ON is a 0. DIP switch labels 1 through 4 are equivalent to mode pins 0 through 3.

JTAG

Vivado®, SDK, or third-party tools can establish a JTAG connection to the Zynq UltraScale+ MPSoC device through one of these provided JTAG interfaces:

- Xilinx platform USB or cable PC4 connector (J8)
- ARM 20-pin JTAG connector (J6)
- FTDI FT232HL USB-to-JTAG bridge U152 with micro-USB connector (J2)

Quad SPI

To boot from the dual Quad SPI nonvolatile configuration memory:

1. Store a valid Zynq UltraScale+ MPSoC boot image in the Quad SPI flash devices connected to the MIO Quad SPI interface.
2. Set the boot mode pins SW6 [3:0] PS_MODE[3:0] as indicated in Table 2-4 for Quad SPI32.
3. Either power-cycle or press the power-on reset (POR) pushbutton. SW6 is callout 46 in Figure 2-1.

SD

To boot from an SD card:

1. Store a valid Zynq UltraScale+ MPSoC boot image file on to an SD card (plugged into SD socket J100) connected to the MIO SD interface.
2. Set the boot mode pins SW6 [3:0] PS_MODE[3:0] as indicated in Table 2-4 for SD.
3. Either power-cycle or press the power-on reset (POR) pushbutton. SW6 is callout 46 in Figure 2-1.

See the *Zynq UltraScale+ MPSoC Technical Reference Manual* (UG1085) [Ref 2] for more information about Zynq UltraScale+ MPSoC configuration options.

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. Table 2-1, page 14 identifies the components, references the respective schematic page numbers, and links to the corresponding detailed functional description in this chapter. Component locations are shown in Table 2-1, page 14.

Component Descriptions

Zynq UltraScale+ XCZU7EV MPSoC

[Figure 2-1, callout 1]

The ZCU106 board is populated with the Zynq UltraScale+ XCZU7EV-2FFVC1156 MPSoC, which combines a powerful processing system (PS) and programmable logic (PL) in the same device. The PS in a Zynq UltraScale+ MPSoC features the ARM® flagship Cortex®-A53 64-bit quad-core processor and Cortex-R5 dual-core real-time processor.

Production ZCU106 evaluation boards will ship with -2 speed grade devices. Support of multiple speed grades requires voltage adjustments.

The V_{CCINT} supplies are user adjustable via the PMBus with the voltage ranges listed in Table 3-1 to support multiple Zynq UltraScale+ MPSoC speed grades.

Table 3-1: **Recommended Operating Conditions**

Symbol	Description	Min	Typ	Max	Units
Processing System					
$V_{CC\_PSINTFP}$	PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS full-power domain supply voltage.	0.873	0.900	0.927	V
$V_{CC\_PSINTLP}$	PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS low-power domain supply voltage.	0.873	0.900	0.927	V
Programmable Logic					
V_{CCINT}	PL internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE (V_{CCINT} = 0.72V) devices: PL internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: PL internal supply voltage.	0.873	0.900	0.927	V

The top-level block diagram is shown in Figure 3-1.

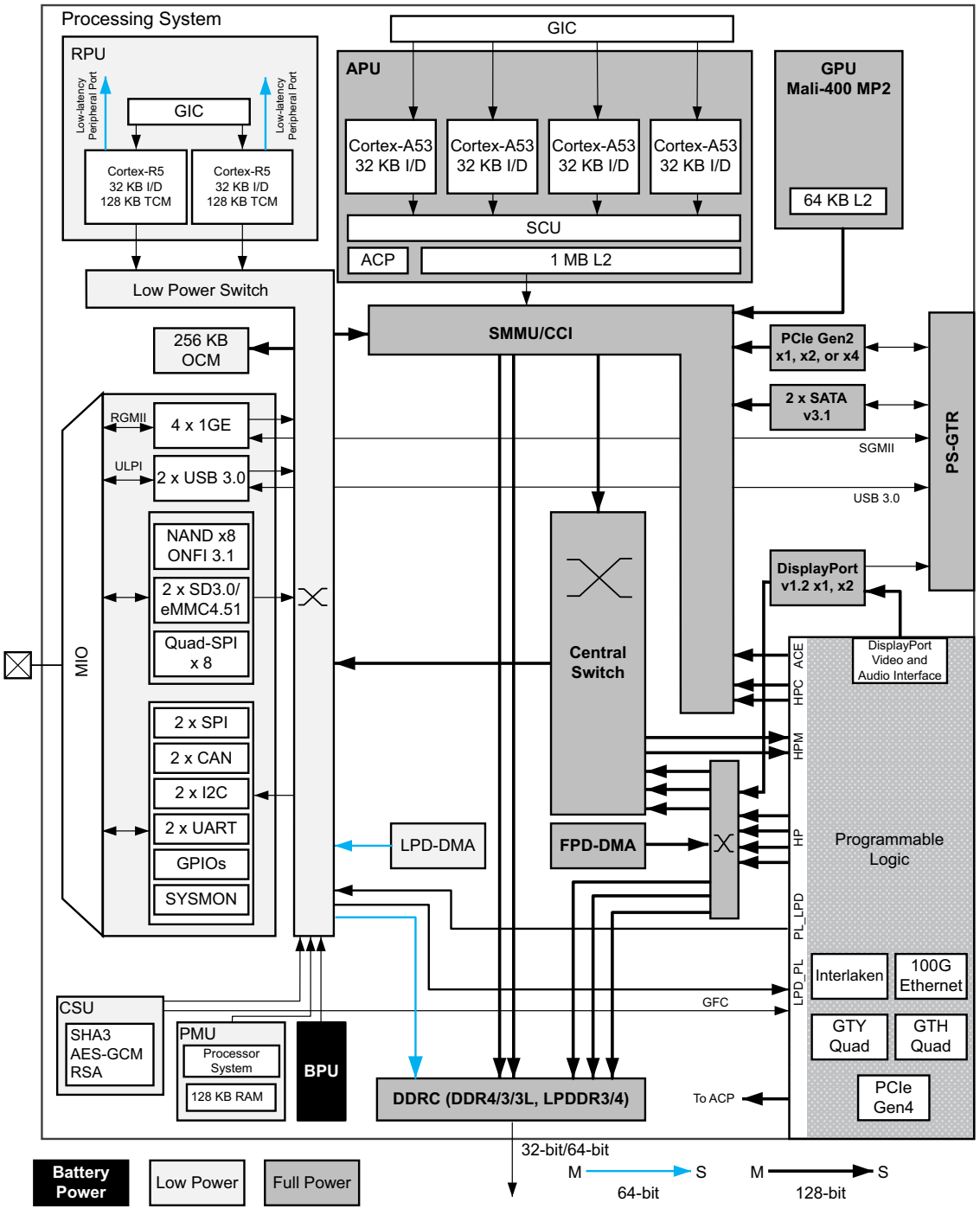

Figure 3-1: **Top-Level Block Diagram**