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ML630 Virtex-6 HXT FPGA Optical Transmission Network Evaluation Board

User Guide

UG828 (v1.0) September 28, 2011

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/28/11	1.0	Initial Xilinx release.

Table of Contents

About This Guide

This document describes the basic setup, features, and operation of the ML630 Virtex®-6 FPGA HXT Optical Transmission Network (OTN) evaluation board. The ML630 board provides the hardware environment for characterizing and evaluating the GTX and GTH transceivers available on the Virtex®-6 XC6VHX565T-2FFG1924C FPGA.

In this document Virtex-6 FPGA GTX transceiver is abbreviated as GTX transceiver. Similarly, Virtex-6 FPGA GTH transceiver is abbreviated as GTH transceiver.

Guide Contents

This user guide contains the following chapters and appendices:

- Chapter 1, ML630 Board Features and Operation, describes the components, features, and operation of the ML630 Virtex-6 HXT FPGA OTN evaluation board.
- Appendix A, Default Jumper Positions, lists the jumpers that must be installed on the board for proper operation.
- Appendix B, VITA 57.1 FMC HPC Connector Pinout, provides a pinout reference for the FPGA mezzanine card (FMC) connectors.
- Appendix C, ML630 Master UCF Listing for U1, provides a listing of the ML630 FPGA U1 user constraints file (UCF).
- Appendix D, ML630 Master UCF Listing for U2, provides a listing of the ML630 FPGA U2 user constraints file (UCF).
- Appendix E, ML630C Schematic Page List, provides a listing of schematic page numbers versus the detailed description callout numbers, for easy cross-referencing.
- Appendix F, Documents and Resources, lists documents relevant to Virtex®-6 devices, the ML630 Virtex-6 FPGA GTX Transceiver Characterization Board, and intellectual property.

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Command Line Tools User Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

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Chapter 1

ML630 Board Features and Operation

This chapter describes the components, features, and operation of the ML630 Virtex®-6 HXT FPGA Optical Transmission Network (OTN) evaluation board. The ML630 board provides the hardware environment for characterizing and evaluating the GTX and GTH transceivers available on the Virtex -6 XC6VHX565T-2FFG1924C FPGA.

ML630 Board Features

- Two Virtex-6 XC6VHX565T-2FFG1924C FPGAs
- On-board power regulators for all necessary voltages with power status LEDs
- All ML630 FPGA U1 and U2 I/O banks V_{CCO} voltage is 2.5V
- Two types of external power supply jacks (12V "brick" DIN4 type, PC ATX type)
- USB JTAG configuration port for use with USB A-to-Mini-B cable
- System ACE™ controller with companion CompactFlash socket
- General purpose pushbutton and DIP switches, LEDs, and test I/O header for each FPGA
- VGA 2X5 male debug header for each FPGA
- USB-to-UART bridge with USB Mini-B pcb connector for each FPGA
- Two VITA 57.1 FMC HPC connectors
- I^2C bus hosting EEPROM, clock sources and FMC connectors
- A separate SiTime fixed 200 MHz 2.5V LVDS oscillator wired to each FPGAs global clock inputs
- Eight pairs of differential clock input SMA connectors
- Six I^2C programmable Silicon Labs Si570 3.3V LVPECL 10 MHz to 810 MHz oscillators
- Two differential input 8X8 crosspoint switches providing 16 selectable differential clock sources
- Four sets of plug and receptacle FCI Airmax 120 pin connectors implementing the Interlaken interconnect protocol

The ML630 board block diagram is shown in Figure 1-1.

Caution! The ML630 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

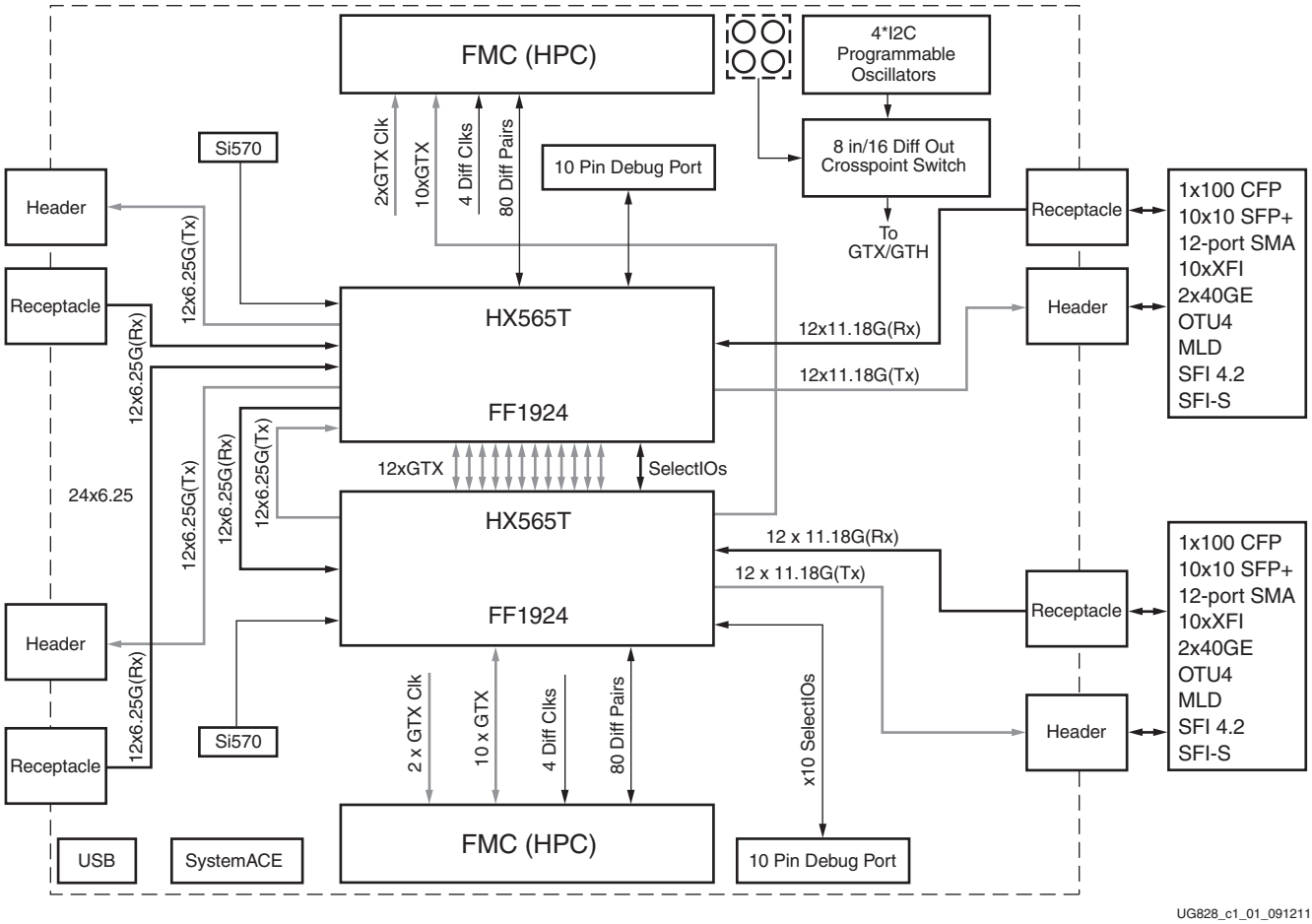

Figure 1-1: **ML630 Board Block Diagram**

Detailed Description

Note: This section of the user guide is intended to be read in conjunction with reference to the ML630 (pdf) Schematic 0381388. The ML630 board hosts a complicated clocking system and intricate FPGA-to-FPGA and Interlaken connector connectivity which the schematic helps clarify. Please refer to the schematic pages associated with the circuitry described in each section of this detailed description.

Figure 1-2 shows the ML630 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Note: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

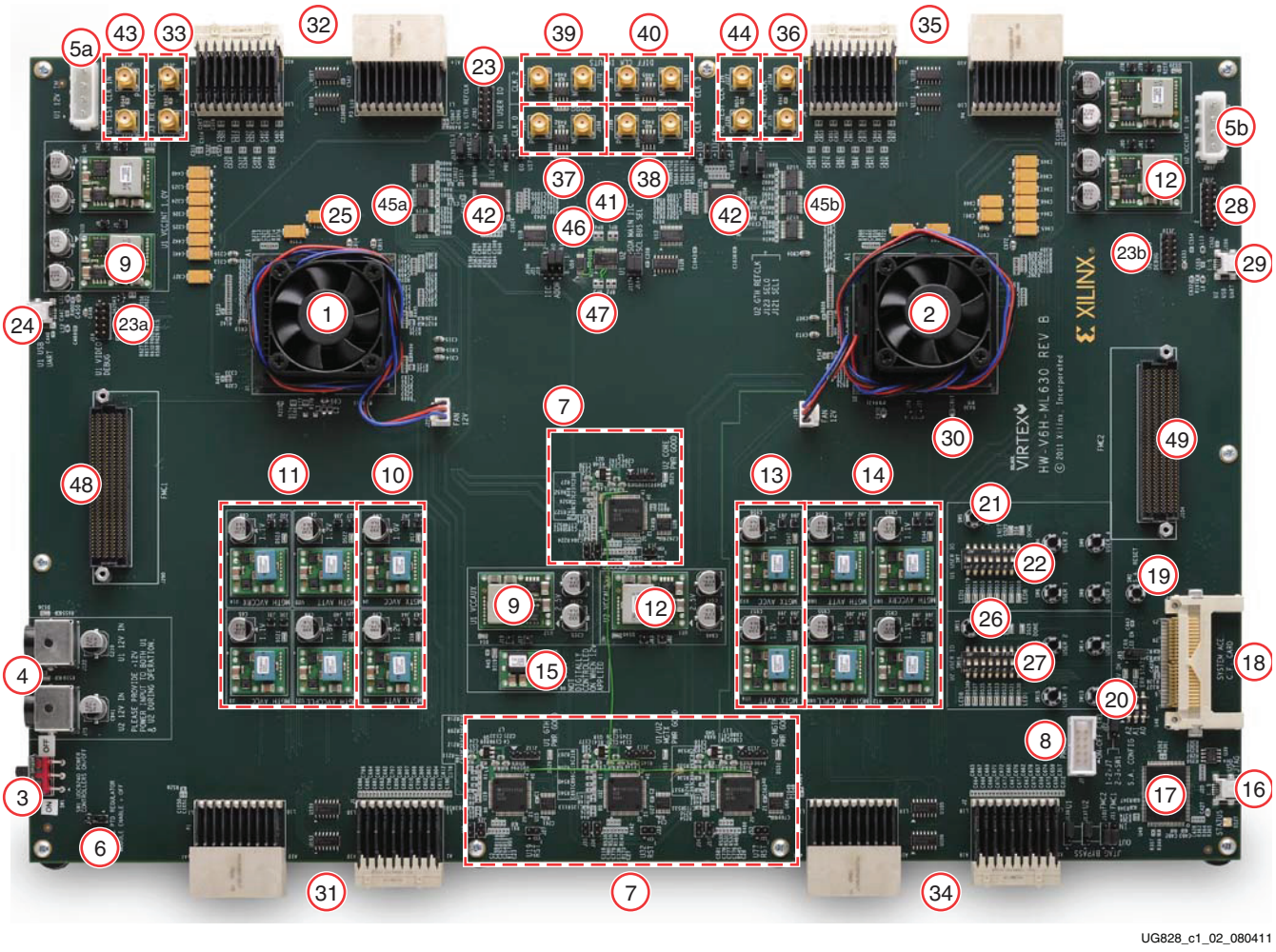

Figure 1-2: **Detailed Description of ML630 Board Components**

Virtex-6 HXT XC6VHX565T-2FFG1924 FPGA U1 and U2

1. FPGA U1
2. FPGA U2

ML630 12 VDC Power Input

3. Main power on-off "soft" slide switch (SW1)
4. U1/U2 12V DIN4 connectors (J122 and J75)
5. U1/U2 12V ATX connector (J141 and J102)

FPGA Power Inhibit Jumper

6. J289 regulator inhibit jumper

FPGA U1 and U2 Power System Controllers

7. U1 and U2 TI UCD9240 digital power controllers (U8, U19, U32 and U77)
8. PMBus connector (J7) for TI GPIO adapter (PMBus pod)

FPGA U1 Power Regulators

9. U1 V_{CCINT} (U10/U41) and V_{CCAUX} (U12) TI PTD08A020W regulators
10. U1 GTX (U4, U5) TI PTD08A101W regulators
11. U1 GTH (U3, U14, U21, U20) TI PTD08A010W and PTD08A006W regulators

FPGA U2 Power Regulators

12. U2 V_{CCINT} (U81/U82) and V_{CCAUX} (U83) TI PTD08A020W regulators
13. U2 GTX (U73, U74) TI PTD08A101W regulators
14. U2 GTH (U72, U67, U68, U69) TI PTD08A010W and PTD08A006W regulators

Board-wide 3.3V Regulator

15. TI PTH12000W 3.3V regulator (U6)

ML630 FPGA Configuration

16. USB JTAG Mini-B connector (J20)
17. Embedded JTAG (U48 top of board) and (U45 bottom of board) circuits
18. SystemACE CompactFlash (C.F.) Socket (U46 top of board), SystemACE IC (U47 bottom of board)
19. SystemACE reset pushbutton (SW2)
20. SystemACE C.F. image select DIP switch (SW3)

FPGA U1 Indicators and I/O

21. U1 PROG pushbutton (SW5), INIT LED (DS20) and DONE LED (DS6)
22. U1 User LEDs (DS10-DS17), User DIP switch (SW7) and user pushbutton switches (SW4, SW6, SW8, SW9)
23. 23a: U1 User GPIO 2X6 header (J285)
    23b: VGA video debug 2x5 header (J16)
24. U1 USB UART Mini-B connector (J54 top of board) and USB-to-UART bridge IC (U26 bottom of board)
25. U1 SiTime 200 MHz 2.5V LVDS fixed frequency oscillator (U22 bottom of board)

FPGA U2 Indicators and I/O

26. U2 PROG pushbutton (SW11), INIT LED (DS54) and DONE LED (DS29)
27. U2 User LEDs (DS30-DS38), User DIP switch (SW16) and user pushbutton switches (SW12-SW15)
28. U2 User GPIO 2X6 header (J103)
29. U2 USB UART Mini-B connector (J106) top of board) and USB-to-UART bridge IC (U26 bottom of board)
30. U2 SiTime 200 MHz 2.5V LVDS fixed frequency oscillator (U63 bottom of board)

FPGA U1 FCI Airmax Interlaken Connectors

31. P1, J1 FCI Airmax Interlaken plug and receptacle connectors

32. P3, J3 FCI Airmax Interlaken plug and receptacle connectors
33. J3 refclk (J132, J133) SMA connectors
34. P2, J2 FCI Airmax Interlaken plug and receptacle connectors

FPGA U2 FCI Airmax Interlaken Connectors

35. P4, J4 FCI Airmax Interlaken plug and receptacle connectors
36. J4 refclk (J134, J135) SMA connectors

FPGA U1 and FPGA U2 Clock Circuits

37. Differential clock input connectors CLK0 SMA (J167, J168) with 1-to-2 3.3V LVPECL buffer (U98)
38. Differential clock input connectors CLK1 SMA (J169,J170) with 1-to-2 3.3V LVPECL buffer (U99)
39. Differential clock input connectors CLK2 SMA (J171, J172) with 1-to-2 3.3V LVPECL buffer (U96)
40. Differential clock input connectors CLK3 SMA (J9, J10) with 1-to-2 3.3V LVPECL buffer (U97)
41. Four I^2C programmable Silicon Labs Si570 3.3V LVPECL 10 MHz-to-810 MHz oscillators (U43, U44, U51, U52) each with a 1-to-2 3.3V LVPECL buffer (U53, U54, U55, U56, bottom of board)
42. Two differential clock input-output 8x8 crosspoint switches (U57, U58)
43. FPGA U1 differential test clock input SMA connectors (J124, J125) with 1-to-6 3.3V LVDS buffer (U126)
44. FPGA U2 differential test clock input SMA connectors (J126, J127) with 1-to-6 3.3V LVDS buffer (U127)
45. Six dual 2-to-1 3.3V LVDS input, 3.3V LVPECL output differential clock multiplexers (U102, U115, U116, U120, U121, U122)
46. Two I^2C programmable Silicon Labs Si570 3.3V LVPECL 10 MHz-to-810 MHz oscillators, one for FPGA U1 (U64) and one for FPGA U2 (U65) (bottom of board), each with a 1-to-6 3.3V LVDS buffer (U13, U18), top of board)

ML630 I^2C Bus

47. I^2C Main Bus: M24C02 256x8 EEPROM (U59), TI PCA9548 (U31) 1-to-8 port I^2C expander (six ports wired to the Si570 oscillators, two ports wired to the 8x8 crosspoint switches); U1 I^2C: HPC FMC1 J290; U2 I^2C: HPC FMC2 J104

ML630 HPC FMC Connectors

48. FMC1 connector (J290)
49. FMC2 connector (J104)

Default Jumper Positions

A list of shunts and their required positions for normal board operation is provided in Appendix A, Default Jumper Positions.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for all power rails except the fixed 3.3V through Texas Instruments' Fusion Digital Power graphical user interface (GUI). All onboard TI power controllers are wired to the same PMBus. The PMBus connector, J7, is provided for use with the TI GPIO Interface Adapter (PMBus pod) and associated TI Fusion Digital Power GUI.

References

More information about the power system components used by the ML630 board is available from the Texas Instruments digital power website at:

http://www.ti.com/ww/en/analog/digital-power/index.html

FPGA U1 and U2

Figure 1-2 callouts [1, 2]

The ML630 board hosts two Virtex-6 XC6VHX565T-2FFG1924C FPGAs. This FPGA provides six four-quad GTH and twelve four-quad GTX high speed interfaces.

References

For more detailed information refer to:
http://www.xilinx.com/products/silicon-devices/fpga/virtex-6/hxt.htm

Board Power and Switch

Figure 1-2 callouts [3, 4, 5]

The ML630 board is powered through two 4-pin DIN right angle type connectors J122 and J75 using the two 12V 15A AC-to-DC adapters included with the board.

Power can also be provided through J141 and J102 ATX hard disk type 4-pin power connectors. The DIN4 J122 and ATX J141 connectors are wired in parallel, as are J75 and J102.

Note: Use of a switchable “power bar” (multiple outlet power strip) is recommended for the two ML630 AC adapters. The two adapters can then be turned on and off simultaneously via the power bar on-off switch.

> ***Caution!*** Only use two power supplies of the same type. Power the ML630 board through two connectors at the same time (J122 and J75 or J141 and J102, depending on power supply type). Do NOT apply power to all four power input connectors J122/J75 and J141/J102 at the same time. Doing so may damage the ML630 board and void the board warranty.

When the 12V AC adapters are plugged into the ML630 board and turned on via the multiple outlet AC power strip, 12 VDC is applied to the ML630 12V power planes, and green LED indicators (DS36 and DS49) adjacent to each DIN4 power connector illuminate.

The ML630 board U1 and U2 FPGA power regulators are turned on and off by the “soft” slide switch, SW1. When this switch is in the ON position, power is applied to the FPGAs and the green LEDs adjacent to each active regulator illuminate.

The FPGA U1 and part of FPGA U2 power system block diagram is shown in Figure 1-3. The circuit details may be found on the schematic pages 8 and 51 through 67 as noted in the various function blocks.

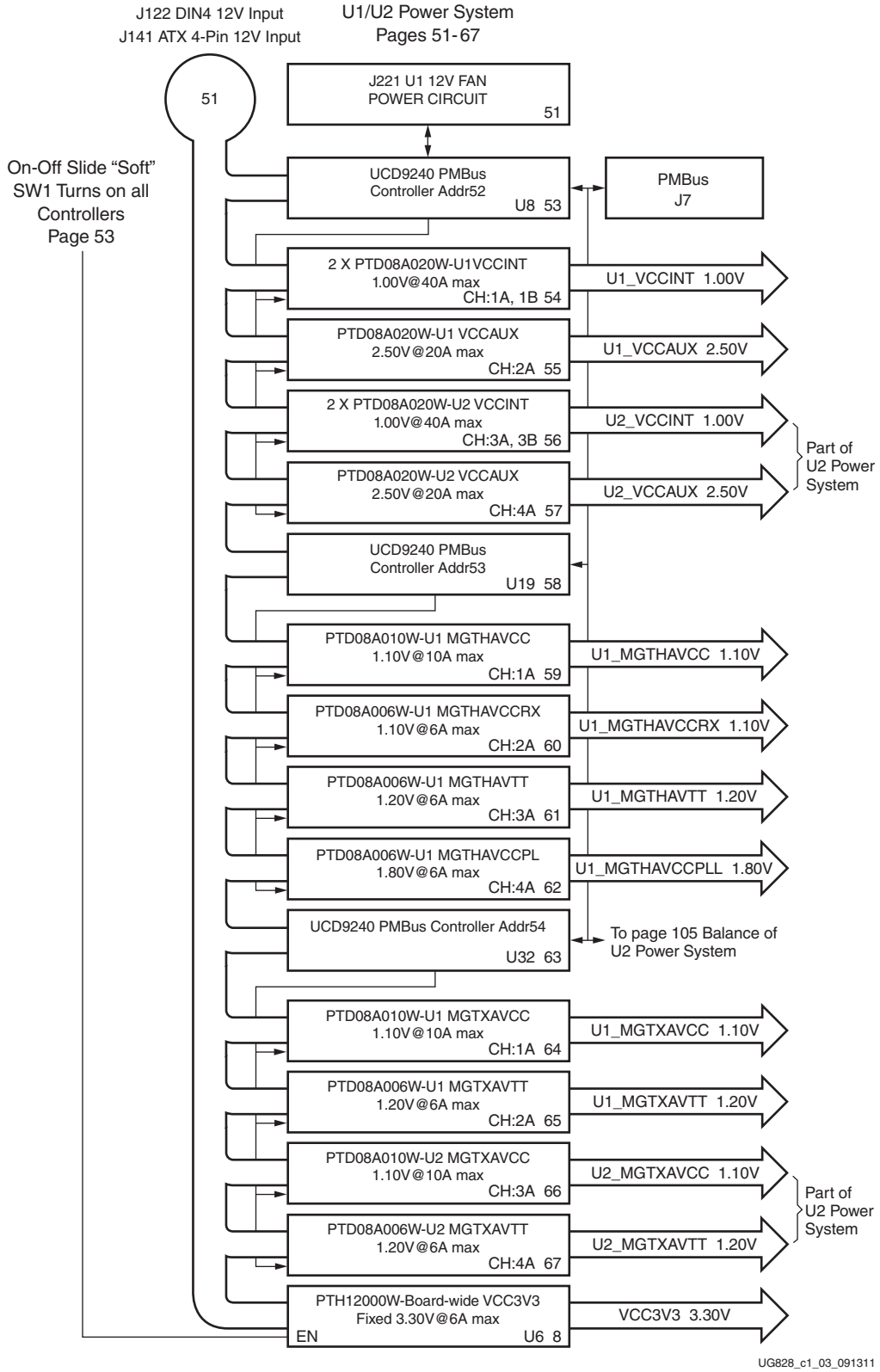

Figure 1-3: **ML630 Board FPGA U1 Power Block Diagram**

Part of the FPGA U2 power system block diagram is shown in, Figure 1-4. The circuit details may be found on the schematic, pages 103 through 109 as noted in the various function blocks.

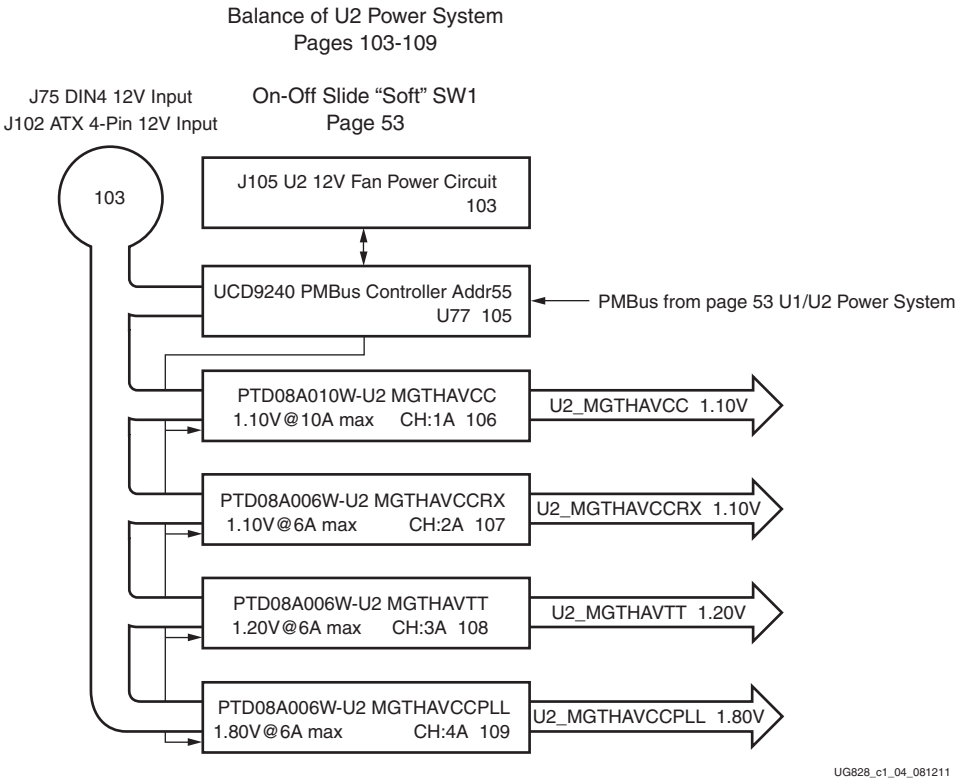

Figure 1-4: **ML630 Board FPGA U2 Power Block Diagram**

The ML630 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the U1 and U2 voltages listed in Table 1-1.

Table 1-1: **ML630 Onboard Power System Devices**

Device	Reference Designator	Description	Power Rail Net Name	Typical Voltage
U1 and U2 Core Voltage Controller and Regulators				
UCD9240PFC	U8	PMBus compliant digital PWM system controller (address = 52)		
PTD08A020W	U10	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 0f 2 Phases	U1_VCCINT	1.0V
PTD08A020W	U41	Adjustable switching regulator 20A, 0.6V to 3.6V, 2 0f 2 Phases	U1_VCCINT	1.0V
PTD08A020W	U12	Adjustable switching regulator 20A, 0.6V to 3.6V	U1_VCCAUX	2.5V
PTD08A020W	U81	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 0f 2 Phases	U2_VCCINT	1.0V
PTD08A020W	U82	Adjustable switching regulator 20A, 0.6V to 3.6V, 2 0f 2 Phases	U2_VCCINT	1.0V
PTD08A020W	U83	Adjustable switching regulator 20A, 0.6V to 3.6V	U2_VCCAUX	2.5V
U1 GTH Voltage Controller and Regulators				
UCD9240PFC	U19	PMBus compliant digital PWM system controller (address = 53)		
PTD08A010W	U3	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTHAVCC	1.1V
PTD08A006W	U14	Adjustable switching regulator 6A, 0.6V to 3.6V	U1_MGTXAVCCRX	1.1V
PTD08A006W	U20	Adjustable switching regulator 6A, 0.6V to 3.6V	U1_MGTHAVTT	1.2V
PTD08A006W	U21	Adjustable switching regulator 6A, 0.6V to 3.6V	U1_MGTXAVCCPLL	1.8V
U1 and U2 GTX Voltage Controller and Regulators				
UCD9240PFC	U32	PMBus compliant digital PWM system controller (address = 54)		
PTD08A010W	U4	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVCC	1.1V
PTD08A010W	U5	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVTT	1.2V
PTD08A010W	U73	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVCC	1.1V
PTD08A010W	U74	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVTT	1.2V
U2 GTH Voltage Controller and Regulators				
UCD9240PFC	U77	PMBus compliant digital PWM system controller (address = 55)		
PTD08A010W	U72	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTHAVCC	1.1V
PTD08A006W	U67	Adjustable switching regulator 6A, 0.6V to 3.6V	U2_MGTXAVCCRX	1.1V
PTD08A006W	U68	Adjustable switching regulator 6A, 0.6V to 3.6V	U2_MGTHAVTT	1.2V
PTD08A006W	U69	Adjustable switching regulator 6A, 0.6V to 3.6V	U2_MGTXAVCCPLL	1.8V
Auxiliary 3.3V Power				
PTH12000W	U6	Adjustable switching regulator 6A, 1.2 to 5.5V	VCC3V3	3.3V

Disabling FPGA Onboard Power

Figure 1-2 callout [6]

All TI controller PTD type voltage regulators are disabled by installing a jumper across pins 1–2 of header J289.

FPGA Configuration

Figure 1-2 callout [16, 17, 18]

The FPGA is configured in JTAG mode only using one of the following options:

- Embedded USB JTAG circuit (uses USB-A-to-Mini-B cable)
- System ACE controller (utilizing a CompactFlash card loaded with bit files)

The FPGA Embedded JTAG option is chosen by connecting a USB A-to-Mini-B cable to ML630 USB Mini-B connector J20. The USB A end of the cable plugs into the user's PC, which hosts the Xilinx FPGA configuration software tool (either ChipScope™ Pro or Impact) which is then used to configure the two ML630 FPGAs.

The FPGAs can also be configured through the System ACE controller by setting the 3-bit configuration address DIP switches (SW3) to select one of eight bitstreams stored on a CompactFlash memory card plugged into socket U46 (see Table 1-2, page 17).

Upon power-on, the System ACE controller checks for the presence of a flash card and loads the FPGA configuration files from it, if present.

The JTAG chain of the board is illustrated in Figure 1-5. Each component (except the System ACE IC) with a JTAG interface has a bypass jumper which permits the component to be in the chain or bypassed.

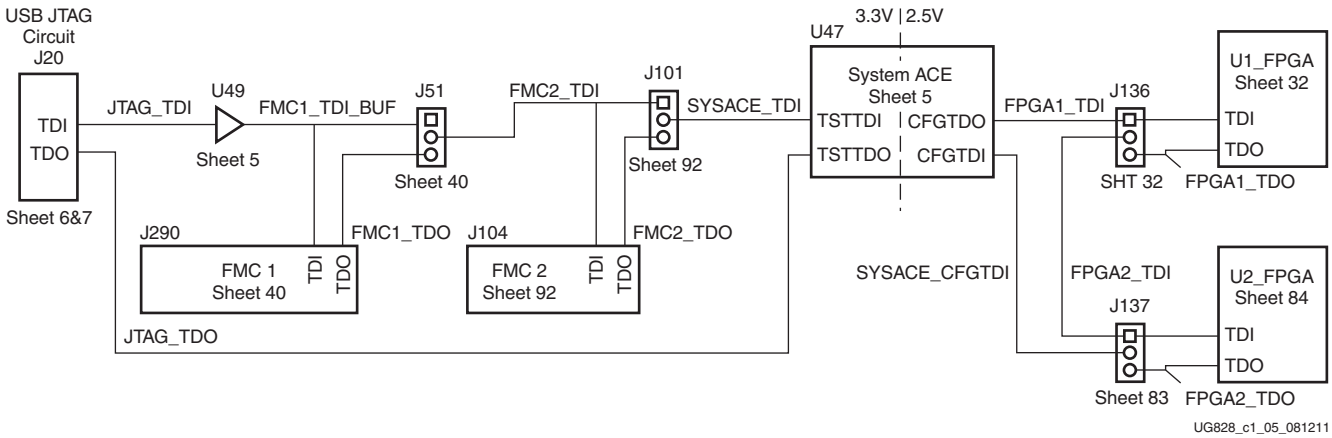

Figure 1-5: **ML630 JTAG Chain Diagram**

System ACE Controller

Figure 1-2 callout [18]

The onboard System ACE controller (U47) allows storage of multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGAs. The CompactFlash card plugs into the CompactFlash card socket (U46) located directly above the System ACE controller (which is on the bottom side of the board).

System ACE Controller Reset

Figure 1-2 callout [19]

Pressing pushbutton SW2 (RESET) resets the System ACE controller. Reset is an active-Low input.

Configuration Address DIP Switches

Figure 1-2 callout [20]

DIP switch SW3 selects one of the eight configuration bitstream addresses in the CompactFlash memory card. The switch settings for selecting each address are shown in Table 1-2.

Table 1-2: **System ACE SW3 DIP Switch Configuration**

Address	ADR2 (POS1)	ADR1 (POS2)	ADR0 (POS3)
0	O(1)	O	O
1	O	O	C(2)
2	O	C	O
3	O	C	C
4	C	O	O
5	C	O	C
6	C	C	O
7	C	C	C

Notes:

1. O indicates the open switch position (Logic 0).
2. C indicates the closed switch position (Logic 1).
3. The System ACE controller has internal pull-down resistors on its CFGADDR[2:0] pins.

References

More information on the System ACE controller is available in DS080, *System ACE CompactFlash Solution*.

FPGA U1 PROG Pushbutton, INIT LED and DONE LED

Figure 1-2 callout [21]

Pressing the U1 PROG push button (SW5) grounds the active-Low program pin of the FPGA. The INIT LED (DS20) lights during FPGA initialization. The DONE LED (DS56) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, the DONE LED lights indicating that the FPGA is successfully configured.

FPGA U1 User LEDs, DIP and Pushbutton Switches

Figure 1-2 callout [22]

DS10 through DS17 are eight active-High LEDs that are connected to user I/O pins on FPGA U1 as shown in Table 1-3. These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-3: **FPGA U1 User LEDs**

FPGA U1 Pin	Net Name	Reference Designator
K33	U1_USER_LED1	DS17
L33	U1_USER_LED2	DS16
A37	U1_USER_LED3	DS15
B37	U1_USER_LED4	DS14
B36	U1_USER_LED5	DS13
B35	U1_USER_LED6	DS12
A35	U1_USER_LED7	DS11
A34	U1_USER_LED8	DS10

User DIP Switches (Active High)

Figure 1-2 callout [22]

FPGA U1 DIP switch SW7 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-4. These switched signals can be used to set control bits or any other purpose determined by the user.

Table 1-4: **FPGA U1 User DIP Switches**

FPGA U1 Pin	Net Name	Reference Designator
J20	U1_USER_SW1	SW7
K21	U1_USER_SW2	
P21	U1_USER_SW3	
R21	U1_USER_SW4	
G20	U1_USER_SW5	
H21	U1_USER_SW6	
E20	U1_USER_SW7	
F20	U1_USER_SW8	

User Push Buttons (Active High)

Figure 1-2 callout [22]

SW4, SW6, SW8 and SW9 are active-High user pushbuttons that are connected to user I/O pins on FPGA U1 as shown in Table 1-5. These switches can be used for any purpose determined by the user.

Table 1-5: **FPGA U1 User Pushbuttons**

FPGA U1 Pin	Net Name	Reference Designator
H26	U1_USER_PB1	SW4
J26	U1_USER_PB2	SW6
N24	U1_USER_PB3	SW8
N23	U1_USER_PB4	SW9

FPGA U1 User GPIO Header

Figure 1-2 callout [23]

A standard 2 x 6, 100-mil pitch header (J285) brings out six FPGA I/Os for test purposes. Table 1-6 lists these pins. J285 odd pin numbers are wired to GND (ground).

Table 1-6: **FPGA U1 User GPIO Header J285**

FPGA U1 Pin	Net Name	J285 Pin
J35	U1_USER_IO_1	2
K35	U1_USER_IO_2	4
D35	U1_USER_IO_3	6
E35	U1_USER_IO_4	8
P35	U1_USER_IO_5	10
P34	U1_USER_IO_6	12

FPGA U1 USB to UART Bridge

Figure 1-2 callout [24]

Communications between the ML630 board FPGA U1 and a host computer are accomplished through a USB cable connected to J54. Control is provided by U26, a USB to UART bridge (Silicon Laboratories CP2103). Table 1-7 lists the pin assignments and signals for the USB connector J54.

Table 1-7: **: J54 USB Mini-B Connector Pin Assignments and Signals**

J54 Pin	Signal Name	Description
1	VBUS	+5V from host system
2	U1_USB_D_N	Bidirectional differential serial data (N-side)

Table 1-7: **: J54 USB Mini-B Connector Pin Assignments and Signals *(Cont'd)***

J54 Pin	Signal Name	Description
3	U1_USB_D_P	Bidirectional differential serial data (P-side)
4	ID	Not used

The CP2103 supports an I/O voltage range of 2.5V on the ML630 board. The connections between FPGA U1 and CP2103 should use the LVCMOS25 I/O standard. UART IP (for example, Xilinx® XPS UART Lite) must be implemented in the FPGA logic. FPGA U1 supports the USB to UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS)

Connections of these signals between the FPGA and the CP2103 at U26 are listed in Table 1-8.

Table 1-8: **FPGA U1 to U26 (CP2103 Bridge) Connections**

FPGA U1 Pin	FPGA Function	Net Name	U26 Pin	U26 Function
P11	RTS, output	U1_USB_CTS_I	22	CTS, input
P10	CTS, input	U1_USB_RTS_O	23	RTS, output
P10	TX, data out	U1_USB_RXD_I	24	RXD, data in
E10	RX, data in	U1_USB_TXD_O	25	TXD, data out

The bridge device also provides as many as four GPIO signals that can be defined by the user for status and control information (see Table 1-9).

Table 1-9: **FPGA U1 to U26 (CP2103 Bridge) User GPIO Connections**

FPGA U1 Pin	Net Name	U26 Pin
L10	U1_USB_GPIO_0	19
M11	U1_USB_GPIO_1	18
D10	U1_USB_GPIO_2	17
E11	U1_USB_GPIO_3	16

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB to UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTerminal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the ML630 board.

References

More information on the Silicon Labs CP2103 USB-to-UART bridge is available at: http://www.silabs.com/products/interface/usbtouart/Pages/default.aspx.

FPGA U1 200 MHz 2.5V LVDS Oscillator

Figure 1-2 callout [25]

The ML630 board has one SiTime 2.5V LVDS differential fixed 200 MHz oscillator per FPGA. Oscillator U22 (located on the bottom of the board) is connected to FPGA U1 as listed in Table 1-10.

Table 1-10: **FPGA U1 LVDS Oscillator U22 Global Clock Connections**

FPGA U1 Pin	Net Name	U22 Pin
J33	U1_LVDS_OSC_P	4
H33	U1_LVDS_OSC_N	5

References

More information on the SiTime SI9102AI oscillator is available at: http://www.sitime.com/products/differential-oscillators/sit9102.

FPGA U2 PROG Push Button, INIT LED and DONE LED

Figure 1-2 callout [26]

Pressing the U2 PROG pushbutton (SW11) grounds the active-Low program pin of the FPGA. The INIT LED (DS54) lights during FPGA initialization. The DONE LED (DS29) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, the DONE LED lights indicating that the FPGA is successfully configured.

FPGA U2 User LEDs, DIP and Pushbutton Switches

Figure 1-2 callout [27]

DS30 through DS35, DS37, and DS38 are eight active-High LEDs that are connected to user I/O pins on FPGA U2 as shown in Table 1-11. These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-11: **FPGA U2 User LEDs**

FPGA U2 Pin	Net Name	Reference Designator
K33	U2_USER_LED1	DS38
L33	U2_USER_LED2	DS37
A37	U2_USER_LED3	DS35
B37	U2_USER_LED4	DS34
B36	U2_USER_LED5	DS33
B35	U2_USER_LED6	DS32
A35	U2_USER_LED7	DS31
A34	U2_USER_LED8	DS30

FPGA U2 User DIP Switches (Active High)

Figure 1-2 callout [27]

FPGA U1 DIP switch SW16 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-12. These switched signals can be used to set control bits or any other purpose determined by the user.

Table 1-12: **FPGA U2 User DIP Switches**

FPGA U2 Pin	Net Name	Reference Designator
J20	U2_USER_SW1	SW16
K21	U2_USER_SW2	
P21	U2_USER_SW3	
R21	U2_USER_SW4	
G20	U2_USER_SW5	
H21	U2_USER_SW6	
E20	U2_USER_SW7	
F20	U2_USER_SW8	

User Push Buttons (Active High)

Figure 1-2 callout [27]

SW12, SW13, SW14 and SW15 are active-High user pushbuttons that are connected to user I/O pins on FPGA U2 as shown in Table 1-13. These switches can be used for any purpose determined by the user.

Table 1-13: **FPGA U2 User Pushbuttons**

FPGA U2 Pin	Net Name	Reference Designator
H26	U2_USER_PB1	SW12
J26	U2_USER_PB2	SW13
N24	U2_USER_PB3	SW14
N23	U2_USER_PB4	SW15

FPGA U2 User GPIO Header

Figure 1-2 callout [28]

A standard 2 x 6, 100-mil pitch header (J103) brings out six FPGA I/Os for test purposes. Table 1-14 lists these pins. J103 odd pin numbers are wired to GND (ground).

Table 1-14: **FPGA U2 User GPIO Header J103**

FPGA U1 Pin	Net Name	J103 Pin
J35	U2_USER_IO_1	2
K35	U2_USER_IO_2	4
D35	U2_USER_IO_3	6
E35	U2_USER_IO_4	8
P35	U2_USER_IO_5	10
P34	U2_USER_IO_6	12

FPGA U2 USB to UART Bridge

Figure 1-2 callout [29]

Communications between the ML630 board FPGA U2 and a host computer are accomplished through a USB cable connected to J106. Control is provided by U79, a USB to UART bridge (Silicon Laboratories CP2103). Table 1-15 lists the pin assignments and signals for the USB connector J106.

Table 1-15: **J106 USB Mini-B Connector Pin Assignments and Signals**

J106 Pin	Signal Name	Description
1	VBUS	+5V from host system
2	U2_USB_D_N	Bidirectional differential serial data (N-side)
3	U2_USB_D_P	Bidirectional differential serial data (P-side)
4	ID	Not used8

The CP2103 supports an I/O voltage range of 2.5V on the ML630 board. The connections between FPGA U2 and CP2103 should use the LVCMOS25 I/O standard. UART IP (for example, Xilinx® XPS UART Lite) must be implemented in the FPGA logic. FPGA U2 supports the USB to UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS)

Connections of these signals between the FPGA and the CP2103 at U79 are listed in Table 1-16.

Table 1-16: **FPGA U2 to U79 (CP2103 Bridge) Connections**

FPGA U2 Pin	FPGA Function	Net Name	U79 Pin	U79 Function
P11	RTS, output	U2_USB_CTS_I	22	CTS, input
P10	CTS, input	U2_USB_RTS_O	23	RTS, output
F10	TX, data out	U2_USB_RXD_I	24	RXD, data in
E10	RX, data in	U2_USB_TXD_O	25	TXD, data out

The bridge device also provides as many as four GPIO signals that can be defined by the user for status and control information (see Table 1-17).

Table 1-17: **FPGA U2 to U79 (CP2103 Bridge) User GPIO Connections**

FPGA U2 Pin	Net Name	U79 Pin
L10	U2_USB_GPIO_0	19
M11	U2_USB_GPIO_1	18
D10	U2_USB_GPIO_2	17
E11	U2_USB_GPIO_3	16

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB to UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTerminal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the ML630 board.

References

More information on the Silicon Labs CP2103 USB-to-UART bridge is available at: http://www.silabs.com/products/interface/usbtouart/Pages/default.aspx.

FPGA U2 200 MHz 2.5V LVDS Oscillator

Figure 1-2 callout [30]

Oscillator U63, located on the bottom of the board, is connected to FPGA U2 global clock inputs. Table 1-18 lists FPGA U2 pin connections to the LVDS oscillator U63.

Table 1-18: **FPGA U2 LVDS Oscillator U63 Global Clock Connections**

FPGA U2 Pin	Net Name	U63 Pin
AR33	U2_LVDS_OSC_P	4
AT33	U2_LVDS_OSC_N	5

References

More information on the SiTime SI9102AI oscillator is available at: http://www.sitime.com/products/differential-oscillators/sit9102.

FPGA U1 FCI Airmax Interlaken Connectors

Figure 1-2 callout [31, 32, 34]

The ML630 board provides four sets of FCI Airmax male/female (plug/receptacle) connector pairs implementing the Interlaken protocol.

Note: The Interlaken protocol definition and recommended connector pinouts can be found in the following documents located on the Interlaken Alliance website (http://www.interlakenalliance.com): Protocol: Interlaken Protocol Definition v1.x and Connector Pinouts: Interlaken Interop Recommendations v1.x. The Protocol Definition document also discusses the flow control functions provided by the TX and RX FC_CLK, FC_DATA and FC_SYNC connector pins.

Three sets of connector pairs (P1/J1, P2/J2, and P3/J3) are wired to FPGA U1. Table 1-19 through Table 1-24 show FPGA U1 to FCI connector details. Refer to the block diagram on the ML630 schematic, page 2, for an overview of the connectivity shown in these tables.