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ML631 Virtex-6 HXT FPGA Packet Processor/Traffic Manager Evaluation Board

User Guide

UG841 (v1.0) March 9, 2012

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/09/2012	1.0	Initial Xilinx release.

Table of Contents

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Chapter 1

ML631 Board Features and Components

This user guide describes the components and features of the ML631 Virtex-6 HXT FPGA Packet Processor/Traffic Manager (PP/TM) evaluation board. The ML631 board provides the hardware environment for characterizing and evaluating the GTX and GTH transceivers available on the Virtex-6 XC6VHXT565-2FFG1923C FPGA.

ML631 Board Features

Details for the following features are described in Feature Descriptions, page 6.

- Two Virtex-6 XC6VHXT565-2FFG1923C FPGAs
- Onboard power regulators for all necessary voltages with power status LEDs
- Two types of external power supply jacks (12V brick DIN4 type, PC ATX type)
- USB JTAG configuration port for use with USB A to Mini-B cable
- System ACE™ controller with companion SanDisk® CompactFlash® socket
- General purpose pushbuttons, DIP switches, and LEDs for each FPGA
- VGA 2 x 5 male debug header for the U2 FPGA
- USB-to-UART bridge with USB Mini-B connector for the U2 FPGA
- I^2C bus hosting EEPROM and clock sources
- A separate SiTime fixed 200-MHz 2.5V LVDS oscillator wired to the global clock inputs of each FPGA
- Six pairs of differential clock input SMA connectors
- Six I^2C programmable Silicon Labs Si570 3.3V LVDS 10-MHz to 810-MHz oscillators
- Two differential input 8 x 8 crosspoint switches providing 16 selectable differential clock sources
- Three sets of plug and receptacle FCI Airmax 120-pin connectors, two implementing the Interlaken interconnect protocol and one available for an OTN/OTN client interface
- 9 x 32-bit DDR3 memory on the U1 FPGA
- 4 x 16-bit DDR3, 2 x 18-bit DDR2, and 2 x 36-bit QDRII+ memories on the U2 FPGA
- NetLogic Microsystems NL92000 series network processor [ternary content addressable memory (TCAM)] adjunct on the U2 FPGA

The ML631 board block diagram is shown in Figure 1-1.

Caution! The ML631 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

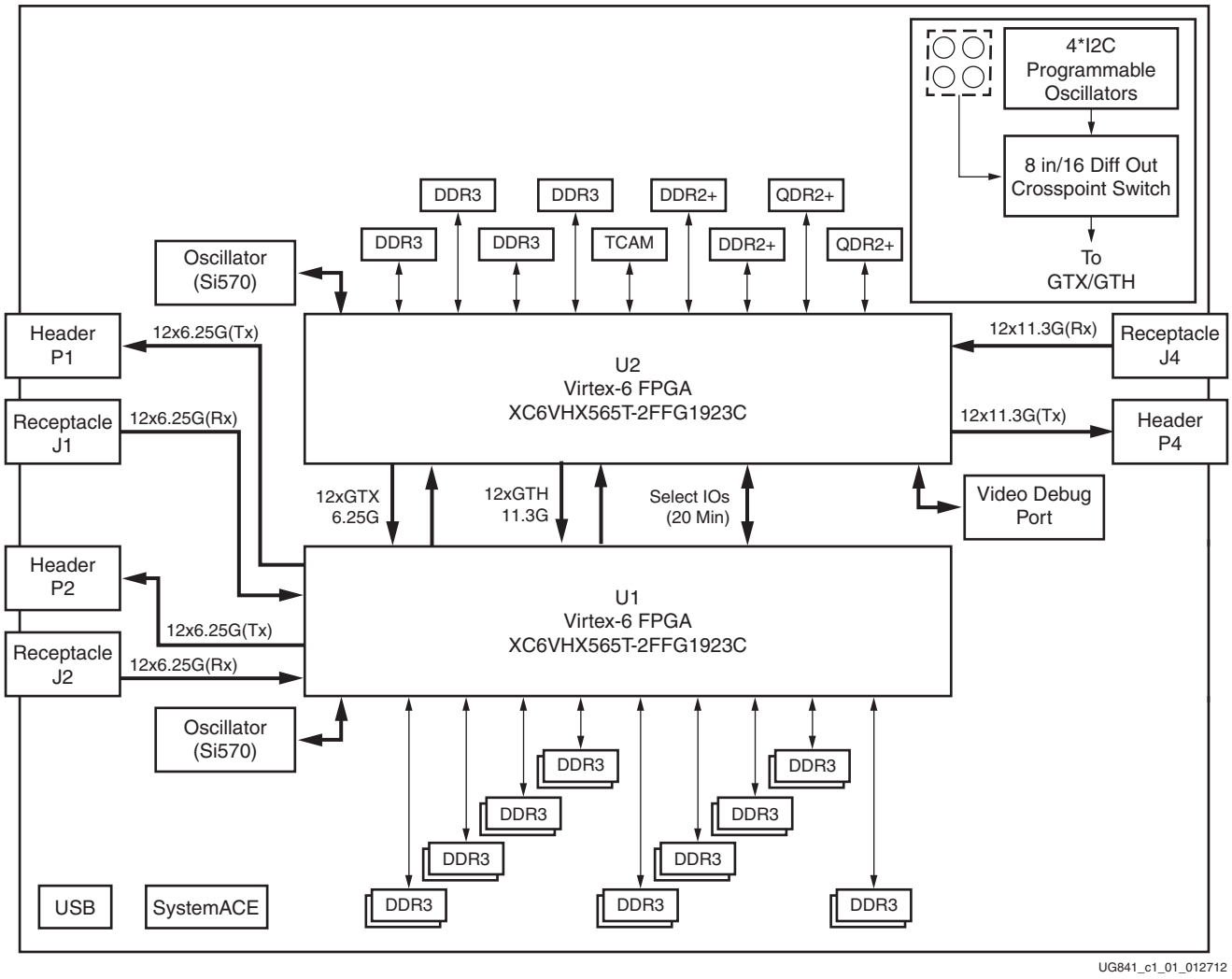

Figure 1-1: **ML631 Board Block Diagram**

Feature Descriptions

This section is intended to be used with the *ML631 Schematic* [Ref 1]. The ML631 board hosts a complicated clocking system and intricate FPGA-to-FPGA and Interlaken connector connectivity that the schematic helps clarify. Refer to the schematic pages associated with the circuitry described in each section of this detailed description [Ref 1].

Figure 1-2 shows the ML631 board. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1 and the other sections in this chapter.

Note: The image in Figure 1-2 is for reference only. It might not reflect the current revision of the board.

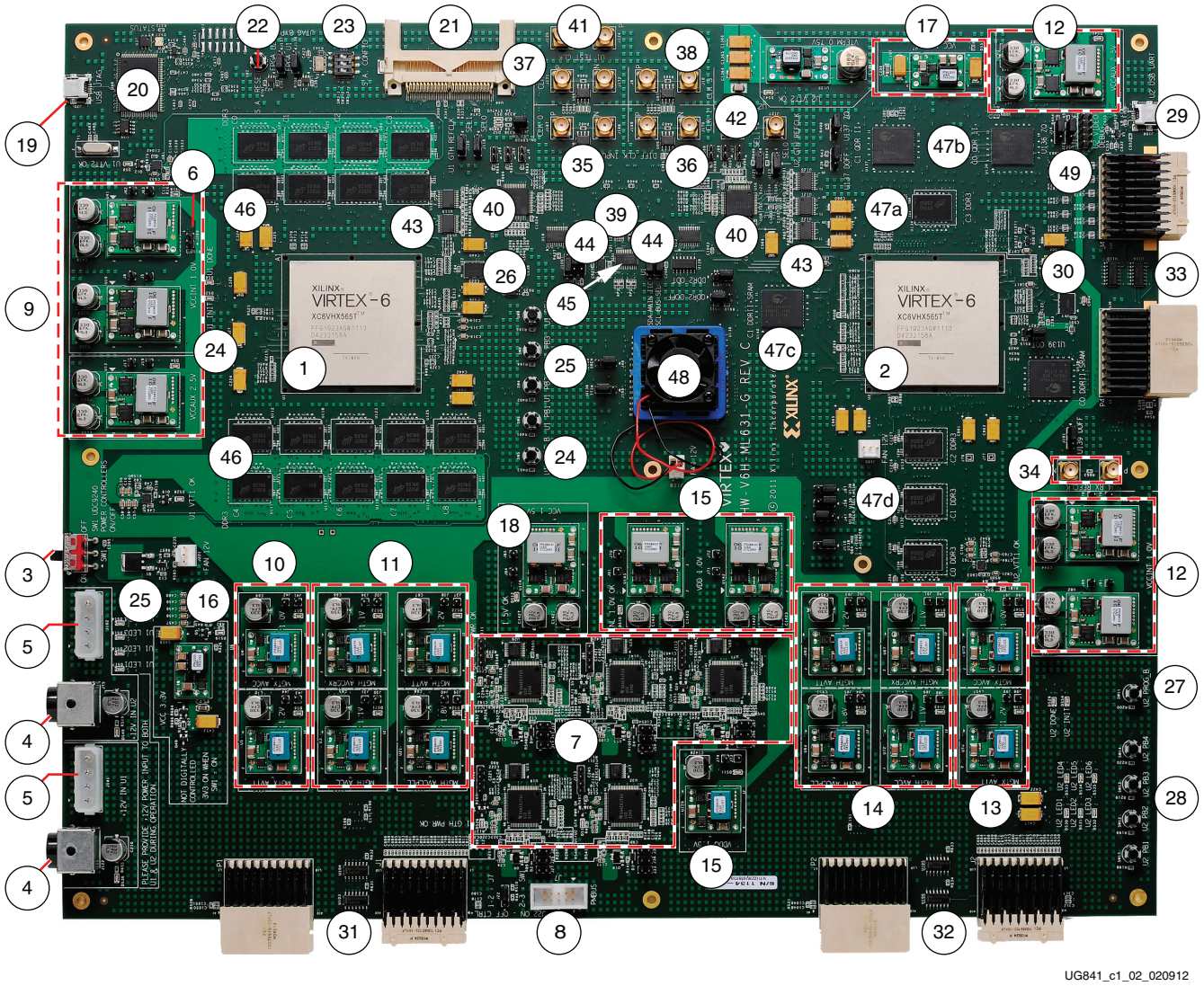

Figure 1-2: **ML631 Board Components**

Table 1-1 summarizes features referenced in Figure 1-2, and lists the page in the *ML631 Schematic* that contains more details [Ref 1].

Table 1-1: **ML631 Board (Revision C) Features and Corresponding Schematic References**

Number	Feature	Notes	Schematic Page
1	Virtex-6 HXT FPGA	U1 XC6VHXT565-2FFG1923C	2
2	Virtex-6 HXT FPGA	U2 XC6VHXT565-2FFG1923C	3
3	On-Off soft slide switch	SW1	65
4	DIN-4 12V input connectors	J122 for the U1 FPGA, J75 for the U2 FPGA	63, 127
5	ATX 4-pin 12V input connectors	J141 for the U1 FPGA, J102 for the U2 FPGA	63, 127
6	Voltage regulator inhibit header	J289 (used only for CM power config.)	66

Table 1-1: **ML631 Board (Revision C) Features and Corresponding Schematic References *(Cont'd)***

Number	Feature	Notes	Schematic Page
7	TI power system controllers	U8, U19, U32, U77, U141	65, 70, 75, 129, 134
8	PMBus connector	J7 for TI Fusion GUI GPIO adapter pod	65
9	U1 V_{CCINT}, V_{CCAUX} TI regulators	U10/U41 V_{CCINT}, U12 V_{CCAUX} (3 x TI PTD08A020W)	66, 67
10	U1 GTX TI regulators	U4 AVCC, U5 AVTT (2 x TI PTD08A010W)	76, 77
11	U1 GTH TI regulators	U3 AVCC, U14 AVCCRX, U20 AVTT, U21 AVCCPLL (1 x PTD08A010W, 3 x PTD08A006W)	71, 72, 73, 74
12	U2 V_{CCINT}, V_{CCAUX} TI regulators	U81/U82 V_{CCINT}, U83 V_{CCAUX} (3 x TI PTD08A020W)	68, 69
13	U2 GTX TI regulators	U73 AVCC, U74 AVTT (2 x TI PTD08A010W)	78, 79
14	U2 GTH TI regulators	U72 AVCC, U67 AVCCRX, U68 AVTT, U69 AVCCPLL (1 x PTD08A010W, 3 x PTD08A006W)	130, 131, 132, 133
15	NetLogic Microsystems processor TI regulators	U142/U143 V_{DD}, U129 V_{DDQ} (2 x TI PTD08A020W, 1 x PTD08A006W)	135, 136
16	ML631 board-wide 3.3V regulator	U6 VCC3V3 TI PTH12000W	8
17	ML631 board-wide 1.8V regulator	U7 VCC1V8 TI PTH12000W	83
18	ML631 board-wide 1.5V regulator	U144 VCC1V5 PTD08A020W	137
19	USB JTAG mini-USB connector	J20	6
20	Embedded JTAG circuits	U48 CY7C68013A, U45 XC2C256	6
21	System ACE controller, CompactFlash socket	U47 XACCE-TQ144I (bottom of board), U46 CF socket	5
22	System ACE controller reset pushbutton switch	SW2	5
23	CompactFlash image select switch	SW3	5
24	U1 PROG PB, INIT, and DONE LEDs	SW5 PROG pushbutton, DS20 INIT, DS6 DONE	16
25	U1 user LEDs and pushbuttons	DS17, 16, 15, 14 user LED1, 2, 3, 4, SW6, 4, 8, 9 user PB1, 2, 3, 4	16
26	U1 fixed 200-MHz system clock	U22 SI9102 2.5V 20 PPM 200.0000 MHz LVDS	16
27	U2 PROG PB, INIT, and DONE LEDs	SW11 PROG pushbutton, DS54 INIT, DS29 DONE	82
28	U2 user LEDs and pushbuttons	DS30–DS35 are user LED1-user LED6; SW15,12,13, and 14 are user PB1–4	82
29	U2 USB UART mini-USB connector	J106	81
30	U2 fixed 200-MHz system clock	U63 SI9102 2.5V 20 PPM 200.0000 MHz LVDS	82

Table 1-1: **ML631 Board (Revision C) Features and Corresponding Schematic References *(Cont'd)***

Number	Feature	Notes	Schematic Page
31	U1 FCI Airmax connector pair	P1, J1 (connected to GTX transceivers)	26, 27
32	U1 FCI Airmax connector pair	P2, J2 (connected to GTX transceivers)	23, 24
33	U2 FCI Airmax connector pair	P4, J4 (connected to GTH transceivers)	87, 88
34	U2 J4 RX REFCLK input SMA connectors	SMA J134, J135	88
35	SMA input clock differential pair	SMA J167, J168, U98 ICS85311 1-to-2 LVPECL clock buffer	9
36	SMA input clock differential pair	SMA J169, J170, U99 ICS85311 1-to-2 LVPECL clock buffer	9
37	SMA input clock differential pair	SMA J171, J172, U96 ICS85311 1-to-2 LVPECL clock buffer	9
38	SMA input clock differential pair	SMA J9, J10, U97 ICS85311 1-to-2 LVPECL clock buffer	9
39	ML631 programmable clock sources	U43, U44, U51, U52 Si570 each with U53, U54, U55, U56 ICS85311 1-to-2 LVPECL clock buffers (bottom of board)	10
40	ML631 8 x 8 crosspoint clock switches	U57, U58 TI SN65LVP408PAP	14
41	U1 differential test clock input SMA	SMA J124, J125, U126 ICS854S006 1-to-6 LVDS clock buffer	12
42	U2 differential test clock input SMA	SMA J126, J127, U127 ICS854S006 1-to-6 LVDS clock buffer	13
43	ML631 differential clock multiplexer circuits	5 each ICS85356 U102, U115, U120, U121, U122	12, 13
44	U1, U2 programmable clock sources	U64 Si570 (bottom of board) U13 ICS854S006 1-to-6 LVDS clock buffer; U65 Si570 (bottom of board) U18 ICS854S006 1-to-6 LVDS clock buffer	15, 81
45	ML631 I^2C bus residents	U59 M24C02 EEPROM, U31 PCA9548 bus-expander	10
46	U1 memory system	9x 32-bit DDR3 chip pairs of MT41J128M16HA, controller C0: U24, U76; C1: U25, U78; C2: U84, U88; C3: U89, U101; C4: U111, U112; C5: U117, U118; C6: U119, U123; C7: U124, U125; C8: U130, U131	29–55
47	U2 memory system	See 47a, 47b, 47c	
47a	DDR3	4x 16-bit DDR3 MT41J128M16HA, controller C0: U70; C1: U132; C2: U133; C3: U134	92–99
47b	DDR2 SRAM	2x 18-bit DDR2 CY7C12481KV18, controller C0: U139; C1: U140	100–103
47c	QDRII+	2x 36-bit QDR2+ CY7C1565KV18, controller C0: U136; C1: U137	104–113

Table 1-1: **ML631 Board (Revision C) Features and Corresponding Schematic References *(Cont'd)***

Number	Feature	Notes	Schematic Page
48	NetLogic Microsystems processor	U138 NL9256EFVH-400H	117–118
49	U2 VGA debug connector	J60 2x5 male pin header	119

Default Shunts

A list of shunts and their required positions for board operation is provided in Appendix A, Default Shunt Positions.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for all power rails except the fixed 3.3V and 1.8V using the Texas Instruments' Fusion Digital Power graphical user interface (GUI). All onboard TI power controllers are wired to the same PMBus. The PMBus connector, J7, is provided for use with the TI GPIO interface adapter (PMBus pod) and associated TI Fusion Digital Power GUI.

More information about the power system components used by the ML631 board is available from the Texas Instruments digital power website [Ref 18].

U1 and U2 FPGAs

See Figure 1-2 callouts [1, 2].

The ML631 board hosts two Virtex-6 XC6VHXT565-2FFG1923C FPGAs. Each FPGA provides six four-transceiver GTH Quads and ten four-transceiver GTX Quad high-speed interfaces.

Appendix D, Additional Resources provides references to ML631 board documents, files, and resources.

Board Power

See Figure 1-2 callouts [3, 4, 5].

The ML631 board is powered through two 4-pin DIN right angle connectors, J122 and J75, using the two 12V, 15A AC adapters included with the board.

Power can also be provided through J141 and J102 ATX hard disk 4-pin power connectors. J122 (4-pin DIN connector) and J141 (ATX connector) are wired in parallel, as are J75 and J102. When the board power is supplied through J122 and J75, 12 VDC is present at the ATX connectors J141 and J102 and vice versa.

Note: Use of a switchable multiple outlet AC power strip is recommended for providing mains power to the two AC adapters. Both adapters can be turned on and off simultaneously via the power strip on/off switch.

> ***Caution!*** Only use two power supplies of the same type. Power the ML631 board through two connectors at the same time (J122 and J75 or J141 and J102, depending on power supply type). Do NOT apply power to all four power input connectors J122/J75 and J141/J102 at the same time. Doing so can damage the ML631 board and void the board warranty.

When the AC adapters are connected to the ML631 board and turned on through the AC power strip, 12 VDC is applied to the 12V power planes. Green LED indicators DS36 and DS49 (adjacent to each 4-pin DIN connector) illuminate to indicate 12V power is on.

Switch SW1

The ML631 board U1 and U2 FPGA power regulators are turned on and off by slide switch SW1. When this switch is in the ON position, power is applied to the FPGAs, and the green LEDs adjacent to each active regulator illuminate.

Figure 1-3 shows the power system block diagram for the U1 FPGA and part of the U2 FPGA. Circuit details are available in the *ML631 Schematic* pages 8, 63–80, 83 and 127–138 as noted in the various function blocks [Ref 1].

Power System

Figure 1-3 shows the onboard power supply architecture for the U1 FPGA.

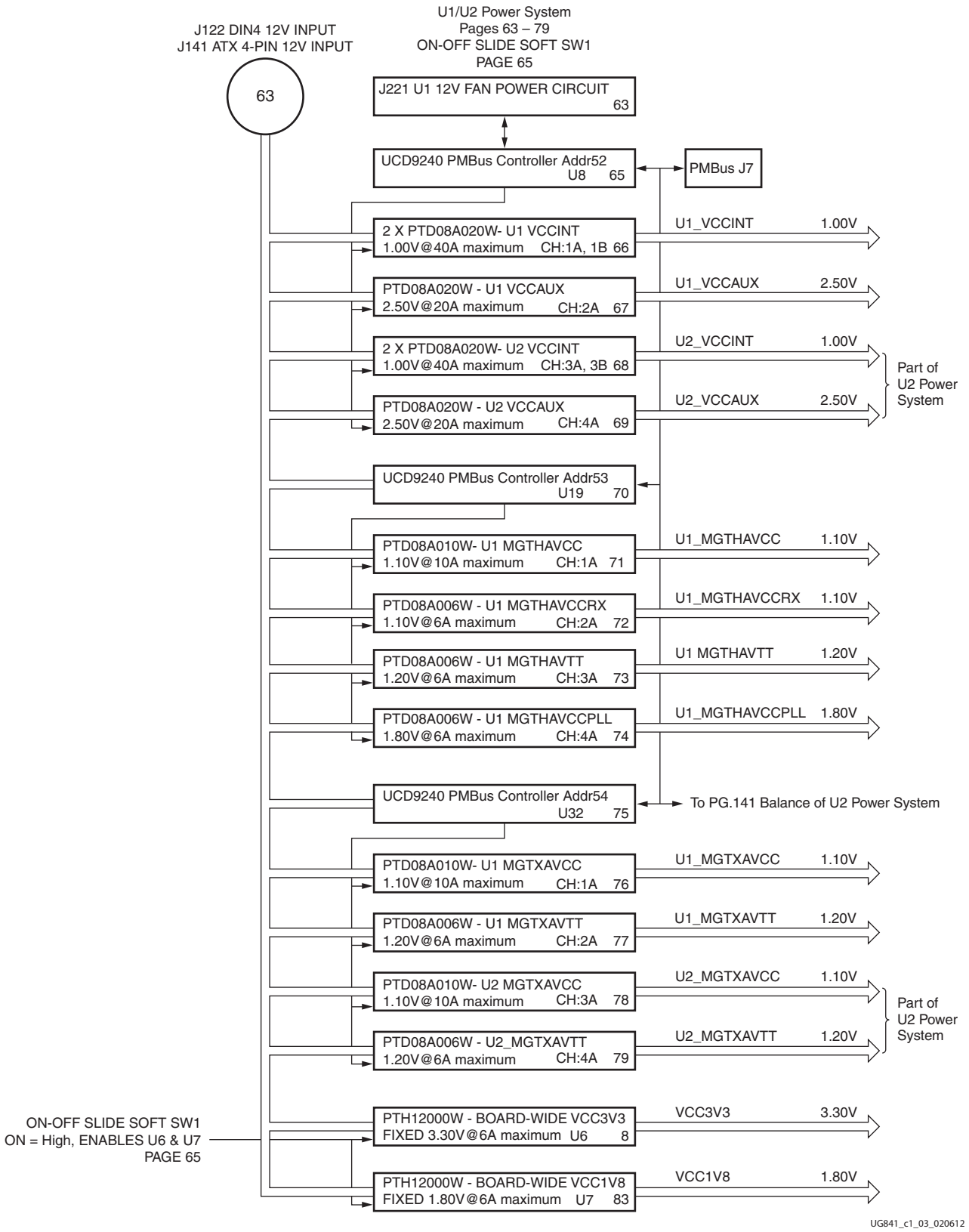

Figure 1-3: **Power Block Diagram for the U1 FPGA**

Figure 1-4 shows the onboard power supply architecture for the U2 FPGA. Circuit details are available in *ML631 Schematic* pages 127 through 137 as noted in the various function blocks [Ref 1].

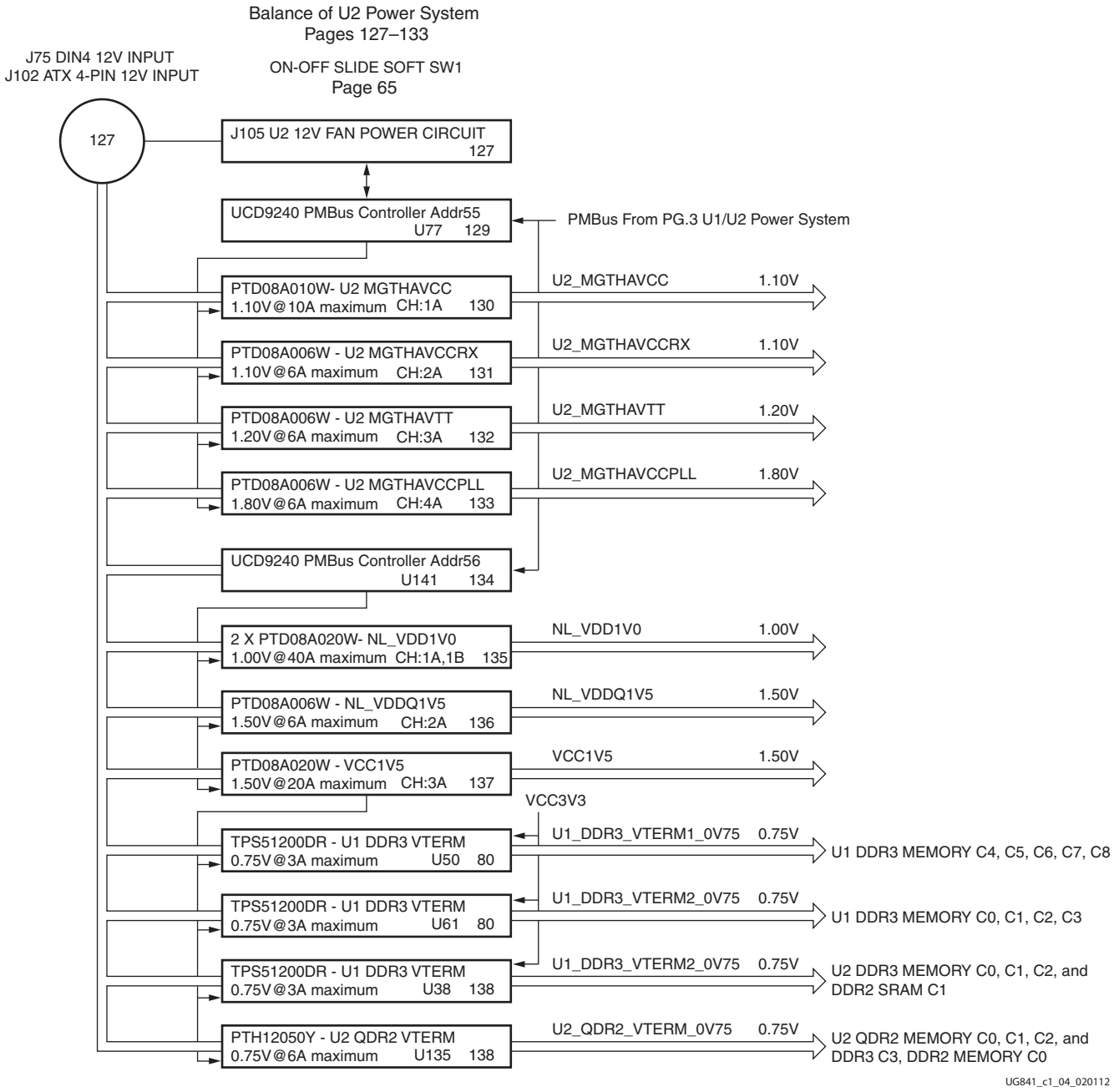

Figure 1-4: **Power Block Diagram for the U2 FPGA**

The ML631 board uses power regulators and PMBus-compliant digital PWM system controllers from Texas Instruments to supply the U1 and U2 voltages listed in Table 1-2.

Table 1-2: **Onboard Power System Devices**

Device	Ref. Des.	Description	Power Rail Net Name	Typical Voltage
U1 and U2 Core Voltage Controller and Regulators				
UCD9240PFC	U8	PMBus-compliant digital PWM system controller (address = 52)		
PTD08A020W	U10	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 of 2 phases	U1_VCCINT	1.0V
PTD08A020W	U41	Adjustable switching regulator 20A, 0.6V to 3.6V, 2 of 2 phases	U1_VCCINT	1.0V
PTD08A020W	U12	Adjustable switching regulator 20A, 0.6V to 3.6V	U1_VCCAUX	2.5V
PTD08A020W	U81	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 of 2 phases	U2_VCCINT	1.0V
PTD08A020W	U82	Adjustable switching regulator 20A, 0.6V to 3.6V, 2 of 2 phases	U2_VCCINT	1.0V
PTD08A020W	U83	Adjustable switching regulator 20A, 0.6V to 3.6V	U2_VCCAUX	2.5V
U1 GTH Transceiver Voltage Controller and Regulators				
UCD9240PFC	U19	PMBus-compliant digital PWM system controller (address = 53)		
PTD08A010W	U3	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTHAVCC	1.1V
PTD08A006W	U14	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVCCRX	1.1V
PTD08A006W	U20	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTHAVTT	1.2V
PTD08A006W	U21	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVCCPLL	1.8V
U1 and U2 GTX Transceiver Voltage Controller and Regulators				
UCD9240PFC	U32	PMBus-compliant digital PWM system controller (address = 54)		
PTD08A010W	U4	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVCC	1.1V
PTD08A010W	U5	Adjustable switching regulator 10A, 0.6V to 3.6V	U1_MGTXAVTT	1.2V
PTD08A010W	U73	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVCC	1.1V
PTD08A010W	U74	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVTT	1.2V
U2 GTH Transceiver Voltage Controller and Regulators				
UCD9240PFC	U77	PMBus-compliant digital PWM system controller (address = 55)		
PTD08A010W	U72	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTHAVCC	1.1V
PTD08A006W	U67	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVCCRX	1.1V
PTD08A006W	U68	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTHAVTT	1.2V
PTD08A006W	U69	Adjustable switching regulator 10A, 0.6V to 3.6V	U2_MGTXAVCCPLL	1.8V
U138 NetLogic and Board-Wide Voltage Controller and Regulators				
UCD9240PFC	U141	PMBus-compliant digital PWM system controller (address = 56)		

Table 1-2: **Onboard Power System Devices *(Cont'd)***

Device	Ref. Des.	Description	Power Rail Net Name	Typical Voltage
PTD08A020W	U142	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 of 2 phases	NL_VDD1V0	1.0V
PTD08A020W	U143	Adjustable switching regulator 20A, 0.6V to 3.6V, 2 of 2 phases	NL_VDD1V0	1.0V
PTD08A006W	U129	Adjustable switching regulator 6A, 0.6V to 3.6V	NL_VDDQ1V5	1.5V
PTD08A020W	U144	Adjustable switching regulator 20A, 0.6V to 3.6V, 1 of 2 phases	VCC1V5	1.5V
Auxiliary Power Fixed Output Voltage Regulators				
PTH12000W	U6	Adjustable switching regulator 6A, 1.2V to 5.5V	VCC3V3	3.3V
PTH12000W	U7	Adjustable switching regulator 6A, 1.2V to 5.5V	VCC1V8	1.8V

Disabling FPGA Onboard Power

See Figure 1-2 callout [6].

All ML631 voltage regulators are disabled by installing a shunt across pins 1-2 of header J289. If 12V is supplied to the board with the J289 shunt installed, the TI power system controllers power up, and if the SW1 on-off slide switch is then switched to the ON position, all board voltage regulators remain inhibited. J289 is typically installed only for assembly house power system programming, and is not installed for standard board operation.

FPGA Configuration

See Figure 1-2 callout [19–23].

The FPGA is configured in JTAG mode only, using one of these options:

- Embedded USB JTAG circuit using USB cable (type A to Mini-B)
- System ACE controller (using a CompactFlash card loaded with bit files)

The FPGA Embedded JTAG option is enabled by connecting the Mini-B connector end of the USB cable to J20 on the ML631 board. The type A connector end of the USB cable plugs into a PC hosting a Xilinx FPGA configuration tool (either ChipScope™ Pro tool or Impact software), which is then used to configure the two FPGAs on the ML631 board.

The FPGAs can also be configured through the System ACE controller by setting the 3-bit configuration address DIP switches (SW3) to select one of eight bitstreams stored on a CompactFlash memory card plugged into socket U46 (see Configuration Address DIP Switches, page 16).

Upon power-on, the System ACE controller checks for the presence of a CompactFlash card and loads the FPGA configuration files from it, if present.

The JTAG chain of the board is illustrated in Figure 1-5. Each component (except the System ACE controller IC) with a JTAG interface has a bypass shunt which permits the component to be in the chain or bypassed.

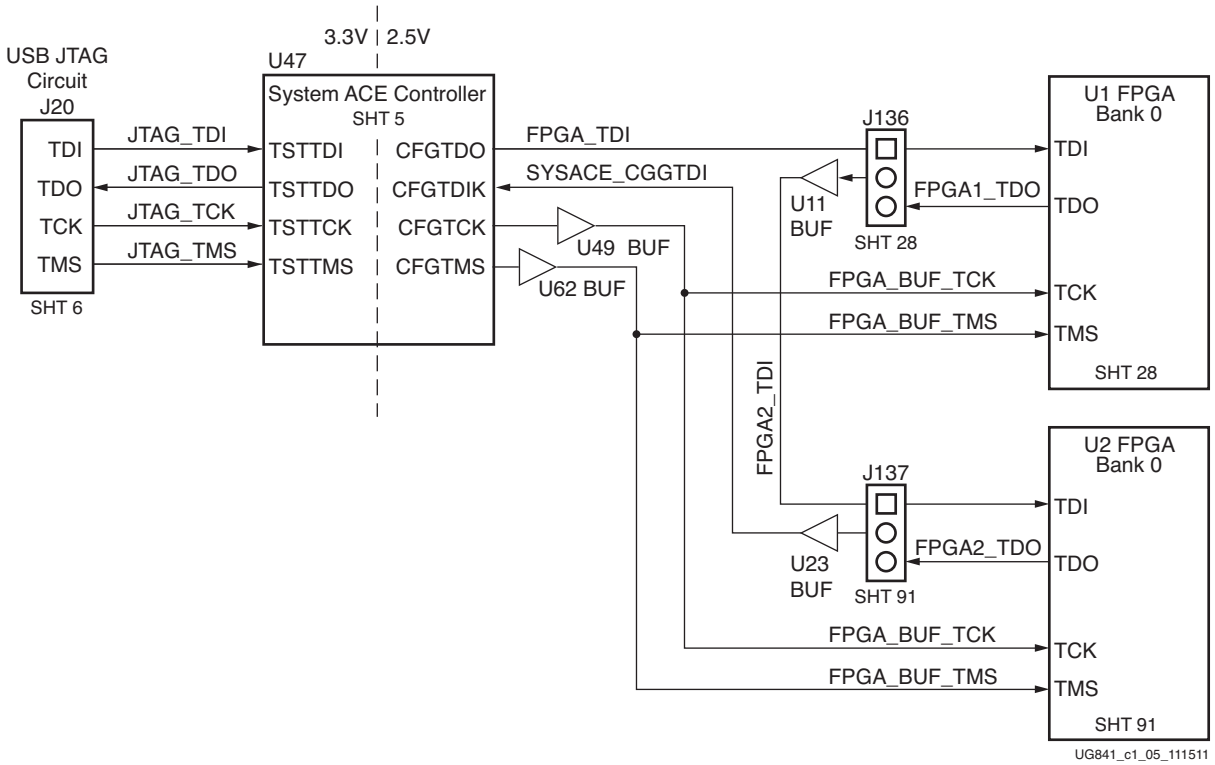

Figure 1-5: **JTAG Chain Diagram**

System ACE Controller

See Figure 1-2 callout [21].

The onboard System ACE controller (U47) allows storage of multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGAs. The CompactFlash card plugs into the CompactFlash card socket (U46) located directly above the System ACE controller on the back side of the board.

System ACE Controller Reset

See Figure 1-2 callout [22].

Pressing pushbutton SW2 (RESET) resets the System ACE controller. Reset is an active-Low input.

Configuration Address DIP Switches

See Figure 1-2 callout [23].

DIP switch SW3 selects one of the eight configuration bitstream addresses in the CompactFlash memory card. The switch settings for selecting each address are shown in Table 1-3.

Table 1-3: **SW3 DIP Switch Configuration**

Address	ADR2	ADR1	ADR0
0	O(1)	O	O
1	O	O	C(2)
2	O	C	O
3	O	C	C
4	C	O	O
5	C	O	C
6	C	C	O
7	C	C	C

Notes:

1. O indicates the open switch position (Logic 0).
2. C indicates the closed switch position (Logic 1).

More information on the System ACE controller is available in DS080, *System ACE CompactFlash Solution* [Ref 2].

U1 FPGA PROG Pushbutton, INIT LED, and DONE LED

See Figure 1-2 callout [24].

Pressing the U1 PROG pushbutton (SW5) grounds the active-Low program pin of the FPGA. The INIT LED (DS20) lights during FPGA initialization. The DONE LED (DS56) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, the DONE LED lights, indicating that the FPGA is successfully configured.

U1 FPGA User LEDs and Pushbuttons

User LEDs

See Figure 1-2 callout [25].

DS14 through DS17 are four active-High LEDs that are connected to user I/O pins on the U1 FPGA as shown in Table 1-4. These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-4: **U1 FPGA User LEDs**

U1 FPGA Pin Number	Net Name	Reference Designator
K25	U1_USER_LED1	DS17
N23	U1_USER_LED2	DS16
D21	U1_USER_LED3	DS15
K22	U1_USER_LED4	DS14

User Pushbuttons

See Figure 1-2 callout [28].

SW4, SW6, SW8, and SW9 are active-High user pushbuttons that are connected to user I/O pins on the U1 FPGA as shown in Table 1-5. These switches can be used for any purpose determined by the user.

Table 1-5: **U1 FPGA User Pushbuttons**

U1 FPGA Pin Number	Net Name	Reference Designator
H34	U1_USER_PB1	SW6
H26	U1_USER_PB2	SW4
J25	U1_USER_PB3	SW8
AR18	U1_USER_PB4	SW9

U1 FPGA 200-MHz 2.5V LVDS Oscillator

See Figure 1-2 callout [26].

The ML631 board has one 2.5V LVDS differential 200-MHz oscillator for each FPGA (SiTime Si9102AI). Oscillator U22 (located on the back side of the board) is connected to the U1 FPGA. A 100Ω terminating resistor on the PCB enables use of DIFF_SSTL15 clock buffer inside the FPGA. Table 1-6 lists the FPGA pin connections to the oscillator.

Table 1-6: **U1 FPGA LVDS Oscillator U22 Global Clock Connections (1)**

FPGA Pin Number	Net Name	U7 Pin Number
R31	U1_LVDS_OSC_P	4
R32	U1_LVDS_OSC_N	5

Notes:

1. The UCF net names for these two clock signals are CLK200_P and CLK200_N, as shown in Appendix B, ML631 Master UCF Listing for U1.

For more information on the SiTime SI9102AI oscillator, visit the SiTime website [Ref 20].

U2 FPGA PROG Pushbutton, INIT LED, and DONE LED

See Figure 1-2 callout [27].

Pressing the U2 PROG pushbutton (SW11) grounds the active-Low program pin of the FPGA. The INIT LED (DS54) lights during FPGA initialization. The DONE LED (DS29) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, the DONE LED lights, indicating that the FPGA is successfully configured.

U2 FPGA User LEDs and Pushbuttons

User LEDs

See Figure 1-2 callout [28].

D30 through D35 are six active-High LEDs that are connected to user I/O pins on U2 FPGA as shown in Table 1-7. These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-7: **U2 FPGA User LEDs**

U2 FPGA Pin	Net Name	Reference Designator
BA15	U2_USER_LED1	DS30
AY15	U2_USER_LED2	DS31
AN21	U2_USER_LED3	DS32
AM21	U2_USER_LED4	DS33
BA13	U2_USER_LED5	DS34
BA14	U2_USER_LED6	DS35

User Pushbuttons

See Figure 1-2 callout [28].

SW12, SW13, SW14, and SW15 are active-High user pushbuttons that are connected to user I/O pins on the U1 FPGA as shown in Table 1-8. These switches can be used for any purpose determined by the user.

Table 1-8: **U2 FPGA User Pushbuttons**

U2 FPGA Pin	Net Name	Reference Designator
BD18	U2_USER_PB1	SW15
BC18	U2_USER_PB2	SW12
BC14	U2_USER_PB3	SW13
BB14	U2_USER_PB4	SW14

U2 FPGA USB-to-UART Bridge

See Figure 1-2 callout [24].

Communications between the ML631 board and a host computer are through a USB cable connected to J106. Control is provided by U79, a USB-to-UART bridge (Silicon Laboratories CP2103) [Ref 21]. Table 1-9 lists the pin assignments and signals for the USB connector J106.

Table 1-9: **J106 USB Mini-B Connector Pin Assignments and Signals**

J106 Pin	Signal Name	Description
1	VBUS	+5V from host system
2	U2_USB_D_N	Bidirectional differential serial data (N-side)
3	U2_USB_D_P	Bidirectional differential serial data (P-side)
4	ID	Not used

The CP2103 supports an I/O voltage range of 2.5V on the ML631 board. The 2.5V CP2103 I/O are routed through 2.5V-to-1.5V level-shifters to provide 1.5V compatibility with U2

1.5V V_{CCO} bank 20. UART IP (for example, Xilinx XPS UART Lite) must be implemented in the FPGA logic. U2 FPGA bank 20 supports the USB-to-UART bridge using four signal pins. Connections of these signals between the FPGA and the CP2103 at U79 are listed in Table 1-10.

Table 1-10: **U2 FPGA to U79 CP2103 Bridge Connections**

U2 FPGA Pin Number	FPGA Function	Net Name	U79 Pin Number	U79 Function
AT20	Request to Send (RTS), output	U2_USB_CTS_I	22	CTS, input
AU20	Clear to Send (CTS), input	U2_USB_RTS_O	23	RTS, output
AP23	Transmit (TX), data out	U1_USB_RXD_I	24	RXD, data in
AR23	Receive (RX), data in	U1_USB_TXD_O	25	TXD, data out

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB-to-UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTerminal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the ML631 board.

More information on the Silicon Labs CP2103 USB-to-UART bridge is available at the Silicon Labs website [Ref 21].

U2 FPGA 200-MHz 2.5V LVDS Oscillator

See Figure 1-2 callout [30].

Oscillator U63, located on the back side of the board, is connected to the U2 FPGA global clock inputs. A 100Ω terminating resistor on the PCB enables use of DIFF_SSTL15 clock buffer inside the FPGA. Table 1-11 lists the U2 FPGA pin connections to the LVDS oscillator U63.

Table 1-11: **U2 FPGA LVDS Oscillator U63 Global Clock Connections**

U2 FPGA Pin Number	Net Name	U63 Pin Number
R31	U2_LVDS_OSC_P	4
R32	U2_LVDS_OSC_N	5

More information on the SiTime SI9102AI oscillator is available at the SiTime website [Ref 20].

U1 FPGA FCI Airmax Interlaken Connectors

See Figure 1-2 callout [31, 32].

The ML631 board provides three sets of FCI Airmax male/female (plug/receptacle) connector pairs, two sets implementing the Interlaken protocol, and one set available for OTN/OTN interface [Ref 23].

Two sets of connector pins (P1/J1, P2/J2) are wired to the U1 FPGA. Table 1-12 through Table 1-17 show the U1 FPGA to FCI connector details. Refer to the block diagram in the *ML631 Schematic* for an overview of the connectivity shown in these tables [Ref 1]. U1 FPGA banks 113, 114, and 115 connect to FCI connectors P1 and J1.

Table 1-12: **U1 FPGA FCI Connector P1**

FCI Connector P1		Net Name	U1 FPGA Pin Number
Pin Name	Pin Number		
TX0_P	A7	U1_MGTTX0_115_P	AA3
TX0_N	B7	U1_MGTTX0_115_N	AA4
TX1_P	D6	U1_MGTTX1_115_P	Y1
TX1_N	E6	U1_MGTTX1_115_N	Y2
TX2_P	D8	U1_MGTTX2_115_P	W3
TX2_N	E8	U1_MGTTX2_115_N	W4
TX3_P	A9	U1_MGTTX3_115_P	V1
TX3_N	B9	U1_MGTTX3_115_N	V2
TX4_P	A3	U1_MGTTX1_114_P	AD1
TX4_N	B3	U1_MGTTX1_114_N	AD2
TX5_P	D2	U1_MGTTX0_114_P	AE3
TX5_N	E2	U1_MGTTX0_114_N	AE4
TX6_P	D4	U1_MGTTX2_114_P	AC3
TX6_N	E4	U1_MGTTX2_114_N	AC4
TX7_P	A5	U1_MGTTX3_114_P	AB1
TX7_N	B5	U1_MGTTX3_114_N	AB2
TX_REFCLK_P	A1	U1_P1_TX_REFCLK_C_P	U13.16
TX_REFCLK_N	B1	U1_P1_TX_REFCLK_C_N	U13.17
TX_FC_CK	E10	U1_AMH1_FC_CK	BD33
TX8_P	G5	U1_MGTTX3_113_P	AF1
TX8_N	H5	U1_MGTTX3_113_N	AF2
TX9_P	G3	U1_MGTTX1_113_P	AH1
TX9_N	H3	U1_MGTTX1_113_N	AH2
TX10_P	J4	U1_MGTTX2_113_P	AG3
TX10_N	K4	U1_MGTTX2_113_N	AG4
TX11_P	G1	U1_MGTTX0_113_P	AJ3
TX11_N	H1	U1_MGTTX0_113_N	AJ4
TX12_P	J6	U1_AMH1_IO0	BB24
TX12_N	K6	U1_AMH1_IO1	BA24
TX13_P	J10	U1_AMH1_IO2	AP24
TX13_N	K10	U1_AMH1_IO3	AN24
TX14_P	J2	U1_AMH1_IO4	AU24

Table 1-12: **U1 FPGA FCI Connector P1 *(Cont'd)***

FCI Connector P1		Net Name	U1 FPGA Pin Number
Pin Name	Pin Number		
TX14_N	K2	U1_AMH1_IO5	AR25
TX15_P	J8	U1_AMH1_IO6	AP25
TX15_N	K8	U1_AMH1_IO7	AJ18
TX_FC_DATA	H7	U1_AMH1_FC_DATA	BC33
TX_FC_SYNC	H9	U1_AMH1_FC_SYNC	AL33

Table 1-13: **U1 FPGA FCI Connector J1**

FCI Connector J1		Net Name	U1 FPGA Pin Number
Pin Name	Pin Number		
RX0_P	A7	U1_MGTRX0_115_C_P	Y5
RX0_N	B7	U1_MGTRX0_115_C_N	Y6
RX1_P	D6	U1_MGTRX1_115_C_P	W7
RX1_N	E6	U1_MGTRX1_115_C_N	W8
RX2_P	D8	U1_MGTRX2_115_C_P	V5
RX2_N	E8	U1_MGTRX2_115_C_N	V6
RX3_P	A9	U1_MGTRX3_115_C_P	U7
RX3_N	B9	U1_MGTRX3_115_C_N	U8
RX4_P	A3	U1_MGTRX1_114_C_P	AC7
RX4_N	B3	U1_MGTRX1_114_C_N	AC8
RX5_P	D2	U1_MGTRX0_114_C_P	AD5
RX5_N	E2	U1_MGTRX0_114_C_N	AD6
RX6_P	D4	U1_MGTRX2_114_C_P	AB5
RX6_N	E4	U1_MGTRX2_114_C_N	AB6
RX7_P	A5	U1_MGTRX3_114_C_P	AA7
RX7_N	B5	U1_MGTRX3_114_C_N	AA8
RX_REFCLK_P	A1	U1_J1_RX_REFCLK_P	Y10
RX_REFCLK_N	B1	U1_J1_RX_REFCLK_N	Y9
RX_FC_CK	E10	U1_AMR1_FC_CK	AK32
RX8_P	G5	U1_MGTRX3_113_C_P	AE7
RX8_N	H5	U1_MGTRX3_113_C_N	AE8
RX9_P	G3	U1_MGTRX1_113_C_P	AG7
RX9_N	H3	U1_MGTRX1_113_C_N	AG8

Table 1-13: **U1 FPGA FCI Connector J1 *(Cont'd)***

FCI Connector J1		Net Name	U1 FPGA Pin Number
Pin Name	Pin Number		
RX10_P	J4	U1_MGTRX2_113_C_P	AF5
RX10_N	K4	U1_MGTRX2_113_C_N	AF6
RX11_P	G1	U1_MGTRX0_113_C_P	AH5
RX11_N	H1	U1_MGTRX0_113_C_N	AH6
RX12_P	J6	NC	
RX12_N	K6	NC	
RX13_P	J10	NC	
RX13_N	K10	NC	
RX14_P	J2	NC	
RX14_N	K2	NC	
RX15_P	J8	NC	
RX15_N	K8	NC	
RX_FC_DATA	H7	U1_AMR1_FC_DATA	BA34
RX_FC_SYNC	H9	U1_AMR1_FC_SYNC	AL34

Table 1-14: **U1 FPGA FCI Connector P2**

FCI Connector P2		Net Names	U1 FPGA Pin Number
Pin Names	Pin Number		
TX0_P	A7	U1_MGTTX1_101_P	AT44
TX0_N	B7	U1_MGTTX1_101_N	AT43
TX1_P	D6	U1_MGTTX0_101_P	AU42
TX1_N	E6	U1_MGTTX0_101_N	AU41
TX2_P	D8	U1_MGTTX2_101_P	AR42
TX2_N	E8	U1_MGTTX2_101_N	AR41
TX3_P	A9	U1_MGTTX3_101_P	AP44
TX3_N	B9	U1_MGTTX3_101_N	AP43
TX4_P	A3	U1_MGTTX0_100_P	BB44
TX4_N	B3	U1_MGTTX0_100_N	BB43
TX5_P	D2	U1_MGTTX2_100_P	AW42
TX5_N	E2	U1_MGTTX2_100_N	AW41
TX6_P	D4	U1_MGTTX1_100_P	AY44
TX6_N	E4	U1_MGTTX1_100_N	AY43

Table 1-14: **U1 FPGA FCI Connector P2 *(Cont'd)***

FCI Connector P2		Net Names	U1 FPGA Pin Number
Pin Names	Pin Number		
TX7_P	A5	U1_MGTTX3_100_P	AV44
TX7_N	B5	U1_MGTTX3_100_N	AV43
TX_REFCLK_P	A1	U1_P2_TX_REFCLK_C_P	U13.19
TX_REFCLK_N	B1	U1_P2_TX_REFCLK_C_N	U13.20
TX_FC_CK	E10	U1_AMH2_FC_CK	J30
TX8_P	G5	U1_MGTTX2_102_P	AL42
TX8_N	H5	U1_MGTTX2_102_N	AL41
TX9_P	G3	U1_MGTTX0_102_P	AN42
TX9_N	H3	U1_MGTTX0_102_N	AN41
TX10_P	J4	U1_MGTTX3_102_P	AK44
TX10_N	K4	U1_MGTTX3_102_N	AK43
TX11_P	G1	U1_MGTTX1_102_P	AM44
TX11_N	H1	U1_MGTTX1_102_N	AM43
TX12_P	J6	U1_AMH2_IO0	AV21
TX12_N	K6	U1_AMH2_IO1	AU21
TX13_P	J10	U1_AMH2_IO2	AN22
TX13_N	K10	U1_AMH2_IO3	AN23
TX14_P	J2	U1_AMH2_IO4	AY21
TX14_N	K2	U1_AMH2_IO5	AU20
TX15_P	J8	U1_AMH2_IO6	AT20
TX15_N	K8	U1_AMH2_IO7	AP21
TX_FC_DATA	H7	U1_AMH2_FC_DATA	K30
TX_FC_SYNC	H9	U1_AMH2_FC_SYNC	T30

Table 1-15: **U1 FPGA FCI Connector J2**

FCI Connector J2		Net Names	U1 FPGA Pin Number
Pin Names	Pin Number		
RX0_P	A7	U1_MGTRX1_101_C_P	AV40
RX0_N	B7	U1_MGTRX1_101_C_N	AV39
RX1_P	D6	U1_MGTRX0_101_C_P	AY40
RX1_N	E6	U1_MGTRX0_101_C_N	AY39
RX2_P	D8	U1_MGTRX2_101_C_P	AT40

Table 1-15: **U1 FPGA FCI Connector J2 *(Cont'd)***

FCI Connector J2		Net Names	U1 FPGA Pin Number
Pin Names	Pin Number		
RX2_N	E8	U1_MGTRX2_101_C_N	AT39
RX3_P	A9	U1_MGTRX3_101_C_P	AP40
RX3_N	B9	U1_MGTRX3_101_C_N	AP39
RX4_P	A3	U1_MGTRX0_100_C_P	BD40
RX4_N	B3	U1_MGTRX0_100_C_N	BD39
RX5_P	D2	U1_MGTRX2_100_C_P	BB40
RX5_N	E2	U1_MGTRX2_100_C_N	BB39
RX6_P	D4	U1_MGTRX1_100_C_P	BC42
RX6_N	E4	U1_MGTRX1_100_C_N	BC41
RX7_P	A5	U1_MGTRX3_100_C_P	BA42
RX7_N	B5	U1_MGTRX3_100_C_N	BA41
RX_REFCLK_P	A1	U1_J2_RX_REFCLK_P	AR37
RX_REFCLK_N	B1	U1_J2_RX_REFCLK_N	AR38
RX_FC_CK	E10	U1_AMR2_FC_CK	T29
RX8_P	G5	U1_MGTRX2_102_C_P	AJ38
RX8_N	H5	U1_MGTRX2_102_C_N	AJ37
RX9_P	G3	U1_MGTRX0_102_C_P	AL38
RX9_N	H3	U1_MGTRX0_102_C_N	AL37
RX10_P	J4	U1_MGTRX3_102_C_P	AK40
RX10_N	K4	U1_MGTRX3_102_C_N	AK39
RX11_P	G1	U1_MGTRX1_102_C_P	AM40
RX11_N	H1	U1_MGTRX1_102_C_N	AM39
RX12_P	J6	NC	
RX12_N	K6	NC	
RX13_P	J10	NC	
RX13_N	K10	NC	
RX14_P	J2	NC	
RX14_N	K2	NC	
RX15_P	J8	NC	
RX15_N	K8	NC	
RX_FC_DATA	H7	U1_AMR2_FC_DATA	G32
RX_FC_SYNC	H9	U1_AMR2_FC_SYNC	M32