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VC707 Evaluation Board for the Virtex-7 FPGA

User Guide

UG885 (v1.7.1) August 12, 2016

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/05/12	1.0	Initial Xilinx release.
10/08/12	1.1	Chapter 1, VC707 Evaluation Board Features: In Table 1-1, notes for J37 changed to Samtec ASP_134486_01. The board photo in Figure 1-2 was replaced. In Table 1-3, GPGA (U1) Bank 32 was deleted. A note was added about the user clock for Figure 1-10. In Table 1-15, FPGA pin AN1 changed to AM4 and pin AN2 changed to AM3. In SGMII GTX Transceiver Clock Generation, page 42, 25 MHz LVDS clock changed to 125 MHz LVDS clock. The Figure 1-10 title also changed from 25 MHz to 125 MHz. In Table 1-23, pin AR42 changed to AT42. In Figure 1-33, switching regulator supply voltage UG63 for MGTVCCAUX was updated. In Table 1-29, device type PTD08D021W (V_{OUT} A) power rail voltage changed to 1.80V. In Table 1-32, values for rail number 3 changed. In Appendix C, Master Constraints File Listing, the entire listing was replaced. Appendix G, Regulatory and Compliance Information now includes a link to the Declaration of Conformity and markings for waste electrical and electronic equipment (WEEE), restriction of hazardous substances (RoHS), and CE compliance.

Date	Version	Revision
02/01/13	1.2	Updated VC707 Board Features, Table 1-1, Virtex-7 XC7VX485T-2FFG1761C FPGA, FPGA Configuration, USB JTAG, System Clock (SYSCLK_P and SYSCLK_N), HDMI Video Output, I2C Bus, Table 1-15, User I/O, Table 1-26, Power Management, and VITA 57.1 FMC2 HPC Connector (Partially Populated). Updated Figure 1-5, Figure 1-16, and Figure 1-25. Updated paragraph following Table 1-4, Figure 1-7, Figure 1-19, Figure 1-20, and Table 1-24. Added CPU Reset Pushbutton, User Rotary Switch, User SMA, and PCIe Form Factor Board TI Power System Cooling. Added Table 1-27 and Table 1-28. Replaced PTD08D021W with PTD08D210W in Table 1-29. Added third paragraph to the introduction in Appendix C, Master Constraints File Listing. Added UG483 and removed NXP Semiconductors in Appendix F, Additional Resources. Added second paragraph to the introduction in Appendix G, Regulatory and Compliance Information.
08/22/13	1.3	Updated Figure 1-2, Table 1-1, Table 1-12, Table 1-13, and Table 1-14. Updated Linear BPI Flash Memory. Replaced Master UCF Listing with Appendix C, Master Constraints File Listing.
05/12/14	1.4	Updated disclaimer and copyright. In Table 1-27, changed U1 FPGA pin N39 to M39, B36 to A35, and B37 to A36.
09/20/14	1.5	Added note to Table 1-1 and Table 1-27. Updated Table 1-7. Changed Net Name column heading to FHG1761 Placement in Table 1-11. Added I/O standard information to Table 1-4, Table 1-5, Table 1-8, Table 1-10, Table 1-18, Table 1-21, Table 1-23, Table 1-26, Table 1-27 and Table 1-28. Updated schematic net name for pins C34 and D35 in Table 1-27 and Table 1-28. Updated GTX Transceivers. Added Figure A-3.
04/07/15	1.6	Added notes to Jitter Attenuated Clock and I2C Bus. Updated Table 1-24. Deleted redundant Figure B-2 FMC2 HPC Connector Pinout in Appendix B, VITA 57.1 FMC Connector Pinouts. Added information for ordering the ATX power supply adapter cable.
09/01/15	1.6.1	Made typographical edits.
03/26/16	1.7	Updated transceiver bank MGT_BANK_119 in Table 1-11. Updated GPIO pin for CPU reset pushbutton switch in Table 1-26. Updated U1 FPGA pins for J37 FMC2 HPC pins B12, B13, B32, and B33 in Table 1-28. Added thickness information in Appendix E, Board Specifications.
08/12/16	1.7.1	Made a typographical edit.

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Appendix D: Board Setup

Appendix E: Board Specifications

Appendix F: Additional Resources

Appendix G: Regulatory and Compliance Information

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Chapter 1

VC707 Evaluation Board Features

Overview

The VC707 evaluation board for the Virtex®-7 FPGA provides a hardware environment for developing and evaluating designs targeting the Virtex-7 XC7VX485T-2FFG1761C FPGA. The VC707 board provides features common to many embedded processing systems, including a DDR3 SODIMM memory, an 8-lane PCI Express® interface, a tri-mode Ethernet PHY, general purpose I/O, and two UART interfaces. Other features can be added by using mezzanine cards attached to either of two VITA-57 FPGA mezzanine connectors (FMC) provided on the board. Two high pin count (HPC) FMCs are provided. See VC707 Board Features for a complete list of features. The details for each feature are described in Feature Descriptions, page 10.

Additional Information

See Appendix F, Additional Resources for references to documents, files and resources relevant to the VC707 board.

VC707 Board Features

- Virtex-7 XC7VX485T-2FFG1761C FPGA
- 1 GB DDR3 memory SODIMM
- 128 MB Linear byte peripheral interface (BPI) Flash memory
- USB 2.0 ULPI Transceiver
- Secure Digital (SD) connector
- USB JTAG through Digilent module
- Clock Generation
  - Fixed 200 MHz LVDS oscillator (differential)
  - I^2C programmable LVDS oscillator (differential)
  - SMA connectors (differential)
  - SMA connectors for GTX transceiver clocking
- GTX transceivers
  - FMC1 HPC connector (eight GTX transceivers)
  - FMC2 HPC connector (eight GTX transceiver)
  - SMA connectors (one pair each for TX, RX, and REFCLK)
  - PCI Express (eight lanes)
  - Small form-factor pluggable plus (SFP+) connector

- Ethernet PHY SGMII interface (RJ-45 connector)
- PCI Express endpoint connectivity
  - Gen1 8-lane (x8)
  - Gen2 8-lane (x8)
- SFP+ Connector
- 10/100/1000 tri-speed Ethernet PHY
- USB-to-UART bridge
- HDMI™ codec
- I^2C bus
  - I^2C MUX
  - I^2C EEPROM (1 KB)
  - USER I^2C programmable LVDS oscillator
  - DDR3 SODIMM socket
  - HDMI codec
  - FMC1 HPC connector
  - FMC2 HPC connector
  - SFP+ connector
  - I^2C programmable jitter-attenuating precision clock multiplier
- Status LEDs
  - Ethernet status
  - Power good
  - FPGA INIT
  - FPGA DONE
- User I/O
  - User LEDs (eight GPIO)
  - User pushbuttons (five directional)
  - CPU reset pushbutton
  - User DIP switch (8-pole GPIO)
  - User SMA GPIO connectors (one pair)
  - LCD character display (16 characters x 2 lines)
- Switches
  - Power on/off slide switch
  - FPGA_PROB_B pushbutton
  - Configuration mode DIP switch
- VITA 57.1 FMC1 HPC Connector
- VITA 57.1 FMC2 HPC Connector
- Power management
  - PMBus voltage and current monitoring through TI power controller
- XADC header
- Configuration options

- Linear BPI Flash memory
- USB JTAG configuration port
- Platform cable header JTAG configuration port

The VC707 board block diagram is shown in Figure 1-1. The VC707 board schematics are available for download from the VC707 Evaluation Kit product page on the Docs & Designs tab at www.xilinx.com/vc707.

Caution! The VC707 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

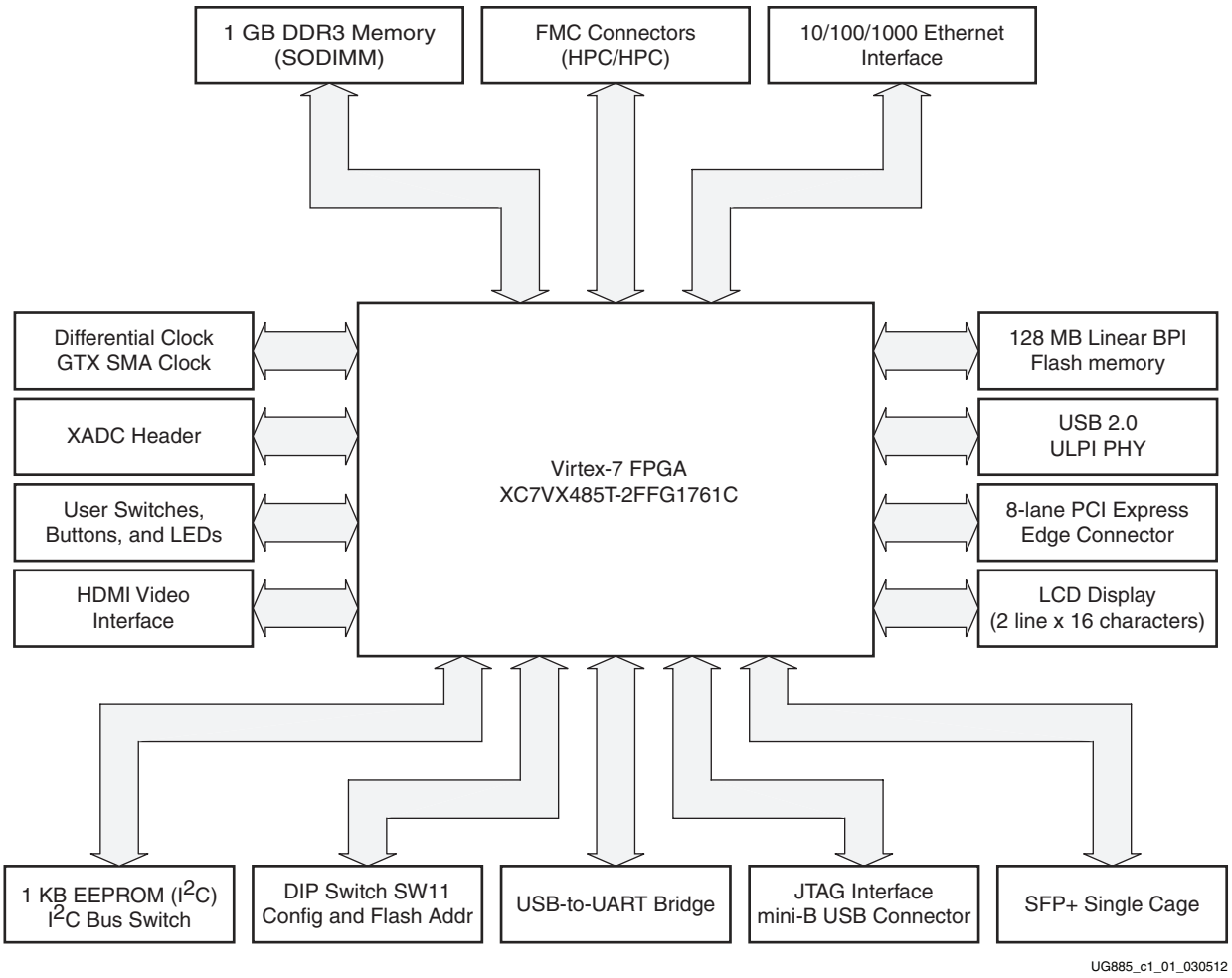

Figure 1-1: **VC707 Board Block Diagram**

Feature Descriptions

Figure 1-2 shows the VC707 board. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Note: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

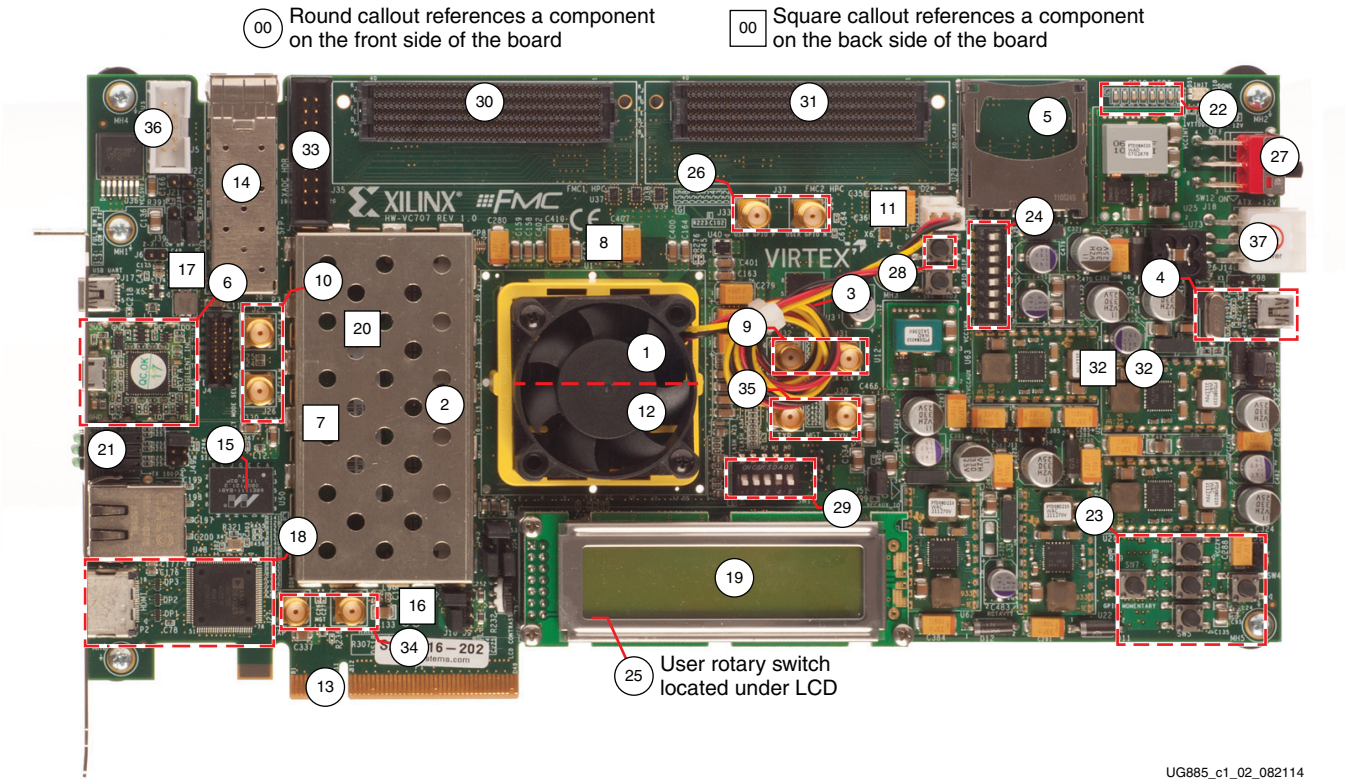

Figure 1-2: **VC707 Board Component Locations**

Table 1-1: **VC707 Board Component Descriptions**

Callout	Reference Designator	Component Description	Notes	Schematic 0381418 Page Number
1	U1	Virtex-7 FPGA with cooling fan	XC7VX485T-2FFG1761C	
2	J1	DDR3 SODIMM memory (1 GB)	Micron MT8JTF12864HZ-1G6G1	21
3	U3	BPI parallel NOR flash memory (1 Gb)	Micron PC28F00AG18FE	35
4	U8, J2	USB ULPI transceiver, USB mini-B connector	SMSC USB3320-EZK	44
5	U29	SD card interface connector	Molex 67840-8001	37
6	U26	USB JTAG interface, USB micro-B connector	Digilent USB JTAG module	20
7	U51	System clock, 200 MHz, LVDS (back side of board)	SiTime SIT9102-243N25E200.0000	32

Table 1-1: **VC707 Board Component Descriptions *(Cont'd)***

Callout	Reference Designator	Component Description	Notes	Schematic 0381418 Page Number
8	U34	I2C programmable user clock LVDS, 156.250 MHz default frequency (back side of board)	Silicon Labs SI570BAB0000544DG	32
9	J31, J32	User SMA clock	Rosenberger 32K10K-400L5	32
10	J25, J26	GTX transceiver SMA reference clock	Rosenberger 32K10K-400L5	32
11	U24	Jitter attenuated clock (back side of board)	Silicon Labs SI5324C-C-GM	33
12		GTX transceiver Quad 111 – Quad 119	Embedded within FPGA U1	12 – 15
13	P1	PCI Express connector	8-lane card edge connector	30
14	P3	SFP/SFP+ module connector	Molex 74441-0010	31
15	U50	10/100/1000 Mb/s Ethernet PHY	Marvell M88E1111-BAB1C000	34
16	U2	SGMII GTX transceiver clock generator	ICS ICS84402IAGI-01LF	32
17	U44	USB-to-UART bridge	Silicon Labs CP2103GM	36
18	P2, U48	HDMI video connector, HDMI controller	Molex 500254-1927, AD ADV7511KSTZ-P	43, 42
19	J23	LCD character display and connector	2 x 7 0.1 inch male header	39
20	U52	I2C Bus Switch (back side of board)	TI PCA9548ARGER	41
21	DS11–DS13	Ethernet status LEDs	EPHY status LED, dual green	34
22	DS2–DS9	User LEDs	GPIO LEDs, green 0603	38
23	SW3–SW7	User pushbuttons, active-High	E-Switch TL3301EP100QG	38
24	SW2	User DIP Switch	8-pole C and K SDA08H1SBD	38
25	SW10	User rotary switch (under LCD assembly)	Panasonic EVQ-WK4001	38
26	J33, J34	User SMA GPIO	Rosenberger 32K10K-400L5	32
27	SW12	Power on/off switch	C&K 1201M2S3AQE2	45
28	SW9	FPGA PROG pushbutton	E-Switch TL3301EP100QG	38
29	SW11	Config mode/upper linear flash address dip switch	5-pole C&K SDA05H1IBD	36
30	J35	FMC HPC1 connector (J35)	Samtec ASP_134486_01	22–25
31	J37	FMC HPC2 connector (J37)	Samtec ASP_134486_01	26–29
32		Power management system (front and back side of board)	TI UCD9248PFC in conjunction with various regulators	45–55
33	J19	Xilinx XADC header	2 x 10 0.1inch male header	40
34	J27, J28	GTX receiver SMA (RX)	Rosenberger 32K10K-400L5	32
35	J29/J30	GTX transmitter SMA (TX)	Rosenberger 32K10K-400L5	32
36	J5	2 x 5 shrouded PMBus connector	Assman HW10G-0202	46
37	J18	12V power input 2 x 3 connector	Molex 39-30-1060	46

Notes:
1. Jumper header locations are identified in Appendix A, Default Switch and Jumper Settings.

Virtex-7 XC7VX485T-2FFG1761C FPGA

[Figure 1-2, callout 1]

The VC707 board is populated with the Virtex-7 XC7VX485T-2FFG1761C FPGA.

For further information on Virtex-7 FPGAs, see *7 Series FPGAs Overview* (DS180) [Ref 1], and *7 Series FPGAs Packaging and Pinout Product Specifications User Guide* (UG475) [Ref 13].

To determine the type of FPGA resident on the VC707 board, refer to the Master Answer Record listed in Appendix F: References.

FPGA Configuration

The VC707 board supports two of the five 7 series FPGA configuration modes:

- Master BPI using the onboard Linear BPI Flash memory
- JTAG using a type-A to micro-B USB cable for connecting the host PC to the VC707 board configuration port

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in Table 1-2. The mode switches M2, M1, and M0 are on SW11 positions 3, 4, and 5 respectively as shown in Figure 1-3.

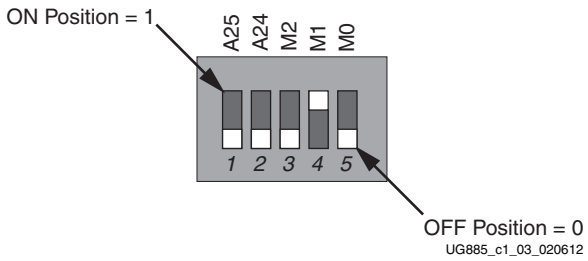

Figure 1-3: **SW11 Default Settings**

The default mode setting is M[2:0] = 010, which selects Master BPI at board power-on. See Configuration Options, page 77 for detailed information about the mode switch SW11.

Table 1-2: **VC707 Board FPGA Configuration Modes**

Configuration Mode	SW13 DIP switch Settings (M[2:0])	Bus Width	CCLK Direction
Master BPI	010	x8, x16	Output
JTAG	101	x1	Not Applicable

For full details on configuring the FPGA, see *7 Series FPGAs Configuration User Guide* (UG470) [Ref 2].

I/O Voltage Rails

There are 17 I/O banks available on the Virtex-7 device. Sixteen I/O banks are available on the VC707 board, bank 31 is not used. The voltages applied to the FPGA I/O banks used by the VC707 board are listed in Table 1-3.

Table 1-3: **I/O Voltage Rails**

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
Bank 0	VCC1V8_FPGA	1.8V
Bank 13	VCC1V8_FPGA	1.8V
Bank 14	VCC1V8_FPGA	1.8V
Bank 15	VCC1V8_FPGA	1.8V
Bank 16(1)	VADJ_FPGA	1.8V (default)
Bank 17(1)	VADJ_FPGA	1.8V (default)
Bank 18(1)	VADJ_FPGA	1.8V (default)
Bank 19(1)	VADJ_FPGA	1.8V (default)
Bank 31	NOT USED	NA
Bank 33	VCC1V8_FPGA	1.8V
Bank 34	VADJ_FPGA	1.8V (default)
Bank 35	VADJ_FPGA	1.8V (default)
Bank 36	FMC1_VIO_B_M2C	Variable
Bank 37	VCC1V5_FPGA	1.5V
Bank 38	VCC1V5_FPGA	1.5V
Bank 39	VCC1V5_FPGA	1.5V

Notes:

1. The VADJ_FPGA rail can support up to 1.8V due to FPGA HP bank connections to FMC. For more information on VADJ_FPGA see Power Management, page 70.

DDR3 Memory

[Figure 1-2, callout 2]

The memory module at J1 is a 1 GB DDR3 small outline dual-inline memory module (SODIMM). It provides volatile synchronous dynamic random access memory (SDRAM) for storing user code and data.

- Part number: MT8JTF12864HZ-1G6G1 (Micron Technology)
- Supply voltage: 1.5V
- Datapath width: 64 bits
- Data rate: Up to 1,600 MT/s

The DDR3 interface is implemented across I/O banks 37, 38, and 39. Each bank is a 1.5V high-performance bank having a dedicated DCI VRP/N resistor connection. An external 0.75V reference VTTREF is provided for data interface banks 37 and 39. Any interface connected to these banks that requires a reference voltage must use this FPGA voltage reference. The connections between the DDR3 memory and the FPGA are listed in Table 1-4.

Table 1-4: **DDR3 Memory Connections to the FPGA**

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
A20	DDR3_A0	SSTL15	98	A0
B19	DDR3_A1	SSTL15	97	A1
C20	DDR3_A2	SSTL15	96	A2
A19	DDR3_A3	SSTL15	95	A3
A17	DDR3_A4	SSTL15	92	A4
A16	DDR3_A5	SSTL15	91	A5
D20	DDR3_A6	SSTL15	90	A6
C18	DDR3_A7	SSTL15	86	A7
D17	DDR3_A8	SSTL15	89	A8
C19	DDR3_A9	SSTL15	85	A9
B21	DDR3_A10	SSTL15	107	A10/AP
B17	DDR3_A11	SSTL15	84	A11
A15	DDR3_A12	SSTL15	83	A12_BC_N
A21	DDR3_A13	SSTL15	119	A13
F17	DDR3_A14	SSTL15	80	A14
E17	DDR3_A15	SSTL15	78	A15
D21	DDR3_BA0	SSTL15	109	BA0
C21	DDR3_BA1	SSTL15	108	BA1
D18	DDR3_BA2	SSTL15	79	BA2
N14	DDR3_D0	SSTL15	5	DQ0

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
N13	DDR3_D1	SSTL15	7	DQ1
L14	DDR3_D2	SSTL15	15	DQ2
M14	DDR3_D3	SSTL15	17	DQ3
M12	DDR3_D4	SSTL15	4	DQ4
N15	DDR3_D5	SSTL15	6	DQ5
M11	DDR3_D6	SSTL15	16	DQ6
L12	DDR3_D7	SSTL15	18	DQ7
K14	DDR3_D8	SSTL15	21	DQ8
K13	DDR3_D9	SSTL15	23	DQ9
H13	DDR3_D10	SSTL15	33	DQ10
J13	DDR3_D11	SSTL15	35	DQ11
L16	DDR3_D12	SSTL15	22	DQ12
L15	DDR3_D13	SSTL15	24	DQ13
H14	DDR3_D14	SSTL15	34	DQ14
J15	DDR3_D15	SSTL15	36	DQ15
E15	DDR3_D16	SSTL15	39	DQ16
E13	DDR3_D17	SSTL15	41	DQ17
F15	DDR3_D18	SSTL15	51	DQ18
E14	DDR3_D19	SSTL15	53	DQ19
G13	DDR3_D20	SSTL15	40	DQ20
G12	DDR3_D21	SSTL15	42	DQ21
F14	DDR3_D22	SSTL15	50	DQ22
G14	DDR3_D23	SSTL15	52	DQ23
B14	DDR3_D24	SSTL15	57	DQ24
C13	DDR3_D25	SSTL15	59	DQ25
B16	DDR3_D26	SSTL15	67	DQ26
D15	DDR3_D27	SSTL15	69	DQ27
D13	DDR3_D28	SSTL15	56	DQ28
E12	DDR3_D29	SSTL15	58	DQ29
C16	DDR3_D30	SSTL15	68	DQ30
D16	DDR3_D31	SSTL15	70	DQ31
A24	DDR3_D32	SSTL15	129	DQ32

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
B23	DDR3_D33	SSTL15	131	DQ33
B27	DDR3_D34	SSTL15	141	DQ34
B26	DDR3_D35	SSTL15	143	DQ35
A22	DDR3_D36	SSTL15	130	DQ36
B22	DDR3_D37	SSTL15	132	DQ37
A25	DDR3_D38	SSTL15	140	DQ38
C24	DDR3_D39	SSTL15	142	DQ39
E24	DDR3_D40	SSTL15	147	DQ40
D23	DDR3_D41	SSTL15	149	DQ41
D26	DDR3_D42	SSTL15	157	DQ42
C25	DDR3_D43	SSTL15	159	DQ43
E23	DDR3_D44	SSTL15	146	DQ44
D22	DDR3_D45	SSTL15	148	DQ45
F22	DDR3_D46	SSTL15	158	DQ46
E22	DDR3_D47	SSTL15	160	DQ47
A30	DDR3_D48	SSTL15	163	DQ48
D27	DDR3_D49	SSTL15	165	DQ49
A29	DDR3_D50	SSTL15	175	DQ50
C28	DDR3_D51	SSTL15	177	DQ51
D28	DDR3_D52	SSTL15	164	DQ52
B31	DDR3_D53	SSTL15	166	DQ53
A31	DDR3_D54	SSTL15	174	DQ54
A32	DDR3_D55	SSTL15	176	DQ55
E30	DDR3_D56	SSTL15	181	DQ56
F29	DDR3_D57	SSTL15	183	DQ57
F30	DDR3_D58	SSTL15	191	DQ58
F27	DDR3_D59	SSTL15	193	DQ59
C30	DDR3_D60	SSTL15	180	DQ60
E29	DDR3_D61	SSTL15	182	DQ61
F26	DDR3_D62	SSTL15	192	DQ62
D30	DDR3_D63	SSTL15	194	DQ63
M13	DDR3_DM0	SSTL15	11	DM0

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
K15	DDR3_DM1	SSTL15	28	DM1
F12	DDR3_DM2	SSTL15	46	DM2
A14	DDR3_DM3	SSTL15	63	DM3
C23	DDR3_DM4	SSTL15	136	DM4
D25	DDR3_DM5	SSTL15	153	DM5
C31	DDR3_DM6	SSTL15	170	DM6
F31	DDR3_DM7	SSTL15	187	DM7
M16	DDR3_DQS0_N	DIFF_SSTL15	10	DQS0_N
N16	DDR3_DQS0_P	DIFF_SSTL15	12	DQS0_P
J12	DDR3_DQS1_N	DIFF_SSTL15	27	DQS1_N
K12	DDR3_DQS1_P	DIFF_SSTL15	29	DQS1_P
G16	DDR3_DQS2_N	DIFF_SSTL15	45	DQS2_N
H16	DDR3_DQS2_P	DIFF_SSTL15	47	DQS2_P
C14	DDR3_DQS3_N	DIFF_SSTL15	62	DQS3_N
C15	DDR3_DQS3_P	DIFF_SSTL15	64	DQS3_P
A27	DDR3_DQS4_N	DIFF_SSTL15	135	DQS4_N
A26	DDR3_DQS4_P	DIFF_SSTL15	137	DQS4_P
E25	DDR3_DQS5_N	DIFF_SSTL15	152	DQS5_N
F25	DDR3_DQS5_P	DIFF_SSTL15	154	DQS5_P
B29	DDR3_DQS6_N	DIFF_SSTL15	169	DQS6_N
B28	DDR3_DQS6_P	DIFF_SSTL15	171	DQS6_P
E28	DDR3_DQS7_N	DIFF_SSTL15	186	DQS7_N
E27	DDR3_DQS7_P	DIFF_SSTL15	188	DQS7_P
H20	DDR3_ODT0	SSTL15	116	ODT0
H18	DDR3_ODT1	SSTL15	120	ODT1
C29	DDR3_RESET_B	LVCMOS15	30	RESET_B
J17	DDR3_S0_B	SSTL15	114	S0_B
J20	DDR3_S1_B	SSTL15	121	S1_B
G17	DDR3_TEMP_EVENT	SSTL15	198	EVENT_B
F20	DDR3_WE_B	SSTL15	113	WE_B
K17	DDR3_CAS_B	SSTL15	115	CAS_B
E20	DDR3_RAS_B	SSTL15	110	RAS_B

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
K19	DDR3_CKE0	SSTL15	73	CKE0
J18	DDR3_CKE1	SSTL15	74	CKE1
G18	DDR3_CLK0_N	DIFF_SSTL15	103	CK0_N
H19	DDR3_CLK0_P	DIFF_SSTL15	101	CK0_P
F19	DDR3_CLK1_N	DIFF_SSTL15	104	CK1_N
G19	DDR3_CLK1_P	DIFF_SSTL15	102	CK1_P

The VC707 DDR3 SODIMM interface adheres to the constraints guidelines in the DDR3 *Design Guidelines* section of *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 3]. The VC707 DDR3 SODIMM interface is a 40Ω impedance implementation. Other memory interface details are available in UG586 and *7 Series FPGAs Memory Resources User Guide* (UG473) [Ref 4]. For more details on the DDR3 SODIMM, see the Micron Semiconductor MT8JTF12864HZ-1G6G1 data sheet [Ref 16].

Linear BPI Flash Memory

[Figure 1-2, callout 3]

The Linear BPI Flash memory located at U3 provides 128 MB of nonvolatile storage that can be used for configuration or software storage. The data, address, and control signals are connected to the FPGA. The BPI Flash memory device is packaged in a 64-pin BGA.

- Part number: PC28F00AG18FE (Micron)
- Supply voltage: 1.8V
- Datapath width: 16 bits (26 address lines and 7 control signals)
- Data rate: Up to 80 MHz

The Linear BPI Flash memory can synchronously configure the FPGA in Master BPI mode at the 80 MHz data rate supported by the PC28F00AG18FE flash memory. The fastest configuration method uses the external 80 MHz oscillator connected to the FPGA's EMCCLK pin.

Multiple bitstreams can be stored in the Linear BPI Flash. The two most significant address bits (A25, A24) of the flash memory are connected to DIP switch SW11 positions 1 and 2 respectively, and to the RS1 and RS0 pins of the FPGA. By placing valid XC7VX485T bitstreams at four different offset addresses in the flash memory, 1 of the 4 bitstreams can be selected to configure the FPGA by appropriately setting the DIP switch SW11. The connections between the BPI Flash memory and the FPGA are listed in Table 1-5.

Table 1-5: **BPI Flash Memory Connections to the FPGA**

FPGA (U1) Pin	Net Name	I/O Standard	BPI Flash Memory (U3)	
			Pin Number	Pin Name
AJ28	FLASH_A0	LVCMOS18	A1	A1
AH28	FLASH_A1	LVCMOS18	B1	A2

Table 1-5: **BPI Flash Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	BPI Flash Memory (U3)	
			Pin Number	Pin Name
AG31	FLASH_A2	LVCMOS18	C1	A3
AF30	FLASH_A3	LVCMOS18	D1	A4
AK29	FLASH_A4	LVCMOS18	D2	A5
AK28	FLASH_A5	LVCMOS18	A2	A6
AG29	FLASH_A6	LVCMOS18	C2	A7
AK30	FLASH_A7	LVCMOS18	A3	A8
AJ30	FLASH_A8	LVCMOS18	B3	A9
AH30	FLASH_A9	LVCMOS18	C3	A10
AH29	FLASH_A10	LVCMOS18	D3	A11
AL30	FLASH_A11	LVCMOS18	C4	A12
AL29	FLASH_A12	LVCMOS18	A5	A13
AN33	FLASH_A13	LVCMOS18	B5	A14
AM33	FLASH_A14	LVCMOS18	C5	A15
AM32	FLASH_A15	LVCMOS18	D7	A16
AV41	FLASH_A16	LVCMOS18	D8	A17
AU41	FLASH_A17	LVCMOS18	A7	A18
BA42	FLASH_A18	LVCMOS18	B7	A19
AU42	FLASH_A19	LVCMOS18	C7	A20
AT41	FLASH_A20	LVCMOS18	C8	A21
BA40	FLASH_A21	LVCMOS18	A8	A22
BA39	FLASH_A22	LVCMOS18	G1	A23
BB39	FLASH_A23	LVCMOS18	H8	A24
AW42	FLASH_A24	LVCMOS18	B6	A25
AW41	FLASH_A25	LVCMOS18	B8	A26
NA	NC	NA	H1	A27
AM36	FLASH_D0	LVCMOS18	F2	DQ0
AN36	FLASH_D1	LVCMOS18	E2	DQ1
AJ36	FLASH_D2	LVCMOS18	G3	DQ2
AJ37	FLASH_D3	LVCMOS18	E4	DQ3
AK37	FLASH_D4	LVCMOS18	E5	DQ4
AL37	FLASH_D5	LVCMOS18	G5	DQ5
AN35	FLASH_D6	LVCMOS18	G6	DQ6

Table 1-5: **BPI Flash Memory Connections to the FPGA *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	BPI Flash Memory (U3)	
			Pin Number	Pin Name
AP35	FLASH_D7	LVCMOS18	H7	DQ7
AM37	FLASH_D8	LVCMOS18	E1	DQ8
AG33	FLASH_D9	LVCMOS18	E3	DQ9
AH33	FLASH_D10	LVCMOS18	F3	DQ10
AK35	FLASH_D11	LVCMOS18	F4	DQ11
AL35	FLASH_D12	LVCMOS18	F5	DQ12
AJ31	FLASH_D13	LVCMOS18	H5	DQ13
AH34	FLASH_D14	LVCMOS18	G7	DQ14
AJ35	FLASH_D15	LVCMOS18	E7	DQ15
AM34	FLASH_WAIT	LVCMOS18	F7	WAIT
BB41	FPGA_FWE_B	LVCMOS18	G8	WE_B
BA41	FLASH_OE_B	LVCMOS18	F8	OE_B
N10	FPGA_CCLK	LVCMOS18	E6	CLK
AL36	FLASH_CE_B	LVCMOS18	B4	CE_B
AY37	FLASH_ADV_B	LVCMOS18	F6	ADV_B
AG11	FPGA_INIT_B	LVCMOS18	D4	RST_B

Additional FPGA bitstreams can be stored and used for configuration by setting the Warm Boot Start Address (WBSTAR) register contained in 7 series FPGAs. More information is available in the reconfiguration and multiboot section in *7 Series FPGAs Configuration User Guide* (UG470) [Ref 2].

The configuration section of *7 Series FPGAs Configuration User Guide* (UG470) [Ref 2] provides details on the Master BPI configuration mode.

Figure 1-4 shows the connections of the linear BPI Flash memory on the VC707 board. For more details, see the Micron PC28F00AG18FE data sheet [Ref 16].

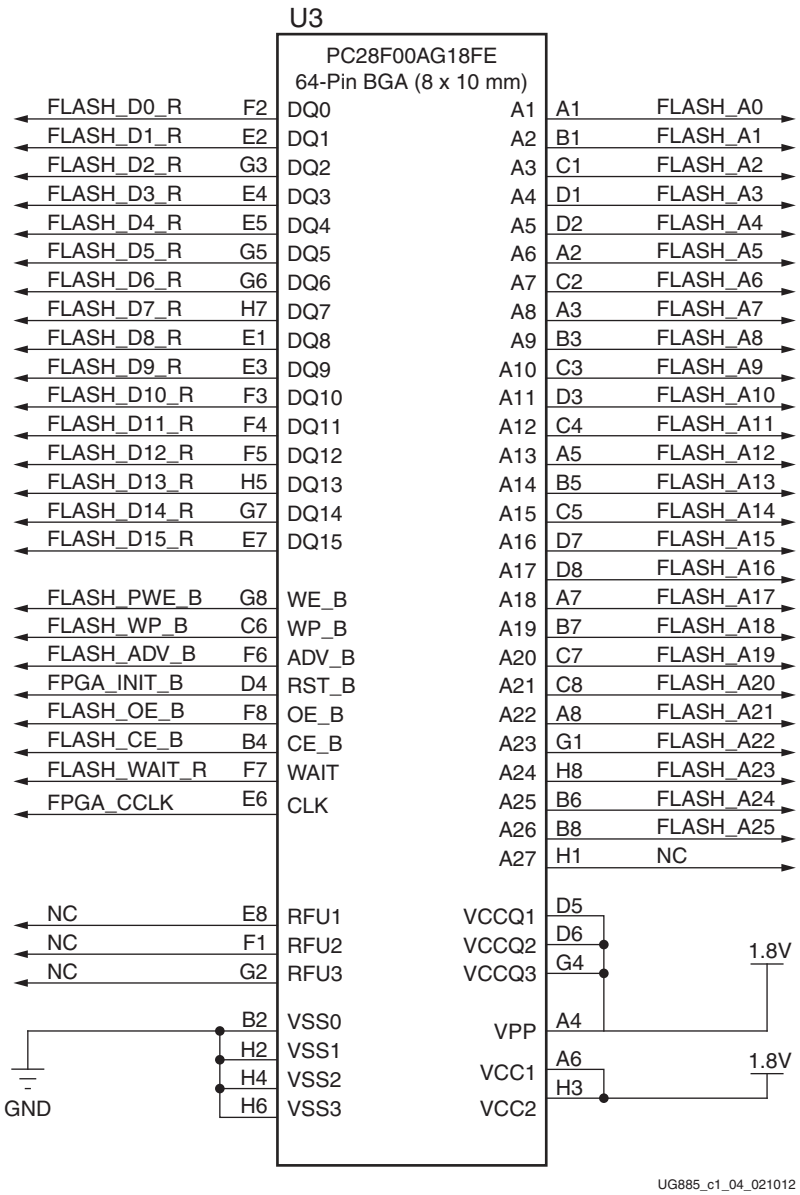

Figure 1-4: **128 MB Linear Flash Memory (U3)**

USB 2.0 ULPI Transceiver

[Figure 1-2, callout 4]

The VC707 board uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver (U8) to support a USB connection to the host computer. A USB cable is supplied in the VC707 Evaluation Kit (type-A connector to host computer, mini-B connector to VC707 board connector J2).

The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device which drives the physical USB bus. Use of the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

The USB3320 is clocked by a 24 MHz crystal. The ULPI interface supports two clocking modes selected by jumper on J14:

- 24 MHz ULPI output clock mode (default): No jumper on J14. The PHY drives the UPLI clock. This is the default setting.
- 60 MHz ULPI input clock mode: Jumper across J14 pins 1–2.

Consult the SMSC USB3320 data sheet for clocking mode details [Ref 17].

The FPGA interface to the USB3320 transceiver is implemented through the AXI universal serial bus 2.0 device IP. See *LogiCORE IP AXI Universal Serial Bus 2.0 Device Product Guide for Vivado Design Suite* (PG137) [Ref 5]

Note: The AXI universal serial bus 2.0 device IP supports USB-supplied power mode only. Jumpers on headers J13 and J45 must be configured to their default state as described here:

- J13 = jumper removed
- J45 = jumper across pins 1–2

Figure 1-5 shows the shield for the USB mini-B connector (J2) can be tied to GND by a jumper on header J44 pins 1–2 (default). The USB shield can optionally be connected through a capacitor to GND by installing a tantalum capacitor (body size C) at location C326 and jumping pins 2-3 on header J44.

The connections between the USB mini-B connector at J2 and the PHY at U8 are listed in Table 1-6.

Table 1-6: **USB Connector Pin Assignments and Signal Definitions Between J2 and U8**

USB Connector J2		Net Name	Description	USB3320 (U8) Pin
Pin	Name			
1	VBUS	USB_SMSC_VBUS	+5V from host system	22
2	D_N	USB_SMSC_HEADER_N	Bidirectional differential serial data (N-side)	19
3	D_P	USB_SMSC_HEADER_P	Bidirectional differential serial data (P-side)	18
4	GND	USB_SMC_GND	Signal ground	33

The connections between the USB 2.0 PHY at U8 and the FPGA are listed in Table 1-7.

Table 1-7: **USB 2.0 ULPI Transceiver Connections to the FPGA**

FPGA (U1) Pin	Net Name	I/O Standard	USB3320 (U8) Pin
AV36	USB_SMSC_DATA0	LVCMOS18	3
AW36	USB_SMSC_DATA1	LVCMOS18	4
BA34	USB_SMSC_DATA2	LVCMOS18	5
BB34	USB_SMSC_DATA3	LVCMOS18	6
BA36	USB_SMSC_DATA4	LVCMOS18	7
AT34	USB_SMSC_DATA5	LVCMOS18	9
AY35	USB_SMSC_DATA6	LVCMOS18	10
AW35	USB_SMSC_DATA7	LVCMOS18	13
BA35	USB_SMSC_NXT	LVCMOS18	2
BB36	USB_SMSC_RESET_B	LVCMOS18	27
BB32	USB_SMSC_STP	LVCMOS18	29
BB33	USB_SMSC_DIR	LVCMOS18	31
AV34	USB_SMSC_REFCLK_OPTION	LVCMOS18	26
AY32	USB_SMSC_CLKOUT	LVCMOS18	1

Figure 1-5 shows the USB 2.0 ULPI Transceiver circuitry.

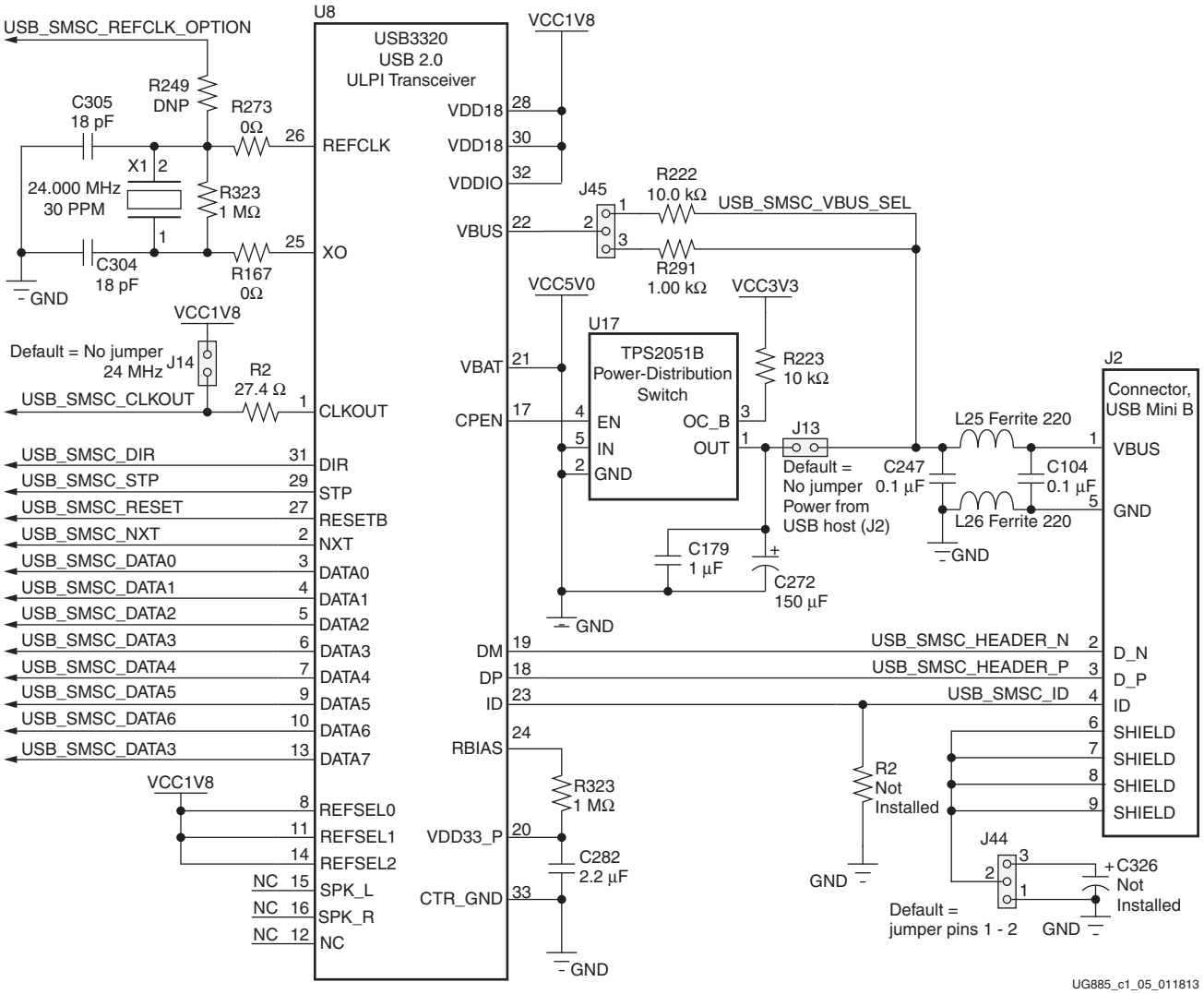

Figure 1-5: **USB 2.0 ULPI Transceiver**

SD Card Interface

[Figure 1-2, callout 5]

The VC707 board includes a secure digital input/output (SDIO) interface to provide user-logic access to general purpose nonvolatile SDIO memory cards and peripherals. The SD card slot is designed to support 50 MHz high speed SD cards.

The SDIO signals are connected to I/O bank 13 which has its VCCO set to 1.8V. A TI TXB0108 8-bit bidirectional voltage-level translator (U31) is used between the FPGA and the SD card connector (U29). Figure 1-6 shows the connections of the SD card interface on the VC707 board.

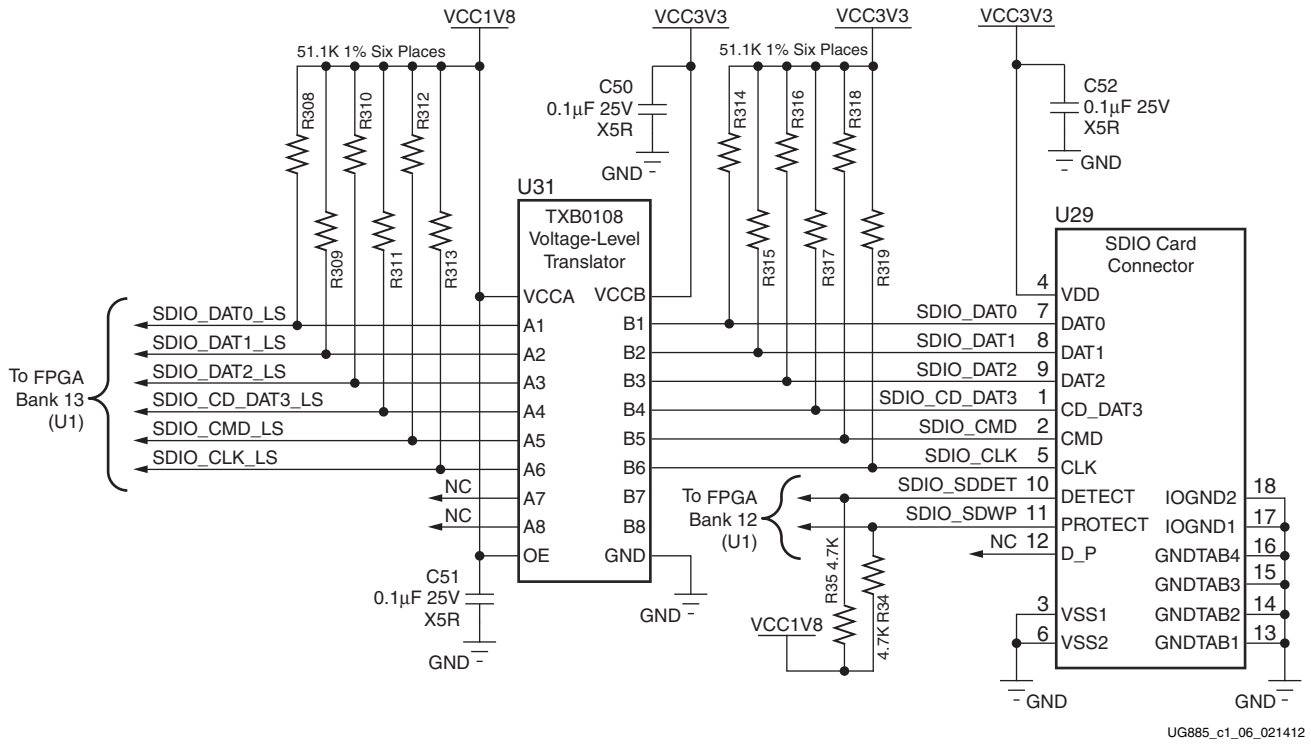

Figure 1-6: **SD Card Interface**

Table 1-8 lists the SD card interface connections to the FPGA.

Table 1-8: **SDIO Connections to the FPGA**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Level Shifter (U31)		SDIO Connector (U29)	
			Pin Number	Pin Name	Pin Number	Pin Name
AR32	SDIO_SDWP	LVCMOS18	N/A	N/A	11	SDWP
AP32	SDIO_SDDET	LVCMOS18	N/A	N/A	10	SDDET
AP30	SDIO_CMD_LS	LVCMOS18	6	A5	2	CMD
AN30	SDIO_CLK_LS	LVCMOS18	7	A6	5	CLK
AV31	SDIO_DAT2_LS	LVCMOS18	4	A3	9	DAT2
AU31	SDIO_DAT1_LS	LVCMOS18	3	A2	8	DAT1
AR30	SDIO_DAT0_LS	LVCMOS18	1	A1	7	DAT0
AT30	SDIO_CD_DAT3_LS	LVCMOS18	5	A4	1	CD_DAT3

USB JTAG

[Figure 1-2, callout 6]

JTAG configuration is provided through a Digilent onboard USB-to-JTAG configuration logic module (U26) where a host computer accesses the VC707 board JTAG chain through a type-A (host side) to micro-B (VC707 board side) USB cable.