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PE41901

Document Category: Product Specification

UltraCMOS® Image Reject Mixer, 10–19 GHz

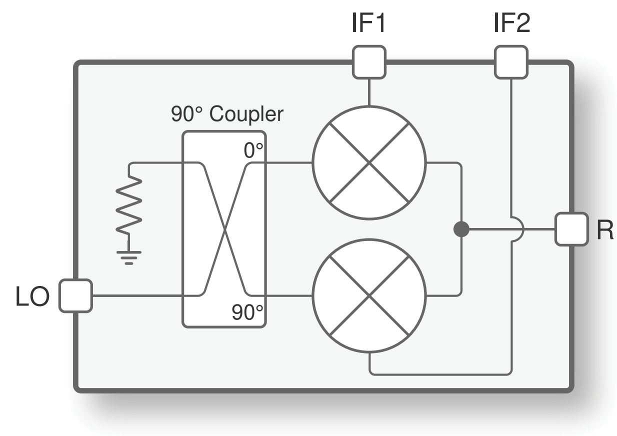
Features

- Complete MMIC mixer solution
- Double balanced high LO–RF isolation of 38 dB
- Conversion loss of 10 dB
- Image rejection of 25 dB
- Ku band coverage and broad IF frequency range support
- Packaging – 24-lead 4 × 4 × 0.85 mm QFN

Applications

- Very small aperture terminal (VSAT)
- Point-to-point communication system
- Test and measurement (T&M)

Figure 1 • ***PE41901 Functional Diagram***



Product Description

The PE41901 is a passive double balanced, Ku band image reject mixer with high dynamic range performance and high local oscillator (LO) isolation capable of operation up to 19 GHz. It can be used as an upconverter or a downconverter. The PE41901 operates with single-ended signals on the radio frequency (RF) and LO ports. The intermediate frequency (IF) port accepts broadband quadrature signals from DC–4 GHz. The device includes two mixers, an LO path 90° coupler and RF port baluns on a single die. Integrating this functionality on a single die reduces LO leakage and improves LO–RF isolation while minimizing board space and design effort. In addition, no external blocking capacitors are required if 0 VDC is present on the LO or RF pins.

The PE41901 image reject mixer is ideal for Ku band earth terminals such as very small aperture terminal (VSAT) block upconverters, point-to-point microwave links and test and measurement (T&M) applications.

The PE41901 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • ***Absolute Maximum Ratings for PE41901***

Parameter/Condition	Min	Max	Unit
RF input power, 50Ω		+10	dBm
IF input power, 50Ω		+10	dBm
LO input power, 50Ω		+25	dBm
Maximum junction temperature		+150	°C
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins(1)		250	V
ESD voltage CDM, all pins(2)		1000	V

Notes:
1) Human body model (MIL-STD 883 Method 3015).
2) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the PE41901. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • ***Recommended Operating Conditions for PE41901***

Parameter	Min	Typ	Max	Unit
RF input power, P_{RF}, 50Ω			+5	dBm
IF input power, P_{IF}, 50Ω			+5	dBm
LO input power, P_{LO}, 50Ω	+10		+20	dBm
Operating temperature range	–40	+25	+105	°C

Electrical Specifications

Table 3 provides the PE41901 key electrical specifications at +25 °C (Z = 50Ω), unless otherwise specified.

Table 3 • *PE41901 Electrical Specifications*

Parameter	Condition		Min	Typ	Max	Unit
RF frequency, f_{RF}			10		19	GHz
IF frequency, f_{IF}			DC		4	GHz
LO frequency, f_{LO}			12		19	GHz
Conversion loss	f_{RF} = 14 GHz P_{LO} = +17 dBm P_{IF} = –5 dBm	f_{IF} = 1 GHz, upper sideband (USB) and lower sideband (LSB) f_{IF} = 4 GHz, USB and LSB		10 11	11 12	dB dB
Image rejection[(1)]	f_{RF} = 14 GHz P_{LO} = +17 dBm P_{IF} = –5 dBm	f_{IF} = 1 GHz, USB f_{IF} = 1 GHz, LSB f_{IF} = 4 GHz, USB	22 17 20	25 20 22		dB dB dB
LO to RF isolation	f_{LO} = 12 GHz, P_{LO} = +17 dBm		35	38		dB
LO to IF isolation	f_{LO} = 12 GHz, P_{LO} = +17 dBm		20	23		dB
RF return loss	f_{RF} = 14 GHz, P_{LO} = +15 dBm, $P_{IF/RF}$ = 0 dBm			10		dB
IF return loss	f_{IF} = 1 GHz, P_{LO} = +15 dBm, $P_{IF/RF}$ = 0 dBm			10		dB
LO return loss	f_{LO} = 12 and 14 GHz, P_{LO} = 0 dBm			12		dB
Input 1dB compression point[(2)]	f_{RF} = 14 GHz, f_{IF} = 1 GHz, P_{LO} = +17 dBm, USB and LSB			10		dBm
Input IP2	f_{RF} = 14 GHz, f_{IF1} = 1 GHz, f_{IF2} = 1.01 GHz, P_{LO} = +17 dBm, P_{IF} = –5 dBm, USB and LSB			45		dBm
Input IP3	f_{RF} = 14 GHz, f_{IF1} = 1 GHz, f_{IF2} = 1.01 GHz, P_{LO} = +17 dBm, P_{IF} = –5 dBm, USB and LSB		18	21		dBm

Notes:
1) Image rejection is measured in upconversion mode. IF1 and IF2 quadrature input signals are generated using a pair of phase locked signal generators. Employed method eliminates errors associated with traditional 90° hybrid.
2) The input P1dB compression point is a linearity figure of merit. Refer to **Table 2** for the operating input power (50Ω).

Thermal Data

Psi-JT (Ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$\Psi_{JT} = (T_J - T_T)/P$

where

Ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

Table 4 • *Thermal Data for PE41901*

Parameter	Typ	Unit
Ψ_{JT}	28	°C/W
Θ_{JA}, junction-to-ambient thermal resistance	75	°C/W

MxN Spurious Outputs

Table 5 and Table 6 show the spurious outputs and LO spurious harmonics of the PE41901.

Table 5 • *Spurious Outputs*(*)

	nLO				
mIF	0	1	2	3	4
0	X	6	21	20	16
1	23	X	36	49	X
2	58	69	52	62	X
3	47	60	59	X	X
4	28	17	38	X	X

Note: * Measured in upconversion mode: P_{RF} = –23 dBm @ 14 GHz; P_{IF} = –10 dBm @ 4 GHz; P_{LO} = +20 dBm @ 10 GHz,. All values in dBc below RF level, measured at RF port.

Table 6 • *LO Spurious Harmonics*(*)

	nLO Spur at RF Port			
LO Freq (GHz)	1	2	3	4
10 (P_{RF} = –32 dBm)	X	4	14	10
12 (P_{RF} = –25 dBm)	X	2	24	X
14 (P_{RF} = –25 dBm)	X	10	X	X
16 (P_{RF} = –16 dBm)	X	16	X	X
18 (P_{RF} = –17 dBm)	X	13	X	X

Note: * Measured in upconversion mode: P_{LO} = +17 dBm. Values in dBc below LO level, measured at RF port.

Typical Performance Data

Figure 2–Figure 23 show the typical performance data at +25 °C, P_{LO} = +17 dBm, P_{IF} = –5 dBm (Z = 50Ω), unless otherwise specified.

Figure 2 • ***Conversion Loss vs USB/LSB, f_{IF} = 1 GHz***

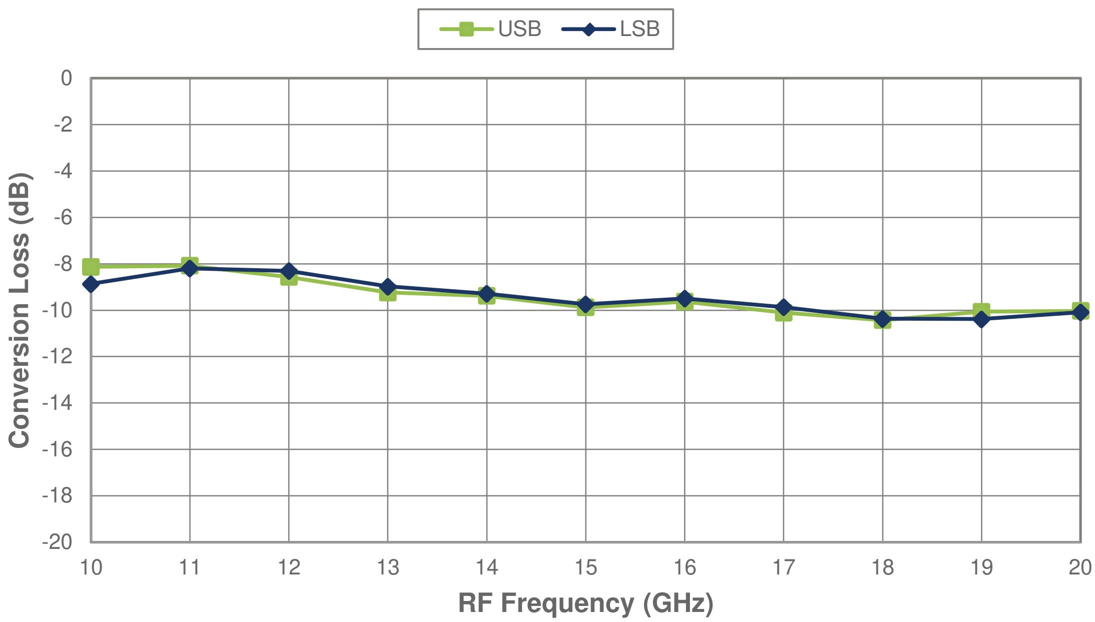


Figure 3 • ***Conversion Loss vs USB/LSB, f_{IF} = 4 GHz***

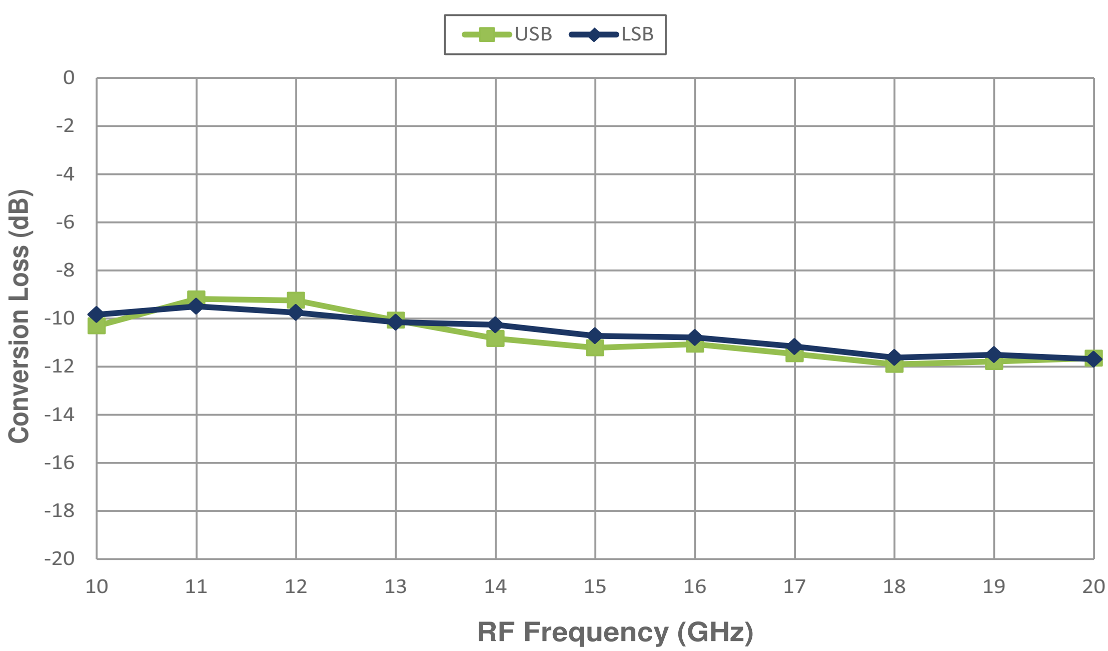


Figure 4 • *USB Conversion Loss vs Temperature, f_{IF} = 1 GHz*

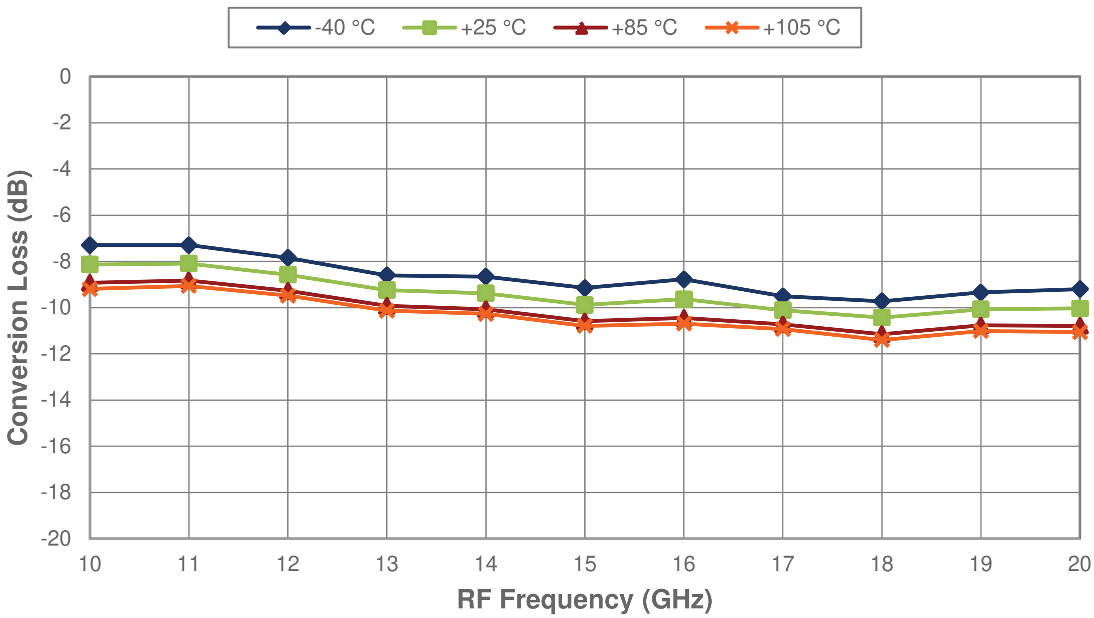


Figure 5 • *LSB Conversion Loss vs Temperature, f_{IF} = 1 GHz*

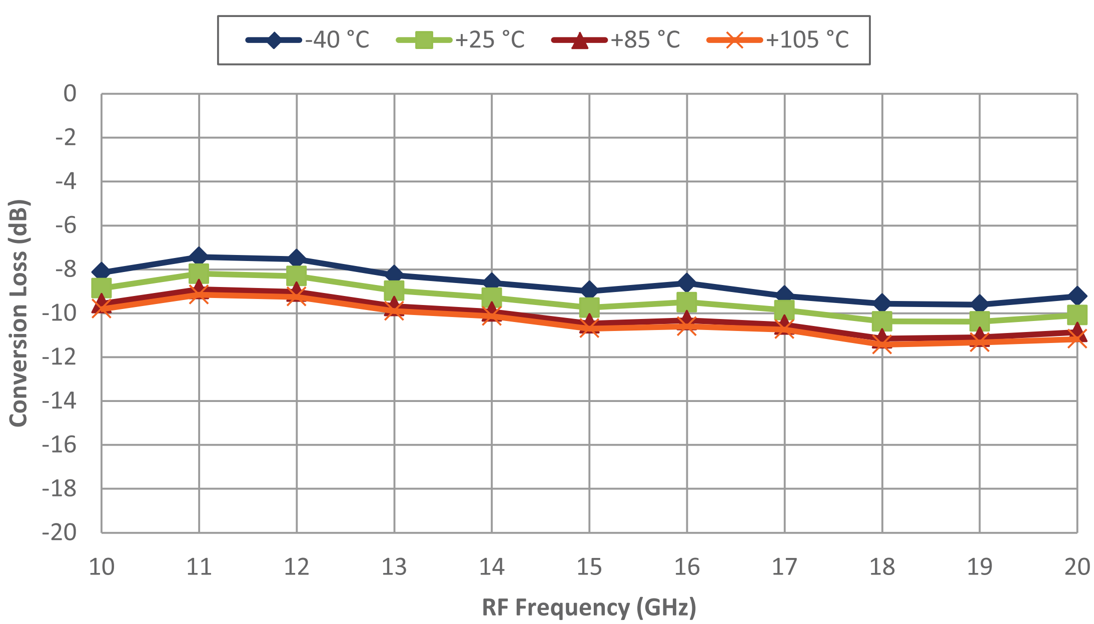


Figure 6 • *Image Rejection vs USB/LSB, f_{IF} = 1 GHz*

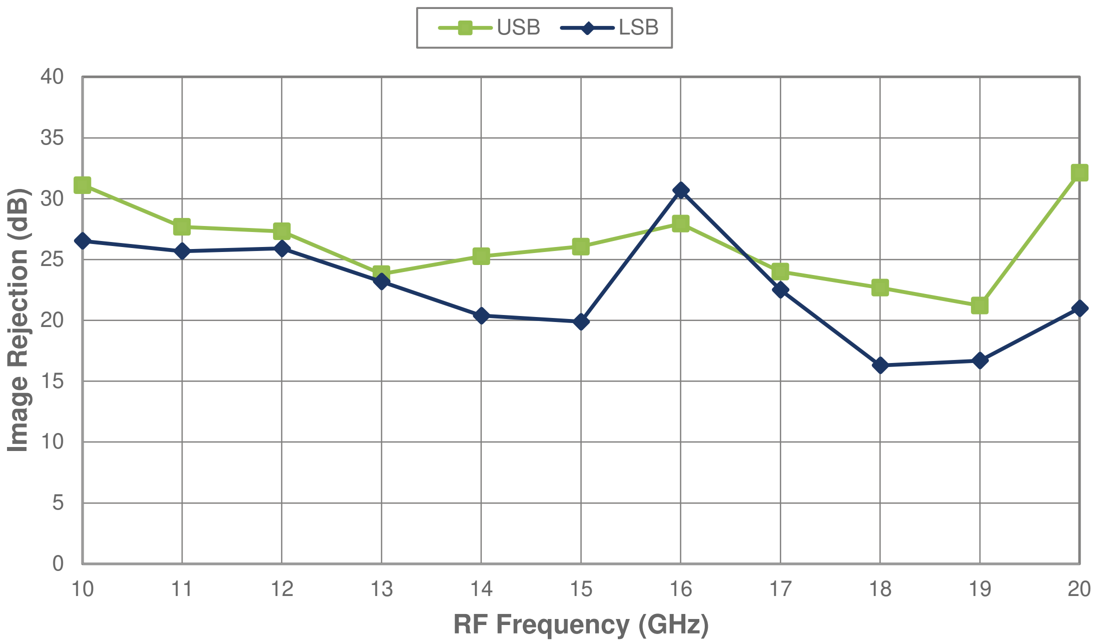


Figure 7 • *Image Rejection vs USB/LSB, f_{IF} = 4 GHz*

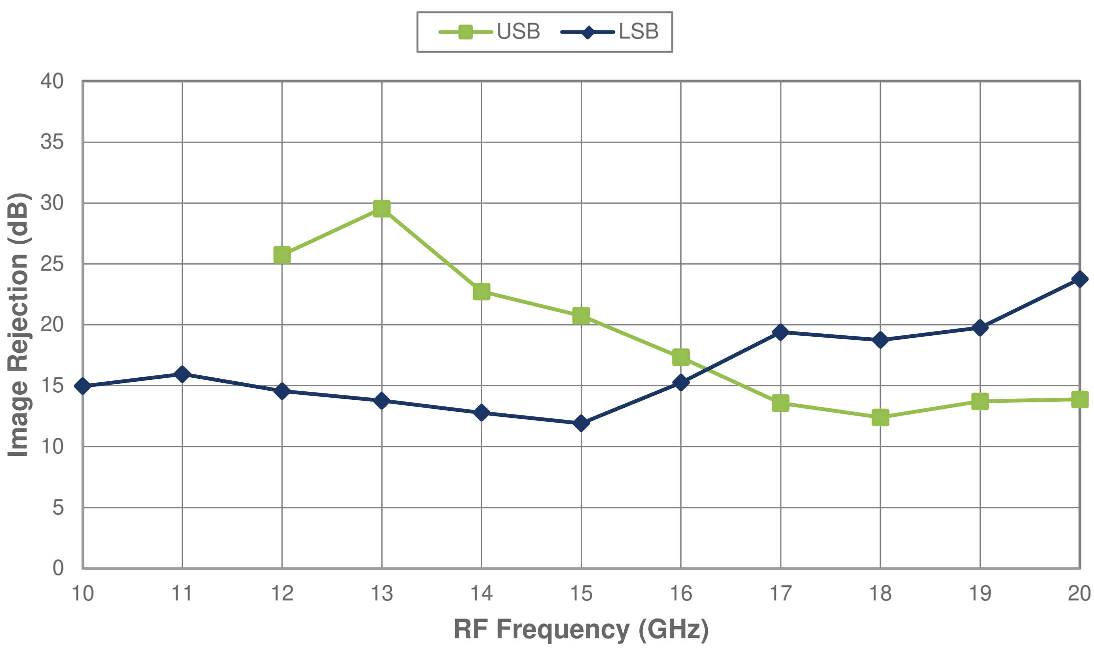


Figure 8 • *USB Image Rejection vs Temperature, f_{IF} = 1 GHz*

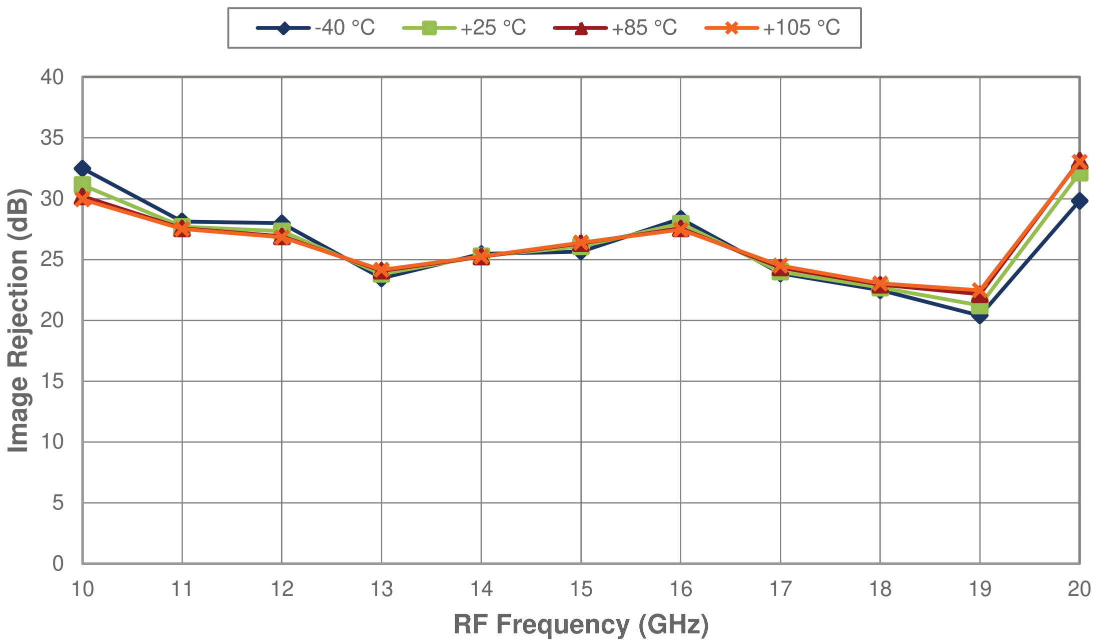


Figure 9 • *LSB Image Rejection vs Temperature, f_{IF} = 1 GHz*

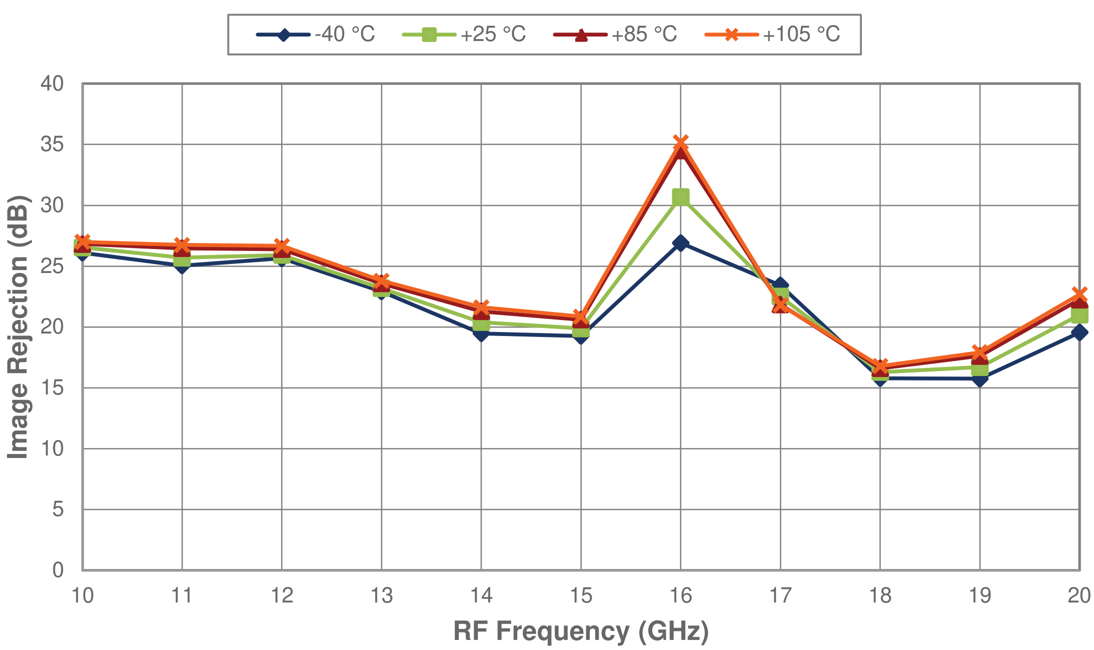


Figure 10 • *Input 1dB Compression Point (P1dB) vs USB/LSB, f_{IF} = 1 GHz*

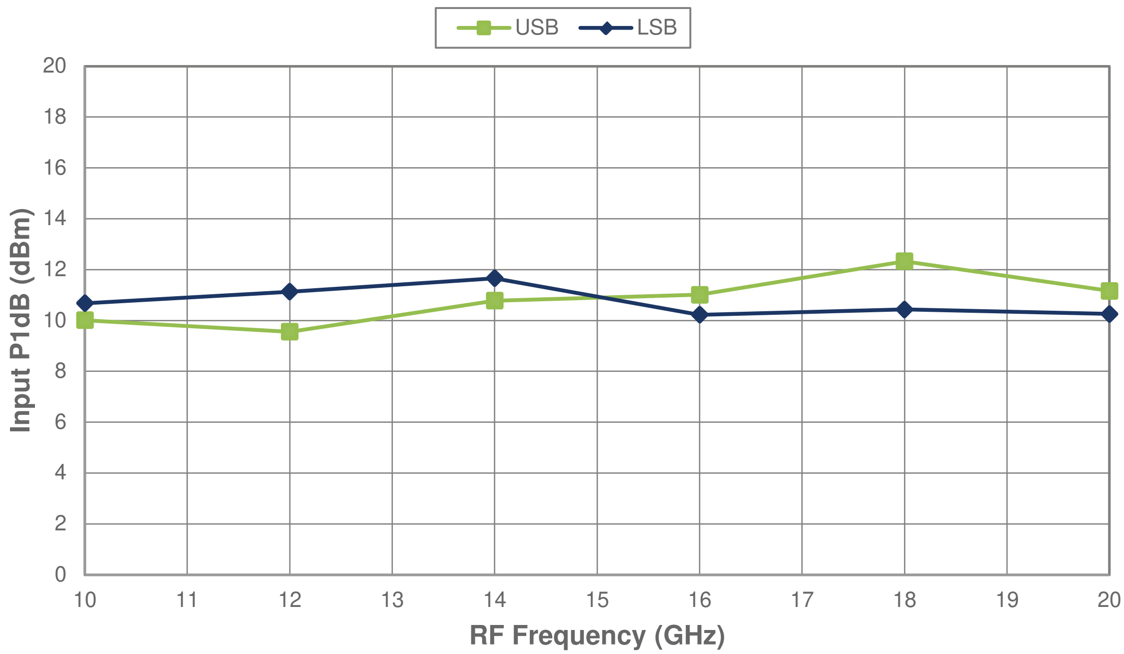


Figure 11 • *Input 1dB Compression Point (P1dB) vs USB/LSB, f_{IF} = 4 GHz*

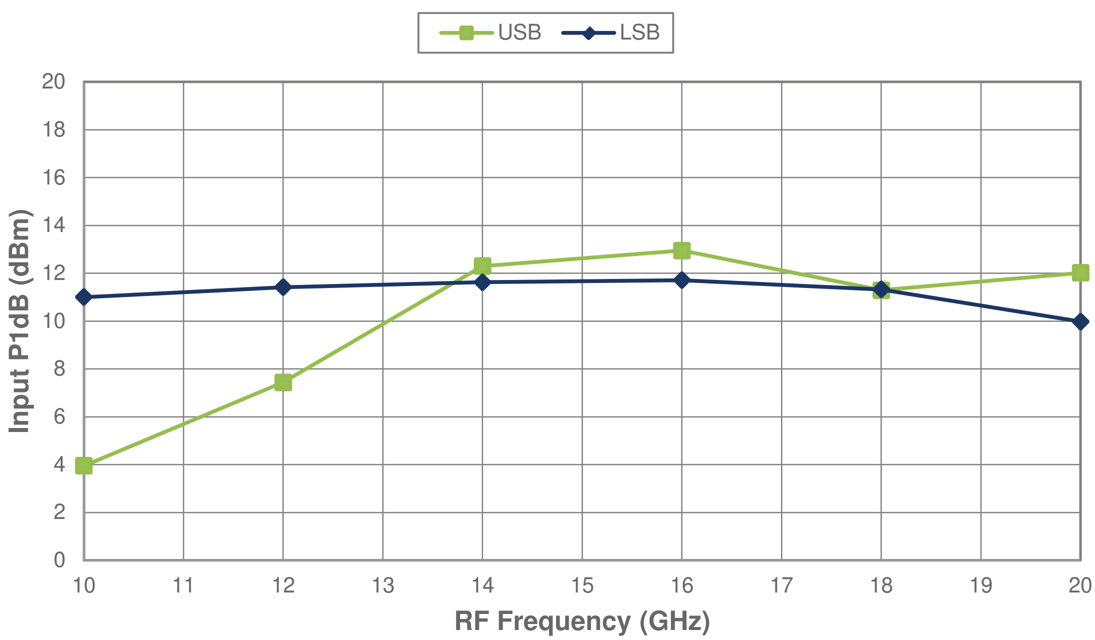


Figure 12 • *Input IP3 vs USB/LSB, f_{IF} = 1 GHz*

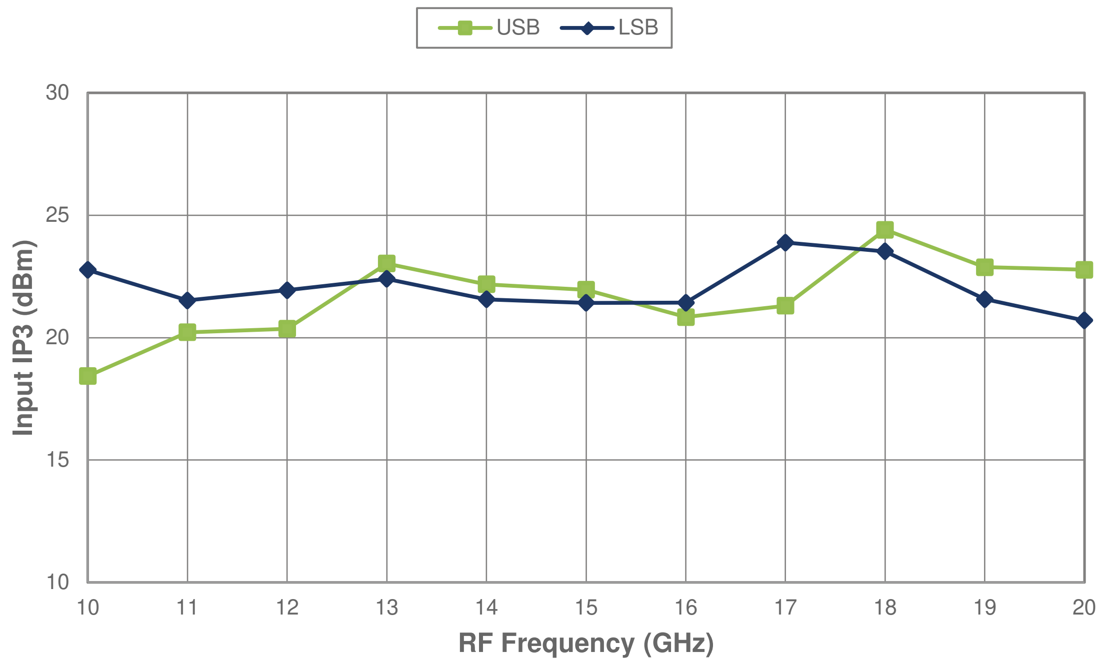


Figure 13 • *Input IP3 vs USB/LSB, f_{IF} = 4 GHz*

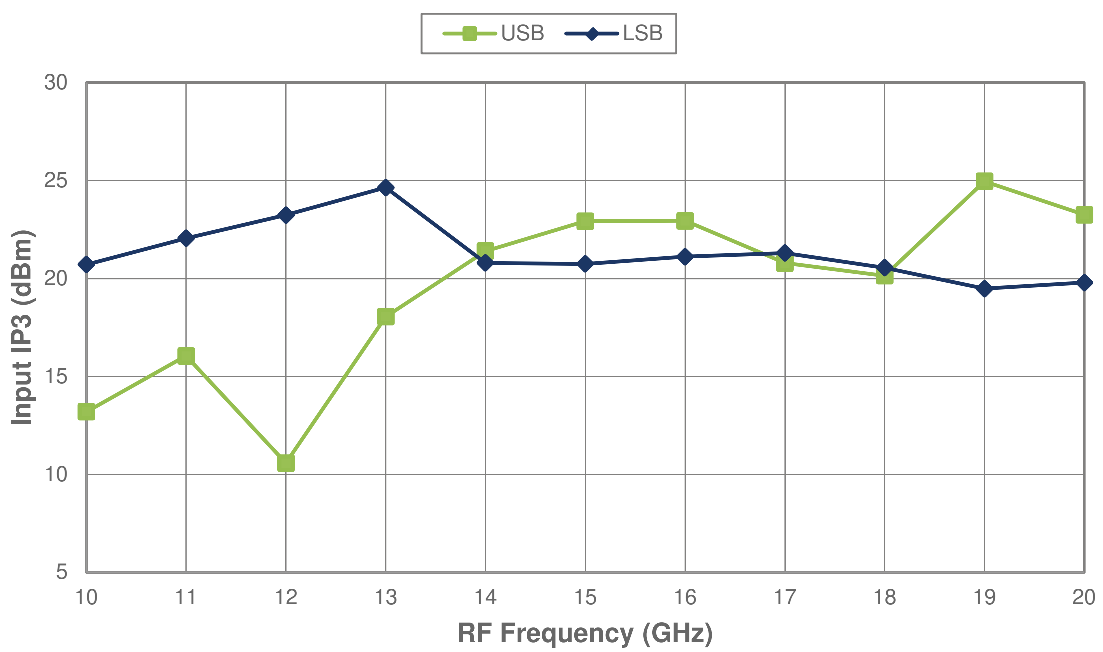


Figure 14 • *USB Input IP3 vs Temperature, f_{IF} = 1 GHz*

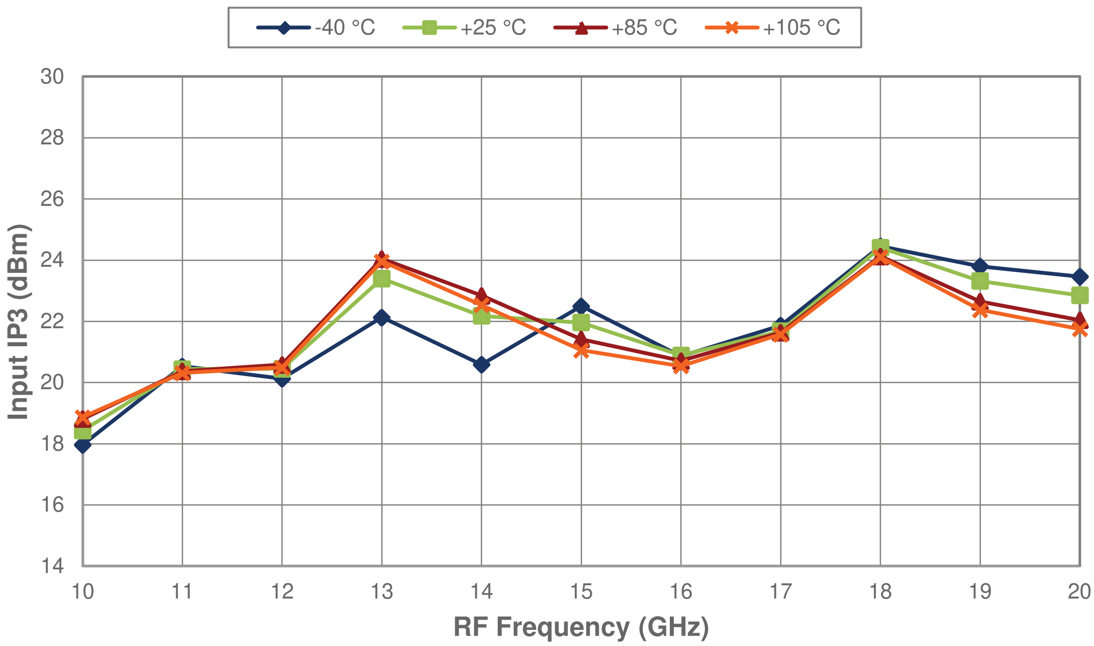


Figure 15 • *LSB Input IP3 vs Temperature, f_{IF} = 1 GHz*

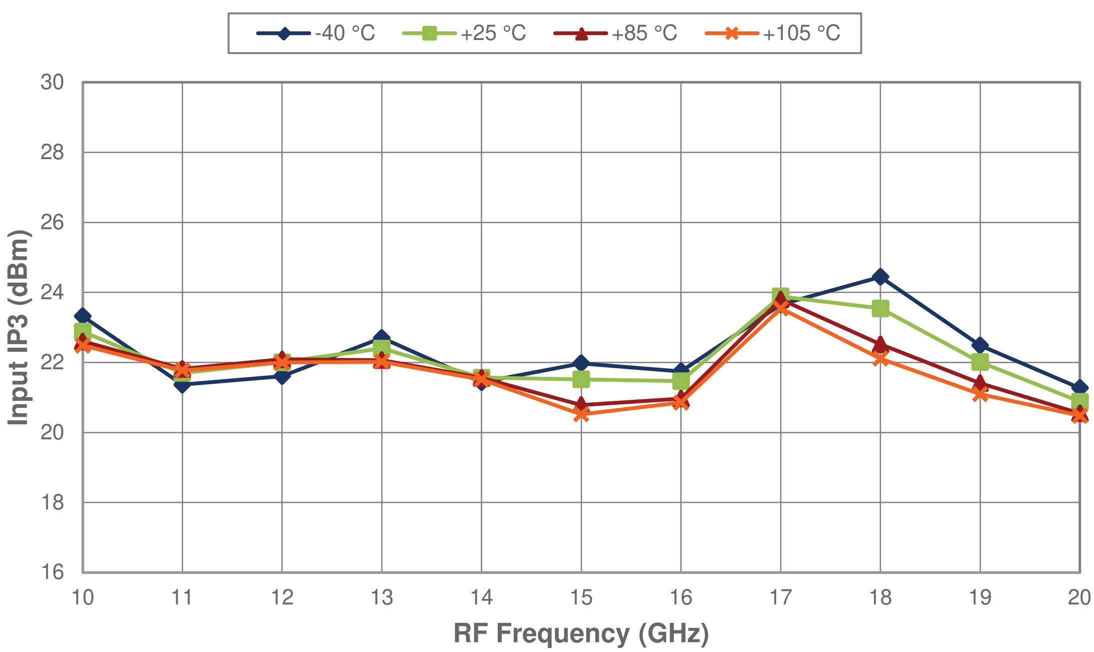


Figure 16 • *USB Input IP3 vs Temperature, f_{RF} = 14 GHz and f_{IF} = 1 GHz*

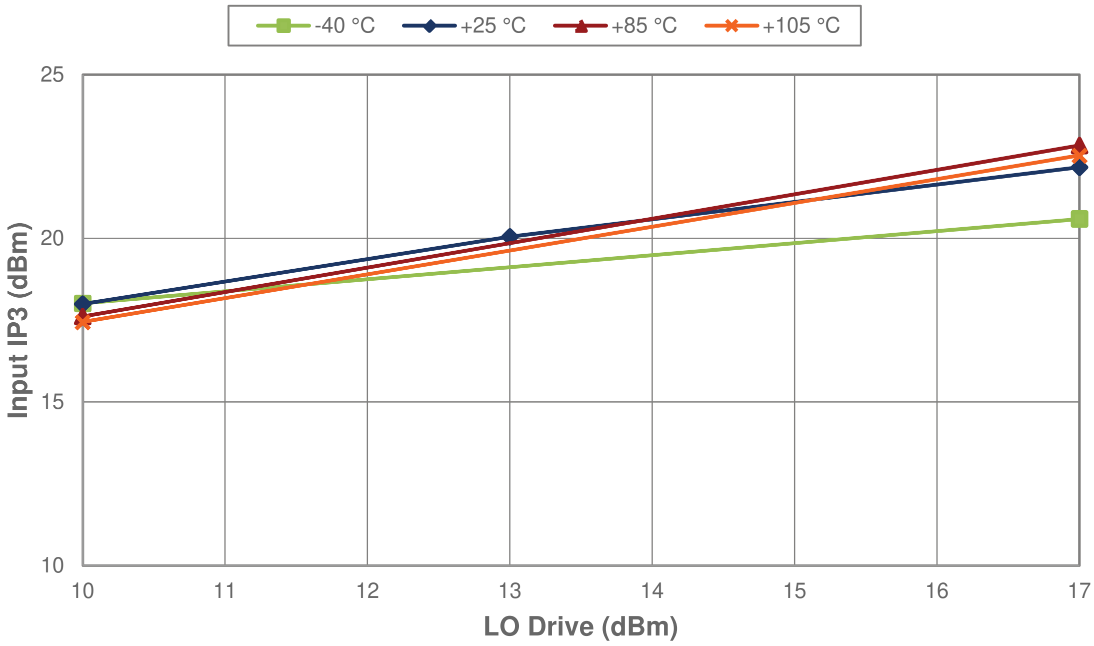


Figure 17 • *LSB Input IP3 vs Temperature, f_{RF} = 14 GHz and f_{IF} = 1 GHz*

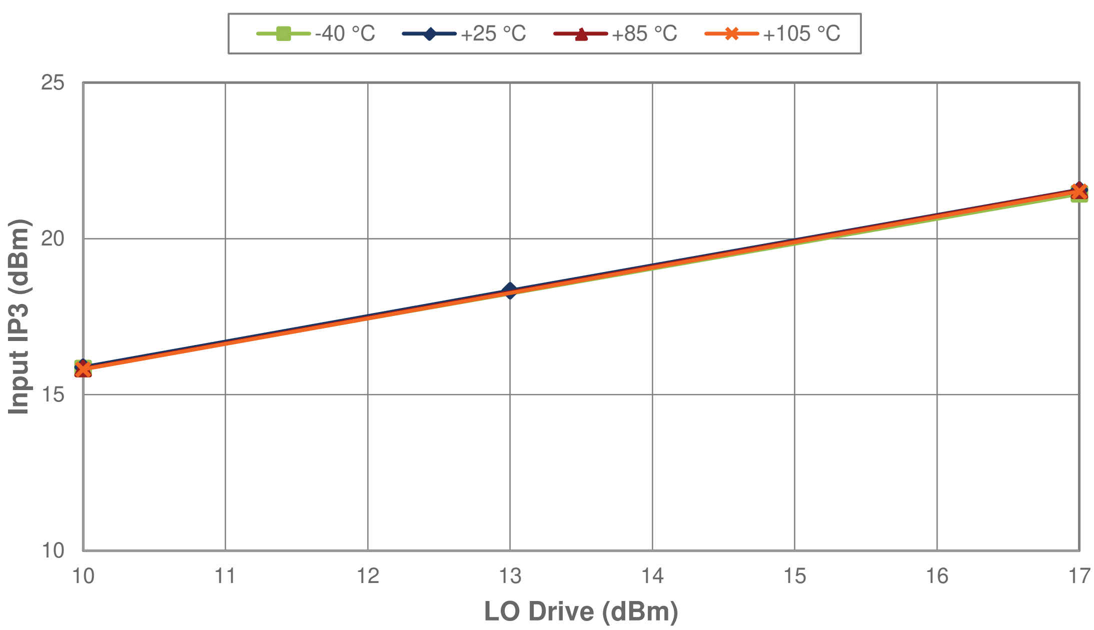


Figure 18 • *RF Return Loss vs Temperature, P_{LO} = +15 dBm, $P_{IF/RF}$ = 0 dBm*

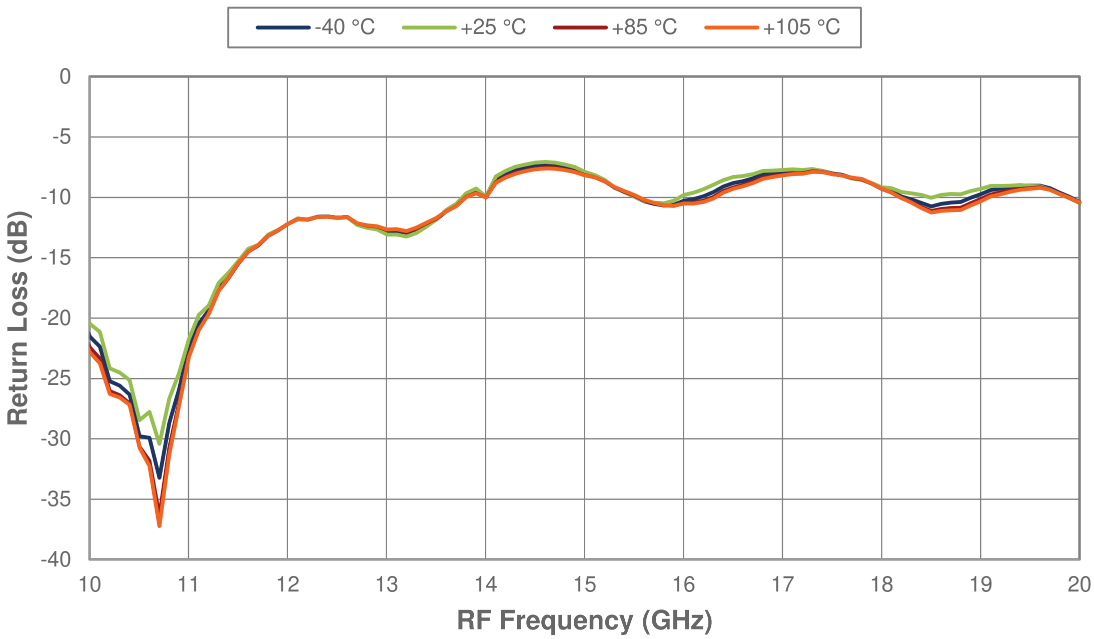


Figure 19 • *IF Return Loss vs Temperature, P_{LO} = +15 dBm, $P_{IF/RF}$ = 0 dBm*

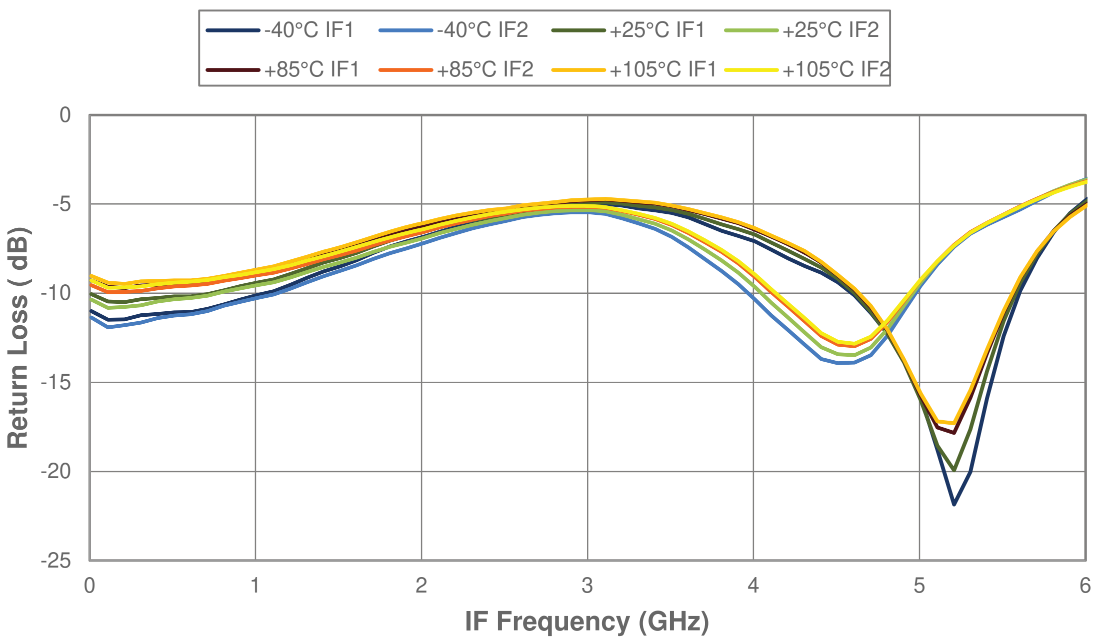


Figure 20 • *LO Return Loss vs Temperature, P_{LO} = 0 dBm*

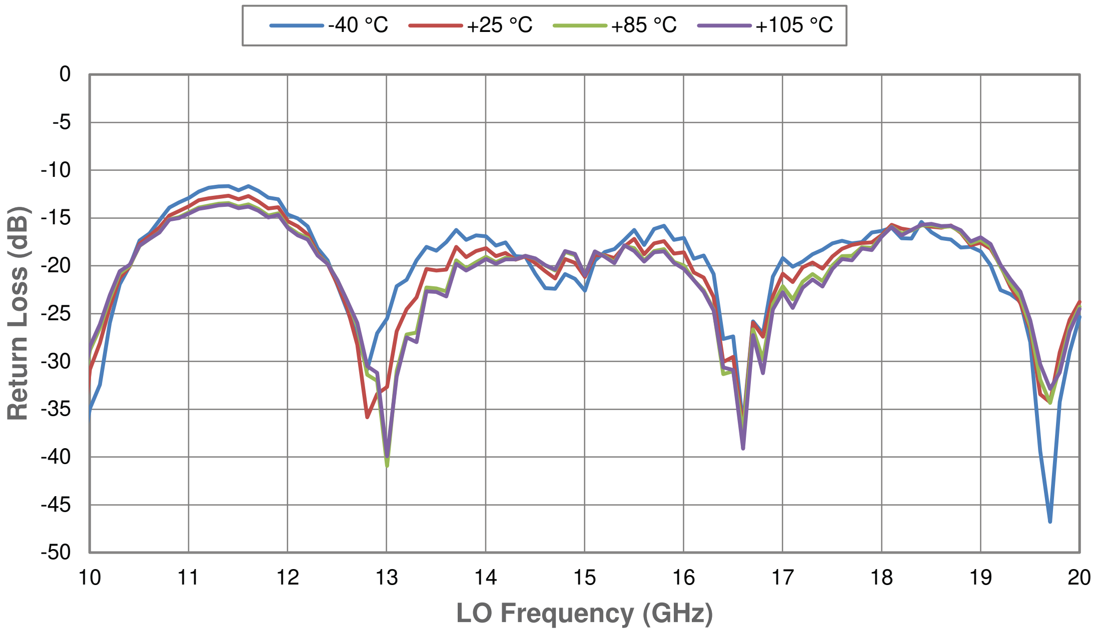


Figure 21 • *LO–IF Isolation vs IF Path*

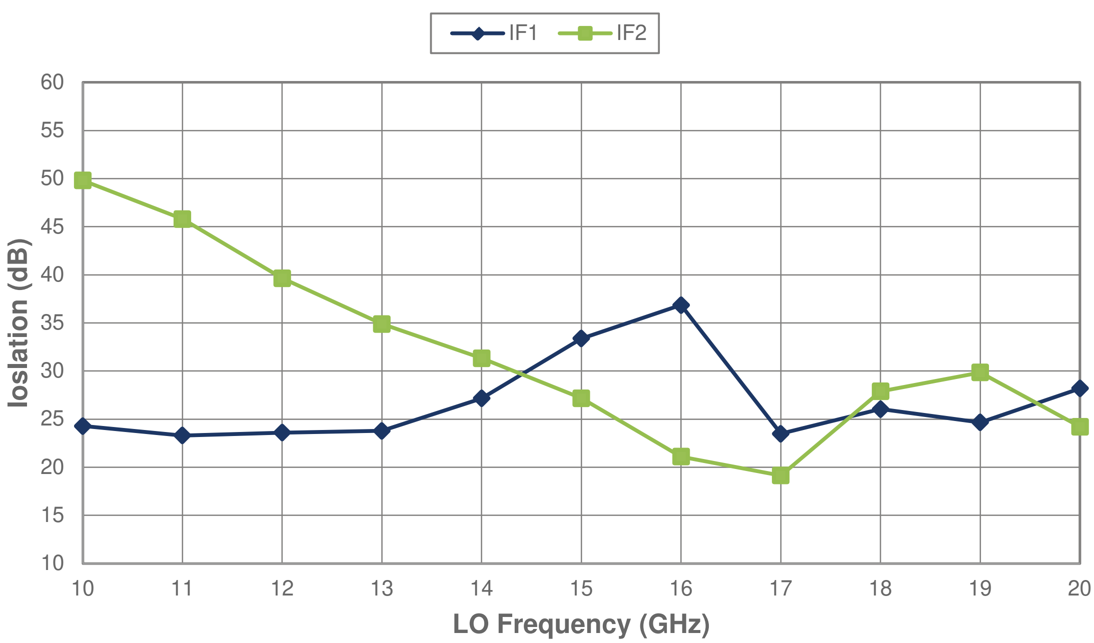


Figure 22 • *LO–IF Isolation vs Temperature/IF Path*

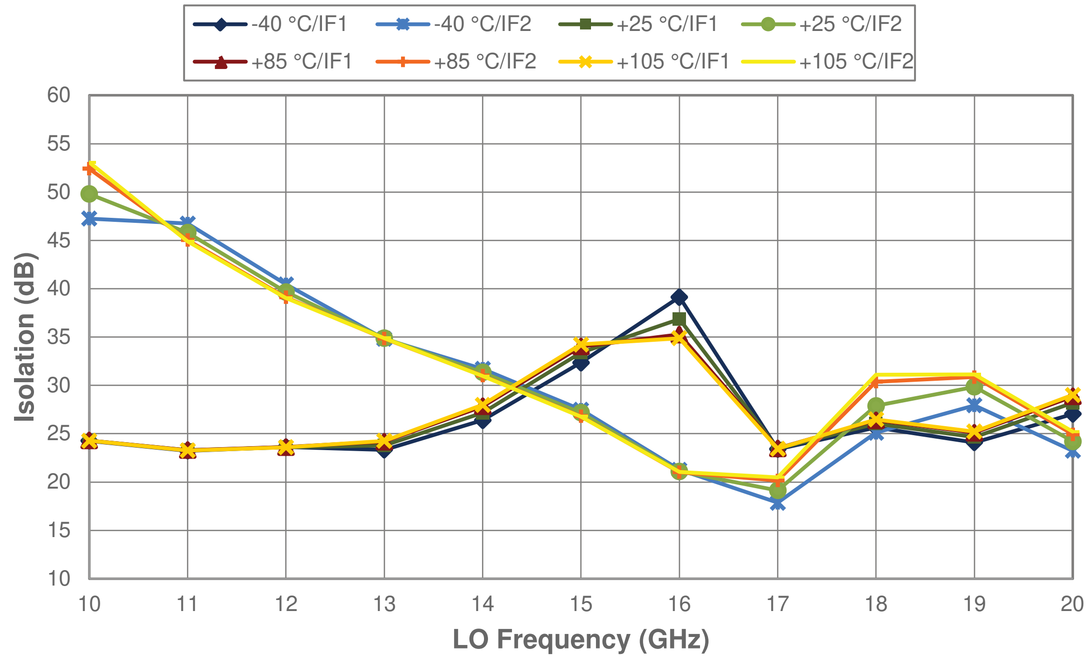
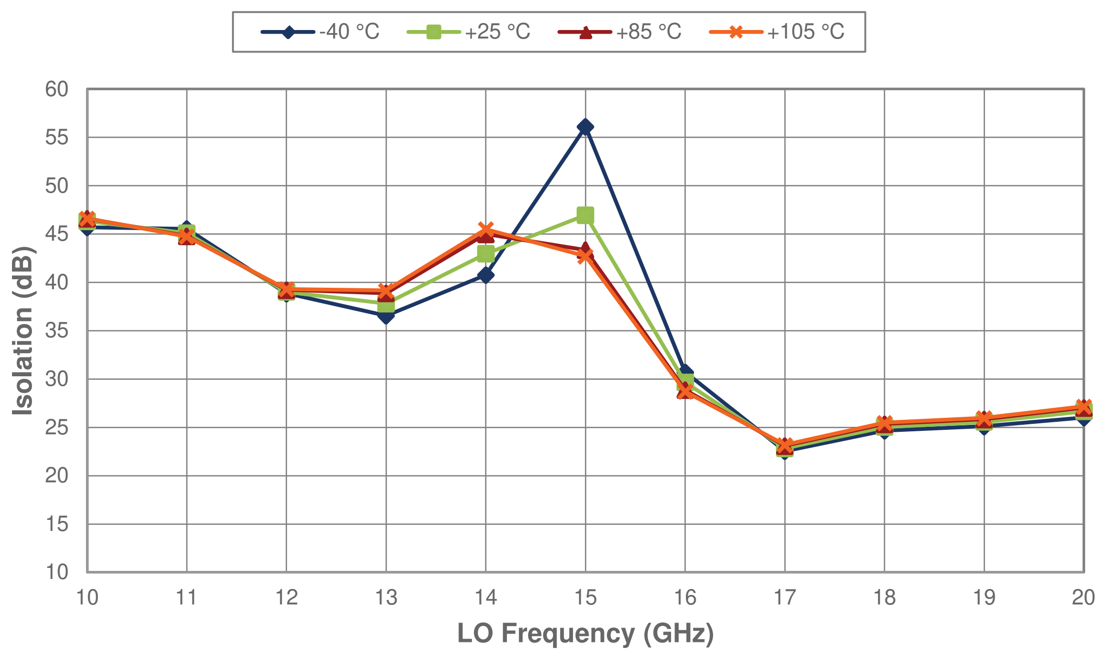


Figure 23 • *LO–RF Isolation vs Temperature*

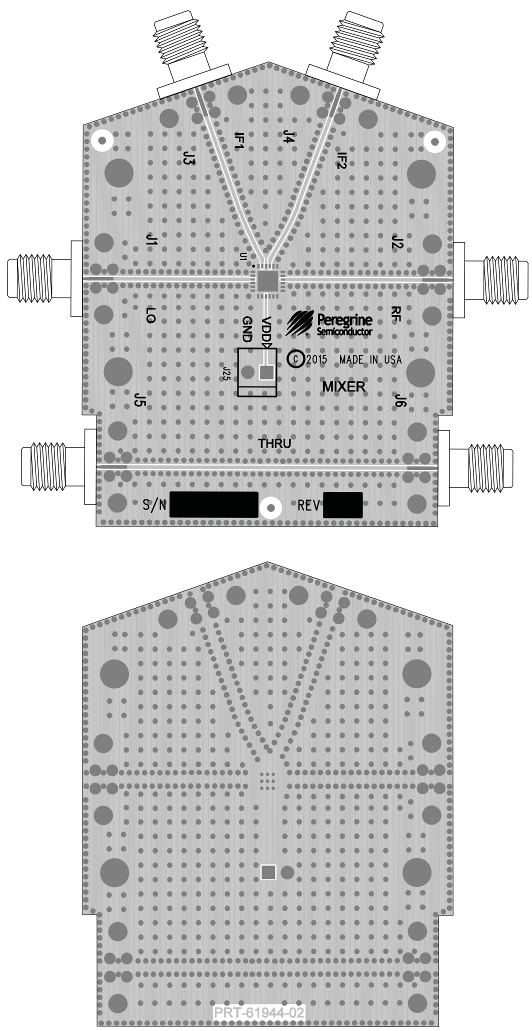


Evaluation Kit

The PE41901 evaluation board (EVB) was designed to ease customer evaluation of the PE41901 mixer. The RF, IF and LO ports are connected through 50Ω transmission lines via SMA connectors J2, J3, J4 and J1, respectively. A 50Ω through transmission line is available via SMA connectors J5 and J6, which can be used to de-embed the loss of the PCB.

Please note that this is a generic PCB and is being used for multiple parts. Pin labeled V_{DD} is GND. J25 is not being used for the PE41901.

Figure 24 • *Evaluation Kit Layout for PE41901*

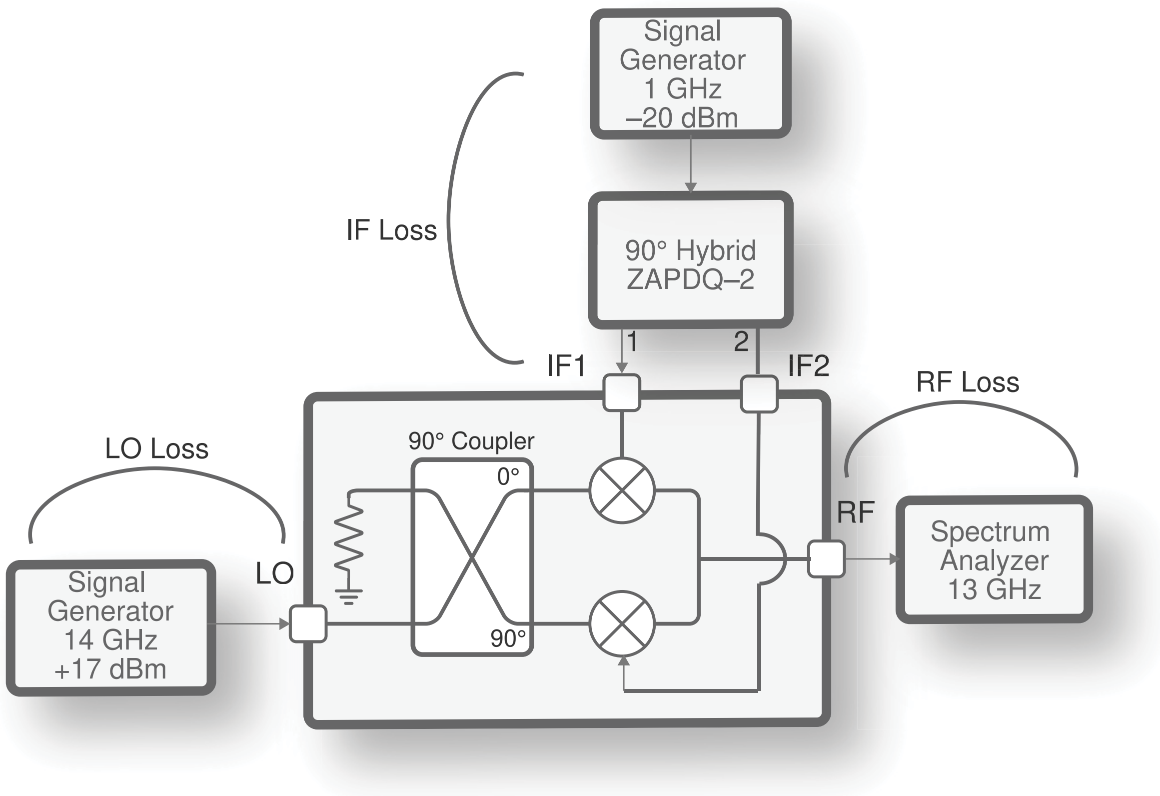


Typical Test Set Up

Figure 25 shows the simplified test circuit of the PE41901. The two IF inputs require a quadrature signal to be applied. The figure shows a method of creating this signal using a 90° hybrid. When measuring the mixer, all cable, connector and board losses must be calibrated and compensated for. The EVK includes a through trace that can be used to calibrate out the board loss. The trace length is equivalent to two times the input or output trace lengths.

Please note that 90° hybrids have limited bandwidth, so an appropriate hybrid must be selected for the IF range being tested.

Figure 25 • ***Typical Test Set Up for PE41901***



Pin Information

This section provides pinout information for the PE41901. **Figure 26** shows the pin map of this device for the available package. **Table 7** provides a description for each pin.

Figure 26 • *Pin Configuration (Top View)*

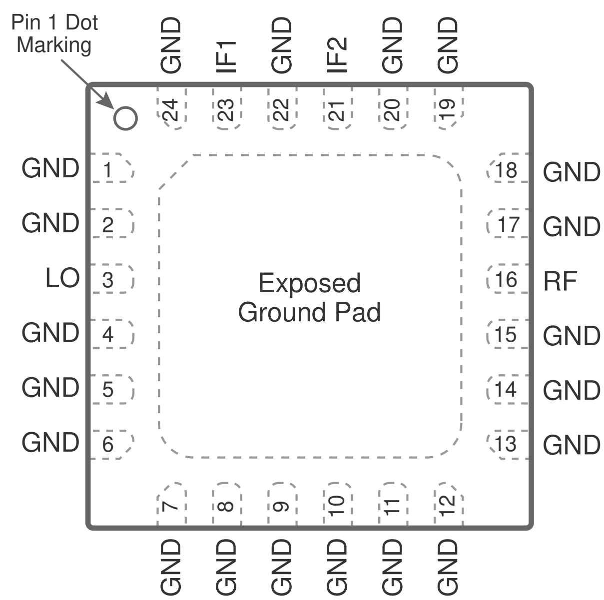


Table 7 • *Pin Descriptions for PE41901*

Pin No.	Pin Name	Description
1, 2, 4–15, 17–20, 22, 24	GND	Ground
3	LO(1)	LO port
16	RF(1)	RF port
21	IF2(2)	IF2 port
23	IF1(2)	IF1 port
Pad	GND	Exposed pad. Ground for proper operation

Notes:

1) The PE41901 does not generate a DC voltage on the LO or RF pins. Consequently, DC blocking capacitors are not required on these pins. If a DC voltage exists on the LO or RF pins due to neighboring components in the application circuit, DC blocking capacitors should be used to protect the PE41901.
2) IF1 and IF2 are 90° out of phase.

Packaging Information

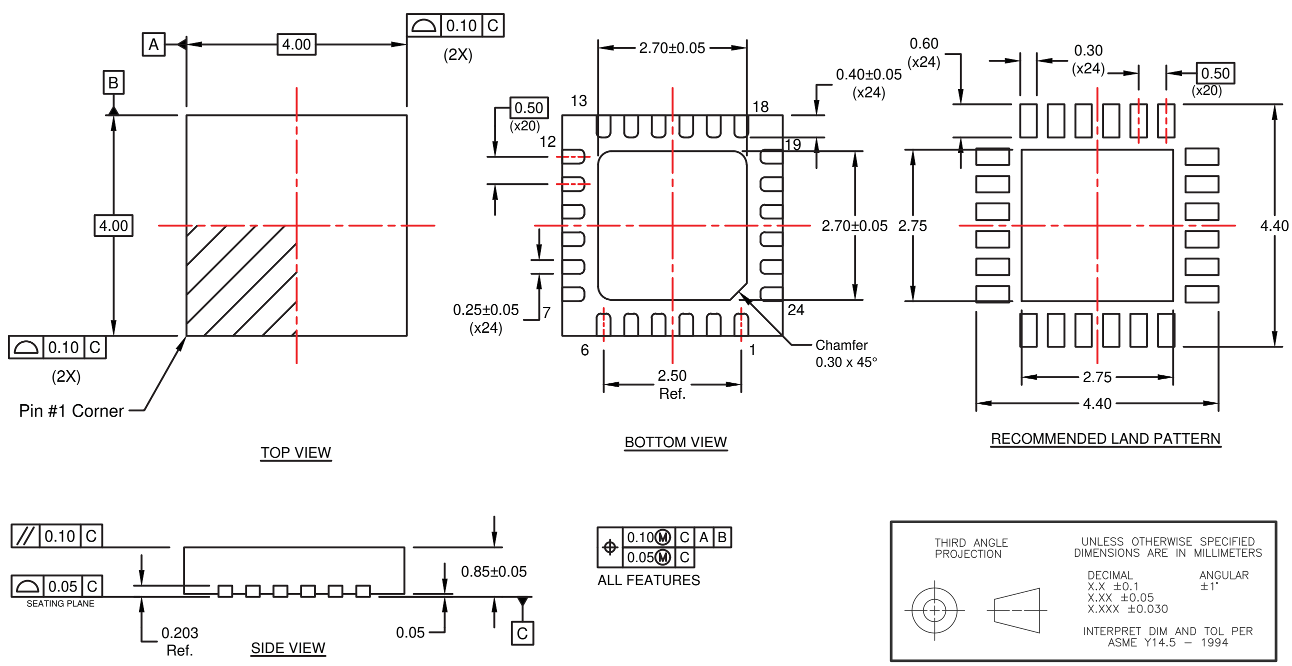
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE41901 in the 24-lead 4 × 4 × 0.85 mm QFN package is MSL1.

Package Drawing

Figure 27 • ***Package Mechanical Drawing for 24-lead 4 × 4 × 0.85 mm QFN***



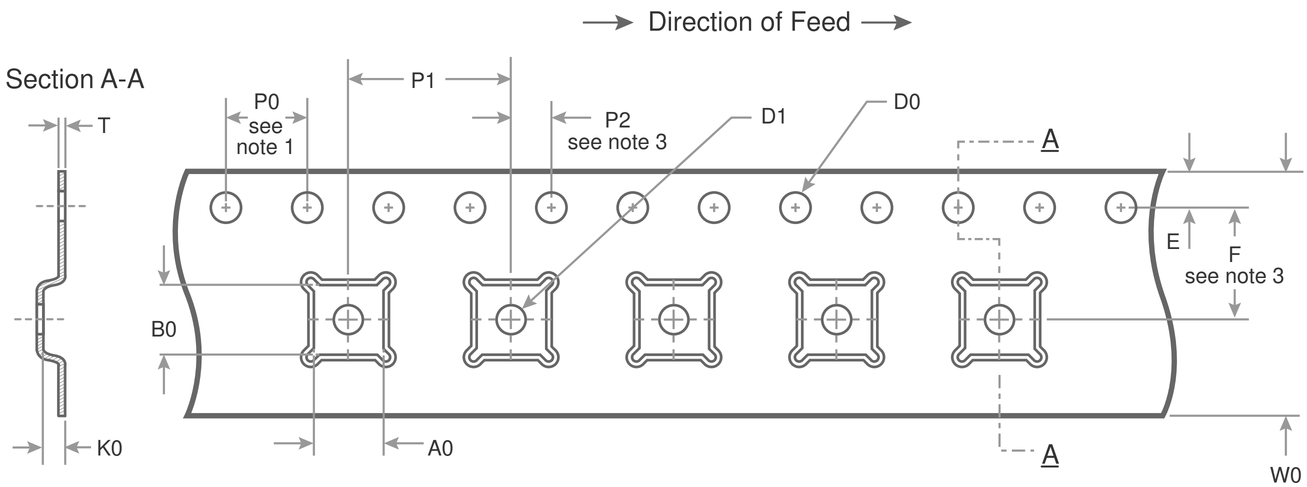
Top-Marking Specification

Figure 28 • ***Package Marking Specifications for PE41901***

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (maximum six characters)

Tape and Reel Specification

Figure 29 • *Tape and Reel Specifications for 24-lead 4 × 4 × 0.85 mm QFN*

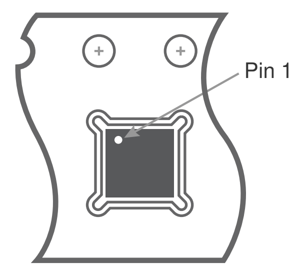


A0	4.35
B0	4.35
K0	1.10
D0	1.50 + 0.10/ -0.00
D1	1.50 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions are in millimeters unless otherwise specified



Device Orientation in Tape

Ordering Information

Table 8 lists the available ordering codes for the PE41901 as well as available shipping methods.

Table 8 • *Order Codes for PE41901*

Order Codes	Description	Packaging	Shipping Method
PE41901A-X	PE41901 image reject mixer	Green 24-lead 4 × 4 mm QFN	500 units/T&R
EK41901-01	Evaluation kit	Evaluation kit	1/box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Not Recommended for New Designs (NRND)

This product is in production but is not recommended for new designs.

End of Life (EOL)

This product is currently going through the EOL process. It has a specific last-time buy date.

Obsolete

This product is discontinued. Orders are no longer accepted for this product.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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