# mail

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# For full datasheet, please visit dtc.psemi.com.

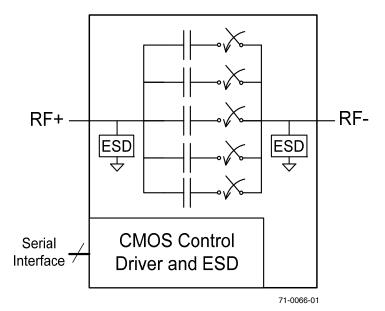
# **Product Description**

The PE64101 is a DuNE<sup>™</sup>-enhanced Digitally Tunable Capacitor (DTC) based on Peregrine's UltraCMOS<sup>®</sup> technology. DTC products provide a monolithically integrated impedance tuning solution for demanding RF applications. They also offer a cost-effective tunable capacitor with excellent linearity and ESD performance.

This highly versatile product can be mounted in series or shunt configuration and is controlled by a 3-wire (SPI compatible) serial interface. High ESD rating of 2 kV HBM on all ports making this the ultimate in integration and ruggedness. The DTC is offered in a standard 12lead 2.0 x 2.0 x 0.55 mm QFN package.

Peregrine's DuNE<sup>™</sup> technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS<sup>®</sup> process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

# Figure 1. Functional Block Diagram



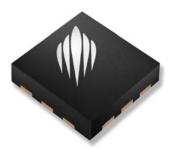
UltraCMOS<sup>®</sup> Digitally Tunable Capacitor (DTC) 100 - 3000 MHz

#### Features

- 3-wire (SPI compatible) 8-bit serial interface with built-in bias voltage generation and stand-by mode for reduced power consumption
- DuNE<sup>™</sup>-enhanced UltraCMOS<sup>®</sup> device
- 5-bit 32-state Digitally Tunable Capacitor
- C = 1.38 5.90 pF (4.3:1 tuning ratio) in discrete 146 fF steps
- RF power handling (up to 26 dBm, 6  $V_{\text{PK}}\,\text{RF})$  and high linearity
- High quality factor
- Wide power supply range (2.3 to 3.6V) and low current consumption (typ. I<sub>DD</sub> = 30 μA @ 2.8V)
- Optimized for shunt configuration, but can also be used in series configuration
- Excellent 2 kV HBM ESD tolerance on all pins
- Applications include:
  - Antenna tuning
  - Tunable filters
  - Phase shifters
  - Impedance matching

# Figure 2. Package Type

12-lead 2 x 2 x 0.55 mm QFN





#### Table 1. Electrical Specifications @ 25°C, V<sub>DD</sub> = 2.8V

Parameter	Configuration	Condition		Тур	Max	Units
Operating Frequency Range 7	Both		100		3000	MHz
Minimum Capacitance	Shunt <sup>6</sup>	State = 00000, 100 MHz (RF+ to Grounded RF-) -1		1.38	+10%	pF
Maximum Capacitance	Shunt 6	State = 11111, 100 MHz (RF+ to Grounded RF-)		5.90	+10%	pF
Tuning Ratio	Shunt 6	C <sub>max</sub> /C <sub>min</sub> , 100 MHz		4.3:1		
Step Size	Shunt 6	5 bits (32 states), constant step size (100 MHz)		0.146		pF
Quality Factor (C <sub>min</sub> ) <sup>1</sup>	Shunt <sup>6</sup>	70 - 582 MHz with $L_s$ removed 98 - 960 MHz, with $L_s$ removed 710 - 2170 MHz, with $L_s$ removed		50 50 30		
Quality Factor (C <sub>max</sub> ) <sup>1</sup>	Shunt <sup>6</sup>	470 - 582 MHz with $L_s$ removed 698 - 960 MHz, with $L_s$ removed 1710 - 2170 MHz, with $L_s$ removed		50 25 10		
Self Resonant Frequency	Shunt 7	Shunt <sup>7</sup> State 00000 State 11111		5.5 2.5		GHz
	Shunt <sup>6</sup>	470 to 582 MHz, Pin +26 dBm, 50Ω 698 to 915 MHz, Pin +26 dBm, 50Ω 1710 to 1910 MHz, Pin +26 dBm, 50Ω			-36 -36 -36	dBm dBm dBm
Harmonics ( $2_{fo}$ and $3_{fo}$ ) $^4$	Series <sup>5</sup>	470 to 582 MHz, Pin +20 dBm, 50Ω 698 to 915 MHz, Pin +20 dBm, 50Ω 1710 to 1910 MHz, Pin +20 dBm, 50Ω			-36 -36 -36	dBm dBm dBm
3rd Order Intercept Point	Intercept PointIIP3 = (Pblocker + 2*Ptx - [IMD3]) / 2, where IMD3 = -95 dBm, Ptx = +20 dBm and Pblocker = -15 dBm		60		dBm	
Switching Time <sup>2, 3</sup>	Shunt <sup>6</sup>	State change to 10/90% delta capacitance between any two states		2	10	μs
Start-up Time <sup>2</sup>	Shunt <sup>6</sup>	Time from $V_{DD}$ within specification to all performances within specification		5	20	μs
Wake-up Time <sup>2, 3</sup>	Shunt <sup>6</sup>	State change from standby mode to RF state to all performances within specification		5	20	μs

Note: 1. Q for a Shunt DTC based on a Series RLC equivalent circuit
 Q = X<sub>C</sub> / R = (X-X<sub>L</sub>)/R, where X = X<sub>L</sub> + X<sub>C</sub>, X<sub>L</sub> = 2<sup>\*</sup>pi\*f\*L, X<sub>C</sub> = -1 / (2\*pi\*f\*C), which is equal to removing the effect of parasitic inductance L<sub>S</sub>
 2. DC path to ground at RF+ and RF- must be provided to achieve specified performance
 3. State change activated on falling edge of SEN following data word
 4. Between 50Ω ports in series or shunt configuration using a pulsed RF input with 4620 vs period, 50% duty cycle, measured per 3GPPTS45.005
 5. Ju perior configuration the ground are the pulse a character BE were reprint to RE.

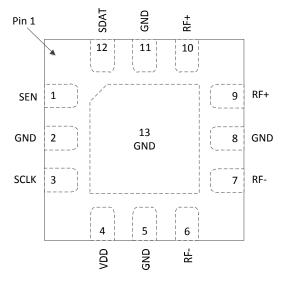
5. In series configuration the greater RF power or higher RF voltage should be applied to RF+

6. RF- should be connected to ground

7. DTC operation above SRF is possible



#### Figure 3. Pin Configuration (Top View)



#### **Table 2. Pin Descriptions**

Pin #	Pin Name	Description	
1	SEN	Serial Enable	
2	GND	Digital and RF Ground	
3	SCLK	Serial Interface Clock Input	
4	VDD	Power Voltage	
5	GND	Digital and RF Ground	
6	RF-	Negative RF Port <sup>1</sup>	
7	RF-	Negative RF Port <sup>1</sup>	
8	GND	Digital and RF Ground <sup>3</sup>	
9	RF+	Positive RF Port <sup>2</sup>	
10	RF+	Positive RF Port <sup>2</sup>	
11	GND	Digital and RF Ground	
12	SDAT	Serial Interface Data Input	
13	GND	Digital and RF Ground <sup>3</sup>	

Notes: 1. Pins 6 and 7 must be tied together on PCB board to reduce inductance

2. Pins 9 and 10 must be tied together on PCB board to reduce inductance

3. Pin 2, 5, 8, 11 and 13 must be connected together on PCB

#### **Moisture Sensitivity Level**

The Moisture Sensitivity Level rating for the PE64101 in the 12-lead 2 x 2 QFN package is MSL1.

#### Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS<sup>®</sup> devices are immune to latch-up.

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#### Table 3. Operating Ranges<sup>1</sup>

Parameter	Symbol	Min	Тур	Max	Units
V <sub>DD</sub> Supply Voltage	V <sub>DD</sub>	2.3	2.8	3.6	V
I <sub>DD</sub> Power Supply Current (Normal mode) <sup>6</sup>	I <sub>DD</sub>		30	75	μA
I <sub>DD</sub> Power Supply Current (Standby mode) <sup>6</sup>	I <sub>DD</sub>		20	45	μA
Control Voltage High	V <sub>IH</sub>	1.2		3.1	V
Control Voltage Low	VIL	0		0.2	V
Peak Operating RF Voltage $^5$ $$V_{\rm P}$ to $V_{\rm M}$$ $V_{\rm P}$ to $RFGND$$ $V_{\rm M}$ to $RFGND$$				6 6 6	V <sub>PK</sub> V <sub>PK</sub> V <sub>PK</sub>
RF Input Power (50Ω) <sup>3, 4, 5</sup> shunt series				+26 +20	dBm dBm
Input Control Current	I <sub>CTL</sub>		1	10	μA
Operating Temperature Range	T <sub>OP</sub>	-40		+85	°C
Storage Temperature Range	T <sub>ST</sub>	-65		+150	°C

Notes: 1. Operation should be restricted to the limits in the Operating Ranges table 2. The DTC is active when STBY is low (set to 0) and in low-current stand-by mode when high (set to 1)

3. Maximum CW power available from a 50 $\Omega$  source in shunt configuration 4. Maximum CW power available from a 50 $\Omega$  source in series configuration 5. RF+ to RF- and RF+ and/or RF- to ground. Cannot exceed 6 V<sub>PK</sub> or max RF input power (whichever occurs first)

 $I_{DD}$  (interest value is based on  $V_{DD}$  = 2.8V. Max  $I_{DD}$  is based on  $V_{DD}$  = 3.6V

#### **Table 4. Absolute Maximum Ratings**

Symbol	Parameter/Conditions	Min	Max	Units
$V_{\text{DD}}$	Power supply voltage	-0.3	4.0	V
VI	Voltage on any DC input	-0.3	4.0	v
$V_{\text{ESD}}$	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		2000	V
$V_{\text{ESD}}$	ESD Voltage (MM, JEDEC JESD22-A115-A)		100	v

Exceeding absolute maximum ratings may cause permanent damage. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

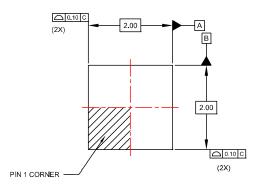
#### **Electrostatic Discharge (ESD) Precautions**

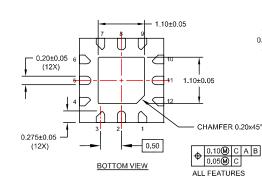
When handling this UltraCMOS<sup>®</sup> device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

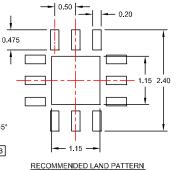


#### Figure 4. Package Drawing

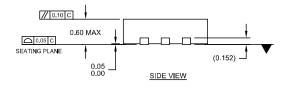
12-lead 2 x 2 x 0.55 mm QFN







TOP VIEW





#### Figure 5. Top Marking Specifications



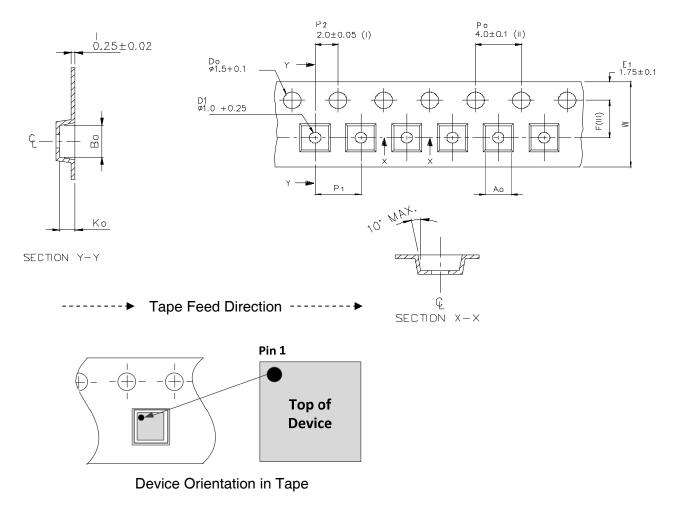
Marking Spec Symbol	Package Marking	Definition		
PP	CR Part number marking for PE64101			
ZZ	00-99	Last two digits of lot code		
		Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc)		
<b>WW</b> 01-53		Work week		

17-0112



#### Figure 6. Tape and Reel Specifications

12-lead 2 x 2 x 0.55 mm QFN



#### **Table 5. Ordering Information**

Order Code	Code Package Description		Shipping Method	
PE64101MLAA-Z	12-lead 2 x 2 x 0.55 mm QFN	Package Part in Tape and Reel	3000 units/T&R	
EK64101-11	Evaluation Kit	Evaluation Kit	1 Set/Box	

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