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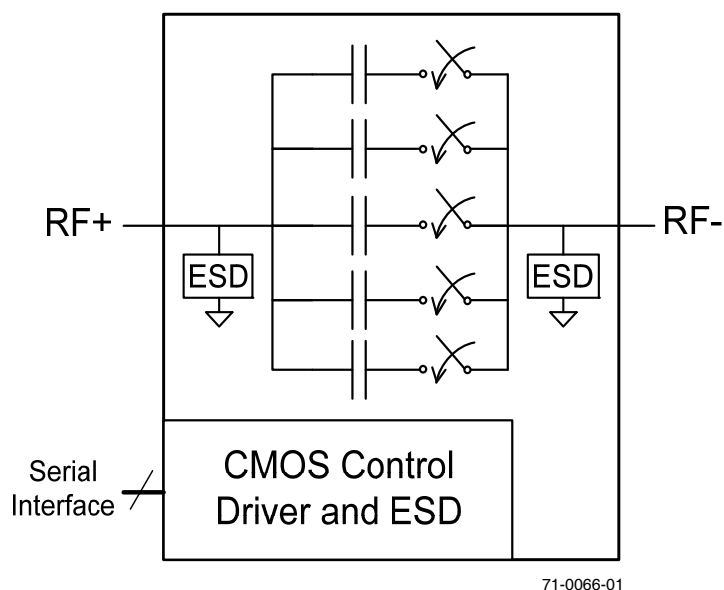
General Description

The PE64102 is a DuNE™-enhanced Digitally Tunable Capacitor (DTC) based on Peregrine's UltraCMOS® technology. DTC products provide a monolithically integrated impedance tuning solution for demanding RF applications. They also offer a linear capacitance change versus tuning state and excellent harmonic performance compared to varactor-based tunable solutions.

This highly versatile product can be mounted in series or shunt configurations and uses a 3-wire (SPI compatible) serial interface. It has a high ESD rating of 2 kV HBM on all ports making this the ultimate in integration and ruggedness. The DTC will be offered in a standard 12-lead 2.0 x 2.0 x 0.55 mm QFN commercial package.

Peregrine's DuNE™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS® process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Block Diagram



UltraCMOS® Digitally Tunable Capacitor (DTC) 100 - 3000 MHz

Features

- 3-wire (SPI compatible) 8-bit serial interface with built-in bias voltage generation and stand-by mode for reduces power consumption
- DuNE™-enhanced UltraCMOS® device
- 5-bit 32-state Digitally Tunable Capacitor
- $C = 1.88 - 14.0$ pF (7.4:1 tuning ratio) in discrete 391 fF steps
- RF power handling (up to 26 dBm, 6 V_{PK} RF) and high linearity
- High quality factor
- Wide power supply range (2.3 to 3.6V) and low current consumption (typ. I_{DD} = 30 μA @ 2.8V)
- Optimized for shunt configuration, but can also be used in series configuration
- Excellent 2 kV HBM ESD tolerance on all pins
- Applications include:
 - Antenna tuning
 - Tunable filters
 - Phase shifters
 - Impedance matching

Figure 2. Package Type
12-lead 2 x 2 x 0.55 mm QFN

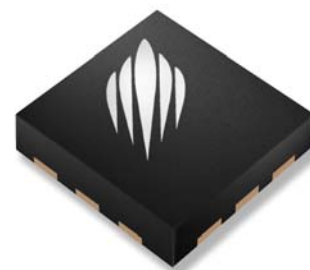


Table 1. Electrical Specifications @ 25°C, V_{DD} = 2.8V

Parameter	Configuration	Condition	Min	Typ	Max	Unit
Operating Frequency Range ⁷	Both		100		3000	MHz
Minimum Capacitance	Shunt ⁶	State = 00000, 100 MHz (RF+ to Grounded RF-)	-10%	1.88	+10%	pF
Maximum Capacitance	Shunt ⁶	State = 11111, 100 MHz (RF+ to Grounded RF-)	-10%	14.0	+10%	pF
Tuning Ratio	Shunt ⁶	C _{max} /C _{min} , 100 MHz		7.4:1		
Step Size	Shunt ⁶	5 bits (32 states), constant step size (100 MHz)		0.391		pF
Quality Factor (C _{min}) ¹	Shunt ⁶	470 - 582 MHz with L _s removed 698 - 960 MHz, with L _s removed 1710 - 2170 MHz, with L _s removed		50 50 28		
Quality Factor (C _{max}) ¹	Shunt ⁶	470 - 582 MHz with L _s removed 698 - 960 MHz, with L _s removed 1710 - 2170 MHz, with L _s removed		25 20 5		
Self Resonant Frequency	Shunt ⁷	State 00000 State 11111		4.7 1.6		GHz
Harmonics (2 _{fo} and 3 _{fo}) ⁴	Shunt ⁶	470 to 582 MHz, Pin +26 dBm, 50Ω 698 to 915 MHz, Pin +26 dBm, 50Ω 1710 to 1910 MHz, Pin +26 dBm, 50Ω			-36 -36 -36	dBm dBm dBm
	Series ⁵	470 to 582 MHz, Pin +20 dBm, 50Ω 698 to 915 MHz, Pin +20 dBm, 50Ω 1710 to 1910 MHz, Pin +20 dBm, 50Ω			-36 -36 -36	dBm dBm dBm
3rd Order Intercept Point	Shunt ⁶	IIP3 = (Pblocker + 2*Ptx - [IMD3]) / 2, where IMD3 = -95 dBm, Ptx = +20 dBm and Pblocker = -15 dBm		60		dBm
Switching Time ^{2,3}	Shunt ⁶	State change to 10/90% delta capacitance between only two states		2	10	μs
Start-up Time ²	Shunt ⁶	Time from V _{DD} within specification to all performances within specification		5	20	μs
Wake-up Time ^{2,3}	Shunt ⁶	State change from standby mode to RF state to all performances within specification		5	20	μs

- Note: 1. Q for a Shunt DTC based on a Series RLC equivalent circuit
 $Q = X_C / R = (X - X_L) / R$, where $X = X_L + X_C$, $X_L = 2\pi f L$, $X_C = -1 / (2\pi f C)$, which is equal to removing the effect of parasitic inductance L_s
2. DC path to ground at RF+ and RF- must be provided to achieve specified performance
3. State change activated on falling edge of SEN following data word
4. Between 50Ω ports in series or shunt configuration using a pulsed RF input with 4620 vs period, 50% duty cycle, measured per 3GPPTS45.005
5. In series configuration the greater RF power or higher RF voltage should be applied to RF+
6. RF- should be connected to ground
7. DTC operation above SRF is possible

Figure 3. Pin Configuration (Top View)

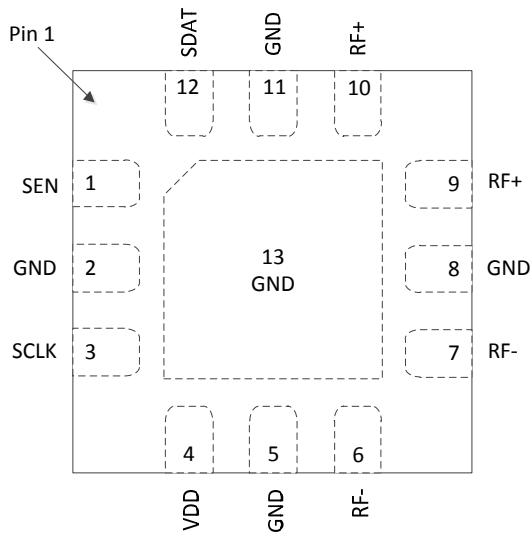


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	SEN	Serial Enable
2	GND	Digital and RF Ground
3	SCLK	Serial Interface Clock Input
4	VDD	Power Voltage
5	GND	Digital and RF Ground
6	RF-	Negative RF Port ¹
7	RF-	Negative RF Port ¹
8	GND	Digital and RF Ground ³
9	RF+	Positive RF Port ²
10	RF+	Positive RF Port ²
11	GND	Digital and RF Ground
12	SDAT	Serial Interface Data Input
13	GND	Digital and RF Ground ³

Notes: 1. Pins 6 and 7 must be tied together on PCB board to reduce inductance
 2. Pins 9 and 10 must be tied together on PCB board to reduce inductance
 3. Pins 2, 5, 8, 11 and 13 must be connected together on PCB

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE64102 in the 12-lead 2 x 2 QFN package is MSL1.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS[®] devices are immune to latch-up.

Table 3. Operating Ranges¹

Parameter	Symbol	Min	Typ	Max	Units
V _{DD} Supply Voltage	V _{DD}	2.3	2.8	3.6	V
I _{DD} Power Supply Current (Normal mode) ⁶	I _{DD}		30	75	μA
I _{DD} Power Supply Current (Standby mode) ⁶	I _{DD}		20	45	μA
Control Voltage High	V _{IH}	1.2		3.1	V
Control Voltage Low	V _{IL}	0		0.2	V
Peak Operating RF Voltage ⁵				6	V _{PK}
V _P to V _M				6	V _{PK}
V _P to RFGND				6	V _{PK}
V _M to RFGND				6	V _{PK}
RF Input Power (50Ω) ^{3,4,5}				+26	dBm
shunt				+20	dBm
series					
Input Control Current	I _{CTL}		1	10	μA
Operating Temperature Range	T _{OP}	-40		+85	°C
Storage Temperature Range	T _{ST}	-65		+150	°C

Notes: 1. Operation should be restricted to the limits in the Operating Ranges table
 2. The DTC is active when STBY is low (set to 0) and in low-current stand-by mode when high (set to 1)
 3. Maximum CW power available from a 50Ω source in shunt configuration
 4. Maximum CW power available from a 50Ω source in series configuration
 5. RF+ to RF- and RF+ and/or RF- to ground. Cannot exceed 6 V_{PK} or max RF input power (whichever occurs first)
 6. I_{DD} current typical value is based on V_{DD} = 2.8V. Max I_{DD} is based on V_{DD} = 3.6V

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V _{DD}	Power supply voltage	-0.3	4.0	V
V _I	Voltage on any DC input	-0.3	4.0	V
V _{ESD}	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		2000	V
V _{ESD}	ESD Voltage (MM, JEDEC JESD22-A115-A)		100	V

Exceeding absolute maximum ratings may cause permanent damage. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS[®] device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Figure 4. Package Drawing
12-lead 2 x 2 x 0.55 mm QFN

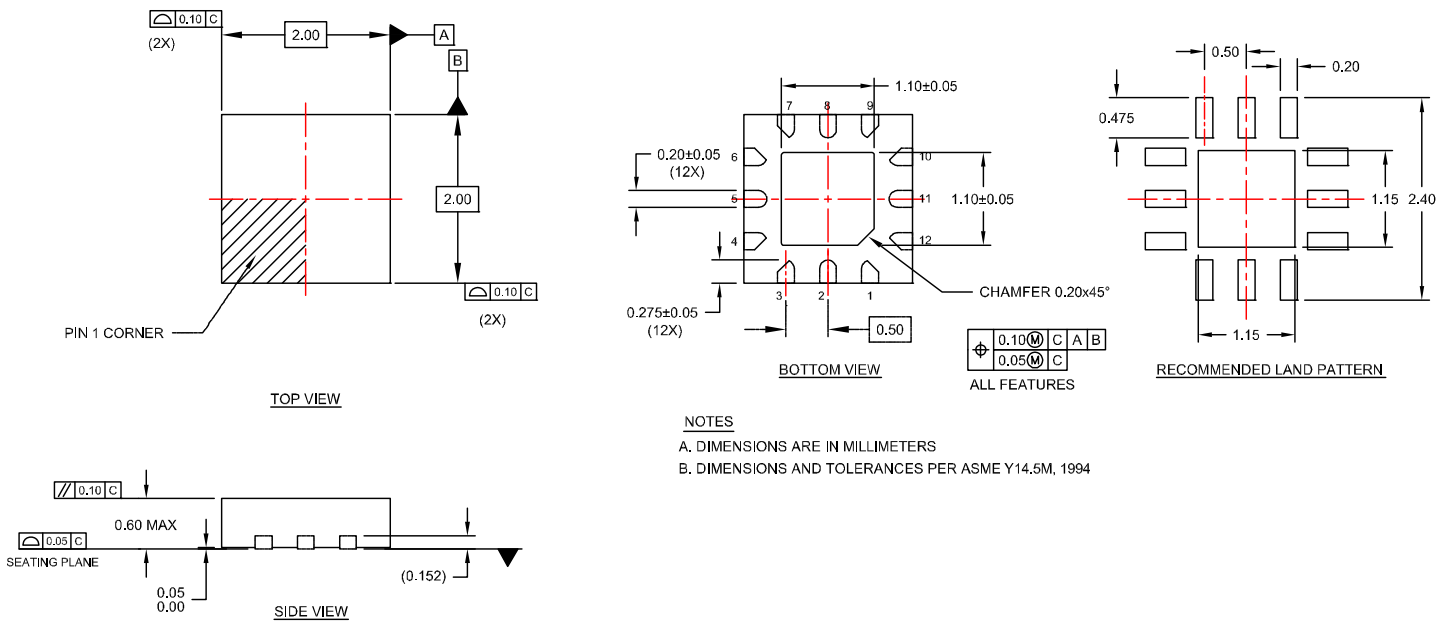
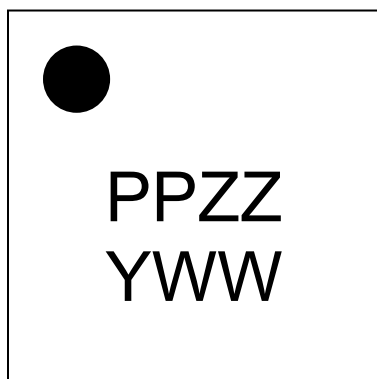


Figure 5. Top Marking Specifications



17-0112

Marking Spec Symbol	Package Marking	Definition
PP	CS	Part number marking for PE64102
ZZ	00-99	Last two digits of lot code
Y	0-9	Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc)
WW	01-53	Work week

Figure 6. Tape and Reel Specifications
12-lead 2 x 2 x 0.55 mm QFN

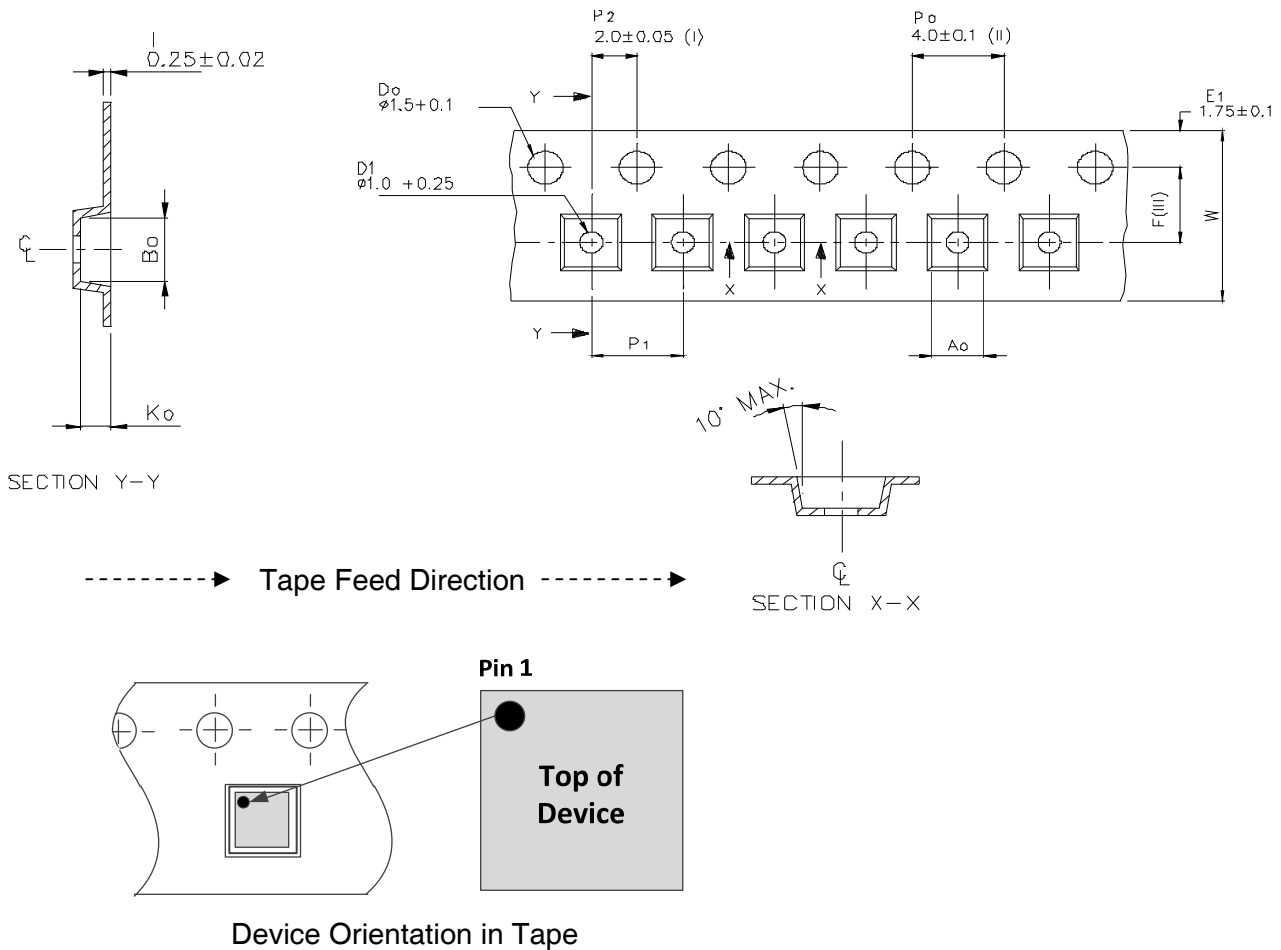


Table 5. Ordering Information

Order Code	Package	Description	Shipping Method
PE64102MLAA-Z	12-lead 2 x 2 x 0.55 mm QFN	Package Part in Tape and Reel	3000 units/T&R
EK64102-11	Evaluation Kit	Evaluation Kit	1 Set/Box

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