Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

HMCAD1520

v04.1015

HIGH SPEED MULTI-MODE 8/12/14-BIT 1000/640/105 MSPS A/D CONVERTER

Features

- High Speed Modes (12-bit / 8-bit)
  Quad Channel Mode: F_{Smax} = 160 / 250 MSPS
  Dual Channel Mode: F_{Smax} = 320 / 500 MSPS
  Single Channel Mode: F_{Smax} = 640 / 1000 MSPS
  SNR: 70 dB, SFDR: 60/75 dB [1] (12-bit 1ch Mode)
- 8-bit Modes Described in
  HMCAD1511 and HMCAD1510
- Precision Mode (14-bit)
  Four channels up to 105 MSPS
  SNR: 74 dB, SFDR: 83 dB @ 70 MHz
  SNR: 72.5 dB, SFDR: 78 dB @ 140 MHz
- Integrated Cross Point Switches with instantaneous switching
- Internal low jitter programmable Clock Divider
- Ultra Low Power Dissipation
  490 mW including I/O at 12-bit 640 MSPS
- 0.5 µs start-up time from Sleep, 15 µs from Power Down
- Internal reference circuitry with no external components required
- Coarse and fine gain control
- Digital fine gain adjustment for each ADC
- Internal offset correction
- 1.8 V supply voltage
- 1.7 - 3.6 V CMOS logic on control interface pins
- Serial LVDS output
  12, 14, 16 and Dual 8-bit modes available
- 7 x 7 mm 48 QFN Package

[1] Including/Excluding Interleaving Spurs

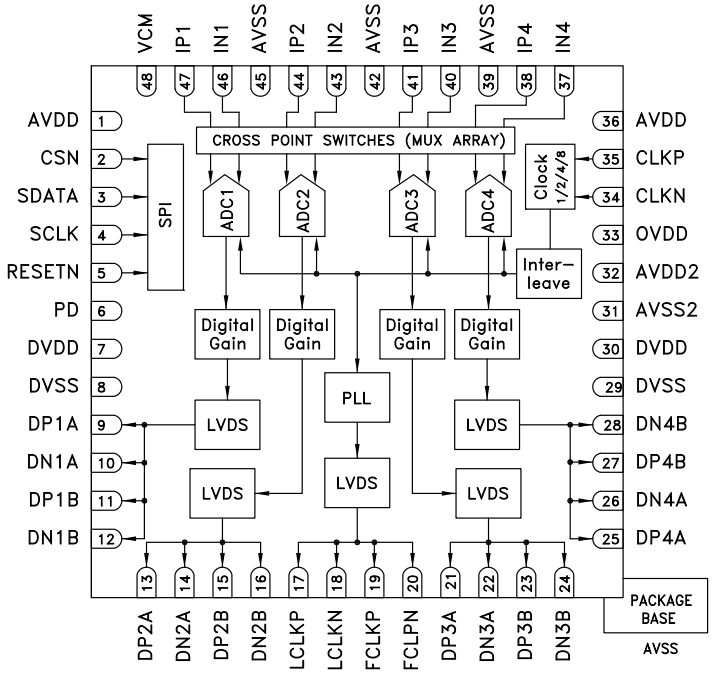
Typical Applications

- Precision Oscilloscopes
- Spectrum Analyzers
- Diversity Receivers
- Hi-End Ultrasound
- Communication Testing
- Non Destructive Testing

Pin compatible parts

HMCAD1520 is pin compatible and can be configured to operate as HMCAD1511 and HMCAD1510, with functionality and performance as described in HMCAD1511 and HMCAD1510 datasheets.

Functional Diagram



Functional Block Diagram

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

HMCAD1520* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMCAD1520 Evaluation Board

DOCUMENTATION

Data Sheet

- HMCAD1520: High Speed Multi-Mode 8/12/14-Bit 1000/640/105 MSPS A/D Converter Data Sheet

REFERENCE MATERIALS

Quality Documentation

- Semiconductor Qualification Test Report: CMOS-C (QTR: 2013-00139)

DESIGN RESOURCES

- HMCAD1520 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMCAD1520 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

HIGH SPEED MULTI-MODE 8/12/14-BIT 1000/640/105 MSPS A/D CONVERTER

General Description

The HMCAD1520 is a versatile high performance low power analog-to-digital converter (ADC), with interleaving High Speed Modes to increase sampling rate. Integrated Cross Point Switches activate the input selected by the user.

In Single Channel Mode, one of the four inputs can be selected as valid input to the single ADC channel. In Dual Channel Mode, any two of the four inputs can be selected to each ADC channel. In Quad Channel Mode and Precision Mode, any input can be assigned to any ADC channel.

An internal, low jitter and programmable clock divider makes it possible to use a single clock source for all operational modes.

The HMCAD1520 is based on a proprietary structure, and employs internal reference circuitry, a serial control interface and a serial LVDS output data. Data and frame synchronization clocks are supplied for data capture at the receiver. Internal digital fine gain can be set separately for each ADC to calibrate for gain errors.

Various modes and configuration settings can be applied to the ADC through the serial control interface (SPI). each channel can be powered down independently and output data format can be selected through this interface. A full chip idle mode can be set by a single external pin. Register settings determine the exact function of this pin.

HMCAD1520 is designed to interface easily with Field Programmable Gate Arrays (FPGAs) from several vendors.

Electrical Specifications

DC Specifications

AVDD = DVDD = OVDD = 1.8V, F_S = 160 MSPS, Quad Channel 12-bit High Speed Mode, 50% Clock Duty Cycle, -1 dBFS 70 MHz Input Signal, 1x / 0 dB Digital Gain (Fine and Coarse), Unless Otherwise Noted

Parameter	Description	Min	Typ	Max	Unit
DC accuracy					
No missing codes		Guaranteed			
Offset	Offset error after internal digital offset correction		1		LSB
G_{abs}	Gain error			±6	%FS
G_{rel}	Gain matching between channels. ±3 sigma value at worst case conditions		±0.5		%FS
DNL	Differential non linearity		±0.2		LSB
INL	Integral non linearity		±0.6		LSB
$V_{CM,out}$	Common mode voltage output		V_{AVDD}/2		
Analog Input					
$V_{CM,in}$	Analog input common mode voltage	V_{CM} -0.1		V_{CM} +0.2	V
FSR	Differential input voltage full scale range		2		Vpp
$C_{in,Q}$	Differential input capacitance, Quad channel mode		5		pF
$C_{in,D}$	Differential input capacitance, Dual channel mode		7		pF
$C_{in,S}$	Differential input capacitance, Single channel mode		11		pF
Power Supply					
V_{AVDD}	Analog Supply Voltage	1.7	1.8	2	V
V_{DVDD}	Digital and output driver supply voltage	1.7	1.8	2	V
V_{OVDD}	Digital CMOS Input Supply Voltage	1.7	1.8	3.6	V
Temperature					
T_A	Operating free-air temperature	-40		85	°C

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

AC Specifications – High Speed Modes

AVDD = DVDD = OVDD = 1.8V, 50% clock duty cycle, -1 dBFS 70 MHz input signal, Gain = 1X, 12-bit output, RSDS output data levels, unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
Performance					
SNR	Signal to Noise Ratio, excluding interleaving spurs				
	Single Channel Mode , F_S = 640 MSPS		70		dBFS
	Dual Channel Mode , F_S = 320 MSPS		70		dBFS
	Quad Channel Mode , F_S = 160 MSPS		70		dBFS
$SINAD_{incl}$	Signal to Noise and Distortion Ratio, including interleaving spurs				
	Single Channel Mode , F_S = 640 MSPS		58		dBFS
	Dual Channel Mode , F_S = 320 MSPS		58		dBFS
	Quad Channel Mode , F_S = 160 MSPS		58		dBFS
$SINAD_{excl}$	Signal to Noise and Distortion Ratio, excluding interleaving spurs				
	Single Channel Mode , F_S = 640 MSPS		67		dBFS
	Dual Channel Mode , F_S = 320 MSPS		68		dBFS
	Quad Channel Mode , F_S = 160 MSPS		68		dBFS
$SFDR_{incl}$	Spurious Free Dynamic Range, including interleaving spurs				
	Single Channel Mode , F_S = 640 MSPS		60		dBc
	Dual Channel Mode , F_S = 320 MSPS		60		dBc
	Quad Channel Mode , F_S = 160 MSPS		60		dBc
$SFDR_{excl}$	Spurious Free Dynamic Range, excluding interleaving spurs				
	Single Channel Mode , F_S = 640 MSPS		75		dBc
	Dual Channel Mode , F_S = 320 MSPS		77		dBc
	Quad Channel Mode , F_S = 160 MSPS		78		dBc
HD2/3	Worst of HD2/HD3				
	Single Channel Mode , F_S = 640 MSPS		75		dBc
	Dual Channel Mode , F_S = 320 MSPS		77		dBc
	Quad Channel Mode , F_S = 160 MSPS		78		dBc
ENOB	Effective number of Bits				
	Single Channel Mode , F_S = 640 MSPS		10.8		bits
	Dual Channel Mode , F_S = 320 MSPS		11.0		bits
	Quad Channel Mode , F_S = 160 MSPS		11.0		bits
$X_{tlk,HS2}$	CrossTalk Dual Ch Mode. Signal applied to 1 channel (F_{IN0}). Measurement taken on one channel with full scale at F_{IN1}. F_{IN1} = 71 MHz, F_{IN0} = 70 MHz		70		dBc
$X_{tlk,HS4}$	CrossTalk Quad Ch Mode. Signal applied to 1 channel (F_{IN0}). Measurement taken on one channel with full scale at F_{IN1}. F_{IN1} = 71 MHz, F_{IN0} = 70 MHz		70		dBc
Power Supply	Single Ch: F_S = 640 MSPS, Dual Ch: F_S = 320 MSPS, Quad Ch: F_S = 160 MSPS.				
I_{AVDD}	Analog Supply Current		190		mA
I_{DVDD}	Digital and output driver Supply Current		82		mA
P_{AVDD}	Analog Power		342		mW

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

RoHS✓ EARTH FRIENDLY

HIGH SPEED MULTI-MODE 8/12/14-BIT 1000/640/105 MSPS A/D CONVERTER

AC Specifications – High Speed Modes

AVDD = DVDD = OVDD = 1.8V, 50% clock duty cycle, -1 dBFS 70 MHz input signal, Gain = 1X, 12-bit output, RSDS output data levels, unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
P_{DVDD}	Digital Power		148		mW
P_{TOT}	Total Power Dissipation		490		mW
P_{PD}	Power Down Mode Dissipation		15		µW
P_{SLP}	Deep Sleep Mode Power Dissipation		66		mW
P_{SLPCH}	Power Dissipation with all channels in sleep channel mode (Light Sleep)		121		mW
P_{SLPCH_SAV}	Power Dissipation savings per channel off		92		mW
Analog Input					
FPBW	Full Power Bandwidth		700		MHz
Clock Inputs					
F_{Smax}	Max. Conversion Rate in Modes: Single / Dual Quad Channel	 640/320 160			MSPS
F_{Smin}	Min. Conversion Rate in Modes: Single / Dual Quad Channel			 120/60 30	MSPS

AC Specifications – Precision Mode

AVDD = DVDD = OVDD = 1.8V, FS = 105 MHz, 50% clock duty cycle, -1 dBFS 70 MHz input signal, Gain = 1X, dual 8-bit output, RSDS output data levels, unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
Performance					
SNR	Signal to Noise Ratio				
	F_S = 80 MSPS		75		dBFS
	F_S = 105 MSPS		74		dBFS
	F_S = 105 MSPS, F_{in} = 105 MSPS		72.5		dBFS
SINAD	Signal to Noise and Distortion Ratio				
	F_S = 80 MSPS		73		dBFS
	F_S = 105 MSPS		72.5		dBFS
	F_S = 105 MSPS, F_{in} = 105 MSPS		71		dBFS
SFDR	Spurious Free Dynamic Range				
	F_S = 80 MSPS		85		dBc
	F_S = 105 MSPS		83		dBc
	F_S = 105 MSPS, F_{in} = 105 MSPS		78		dBc
HD2	Second order harmonic spur				
	F_S = 80 MSPS		90		dBc
	F_S = 105 MSPS		90		dBc
	F_S = 105 MSPS, F_{in} = 105 MSPS		80		dBc
HD3	Third order harmonic spur				

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

RoHS✓ EARTH FRIENDLY

HIGH SPEED MULTI-MODE 8/12/14-BIT 1000/640/105 MSPS A/D CONVERTER

AC Specifications – Precision Mode

AVDD = DVDD = OVDD = 1.8V, FS = 105 MHz, 50% clock duty cycle, -1 dBFS 70 MHz input signal, Gain = 1X, dual 8-bit output, RSDS output data levels, unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
	F_S = 80 MSPS		85		dBc
	F_S = 105 MSPS		83		dBc
	F_S = 105 MSPS, F_{in} = 105 MSPS		78		dBc
ENOB	Effective number of Bits				
	F_S = 80 MSPS		11.8		bits
	F_S = 105 MSPS		11.8		bits
	F_S = 105 MSPS, F_{in} = 105 MSPS		11.5		bits
X_{tlk}	CrossTalk. Signal applied to 1 channel (F_{IN0}). Measurement taken on one channel with full scale at F_{IN1} . F_{IN1} = 71 MHz, F_{IN0} = 70 MHz		70		dBc
Power Supply					
I_{AVDD}	Analog Supply Current		229		mA
I_{DVDD}	Digital and output driver Supply Current		106		mA
P_{AVDD}	Analog Power		412		mW
P_{DVDD}	Digital Power		191		mW
P_{TOT}	Total Power Dissipation		603		mW
P_{PD}	Power Down Mode Dissipation		15		µW
P_{SLP}	Deep Sleep Mode Power Dissipation		66		mW
P_{SLPCH}	Power Dissipation with all channels in sleep channel mode (Light Sleep)		131		mW
P_{SLPCH_SAV}	Power Dissipation savings per channel off		118		mW
Analog Input					
FPBW	Full Power Bandwidth		700		MHz
Clock Inputs					
F_{Smax}	Max. Conversion Rate	105			MSPS
F_{Smin}	Min. Conversion Rate			15	MSPS

Digital and Switching Specifications

AVDD = DVDD = OVDD = 1.8V, RSDS output data levels, unless otherwise noted.

Parameter	Description	Min	Typ	Max	Unit
Clock Inputs					
DC	Duty Cycle, High speed modes	40		60	% high
DC	Duty Cycle, Precision mode	30		70	% high
Compliance	LVDS supported up to 700 Mbps	LVPECL, Sine wave, CMOS, LVDS			
$V_{CK,sine}$	Differential input voltage swing, sine wave clock input	1500			mVpp
$V_{CK,CMOS}$	Voltage input range CMOS (CLKN connected to ground)		V_{OVDD}		
$V_{CM,CK}$	Input common mode voltage. Keep voltages within ground and voltage of OVDD	0.3		V_{OVDD} -0.3	V
C_{CK}	Differential Input capacitance		3		pF
Logic inputs (CMOS)					

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

RoHS✓ EARTH FRIENDLY

HIGH SPEED MULTI-MODE 8/12/14-BIT 1000/640/105 MSPS A/D CONVERTER

Digital and Switching Specifications

AVDD = DVDD = OVDD = 1.8V, RSDS output data levels, unless otherwise noted.

Parameter	Description	Min	Typ	Max	Unit
V_{HI}	High Level Input Voltage. V_{OVDD} ≥ 3.0V	2			V
V_{HI}	High Level Input Voltage. V_{OVDD} = 1.7V – 3.0V	0.8 ·V_{OVDD}			V
V_{LI}	Low Level Input Voltage. V_{OVDD} ≥ 3.0V	0		0.8	V
V_{LI}	Low Level Input Voltage. V_{OVDD} = 1.7V – 3.0V	0		0.2 ·V_{OVDD}	V
I_{HI}	High Level Input leakage Current			+/-10	µA
I_{LI}	Low Level Input leakage Current			+/-10	µA
C_I	Input Capacitance		3		pF
Data outputs					
Compliance		LVDS / RSDS			
V_{OUT}	Differential output voltage, LVDS		350		mV
V_{OUT}	Differential output voltage, RSDS		150		mV
V_{CM}	Output common mode voltage		1.2		V
Output coding	Default/optional	Offset Binary/ 2's complement			
Timing Characteristics					
$t_{A,HS}$	Aperture delay, High speed modes		1.5		ns
$t_{A,PM}$	Aperture delay, Precision mode		1.4		ns
$t_{j,HS}$	Aperture jitter, all bits set to '1' in jitter_ctrl<7:0>, High speed modes		120		fsrms
$t_{j,HS}$	Aperture jitter, one bit set to '1' in jitter_ctrl<7:0>, High speed modes		160		fsrms
$t_{j,PM}$	Aperture jitter, all bits set to '1' in jitter_ctrl<7:0>, Precision modes		75		fsrms
$t_{j,PM}$	Aperture jitter, one bit set to '1' in jitter_ctrl<7:0>, Precision modes		130		fsrms
T_{skew}	Timing skew between ADC channels, High speed modes		2.5		psrms
T_{SU}	Start up time from Power Down Mode and Deep Sleep Mode to Active Mode in µs. See section "Clock Frequency" for details.		15		µs
T_{SLPCH}	Start up time from Sleep Channel Mode to Active Mode		0.5		µs
T_{OVR}	Out of range recovery time		1		clock cycles
T_{LATPM}	Pipeline delay, Precision Speed Mode		15		clock cycles
$T_{LATHSMQ}$	Pipeline delay, Quad High Speed Mode		32		clock cycles
$T_{LATHSMD}$	Pipeline delay, Dual High Speed Mode		64		clock cycles
$T_{LATHSMS}$	Pipeline delay, Single High Speed Mode		128		clock cycles
LVDS Output Timing Characteristics					
t_{data}	LCLK to data delay time (excluding programmable phase shift)		50		ps
T_{PROP}	Clock propagation delay.	6*T_{LVDS} +2.2	7*T_{LVDS} +3.5	7*T_{LVDS} +5.0	ns
	LVDS bit-clock duty-cycle	45		55	% LCLK cycle
	Frame clock cycle-to-cycle jitter			2.5	% LCLK cycle
T_{EDGE}	Data rise- and fall time 20% to 80%		0.7		ns
$T_{CLKEDGE}$	Clock rise- and fall time 20% to 80%		0.7		ns

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Absolute Maximum Ratings

Applying voltages to the pins beyond those specified in Table 1 could cause permanent damage to the circuit.

Table 1: Maximum voltage ratings

Pin	Reference pin	Rating
AVDD	AVSS	-0.3V to +2.3V
DVDD	DVSS	-0.3V to +2.3V
OVDD	AVSS	-0.3V to +3.9V
AVSS / DVSS	DVSS / AVSS	-0.3V to +0.3V
Analog inputs and outputs	AVSS	-0.3V to +2.3V
CLKx	AVSS	-0.3V to +3.9V
LVDS outputs	DVSS	-0.3V to +2.3V
Digital inputs	DVSS	-0.3V to +3.9V

Table 2 shows the maximum external temperature ratings.

Table 2: Maximum Temperature Ratings

Operating Temperature	-40 to +85 ºC
Storage Temperature	-60 to +150 ºC
Maximum Junction Temperature	110 ºC
Thermal Resistance (Rth)	29 ºC/W
Soldering Profile Qualification	J-STD-020
ESD Sensivity HBM	Class 1C
ESD Sensivity CDM	Class III

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

RoHS✓ EARTH FRIENDLY

HIGH SPEED MULTI-MODE 8/12/14-BIT 1000/640/105 MSPS A/D CONVERTER

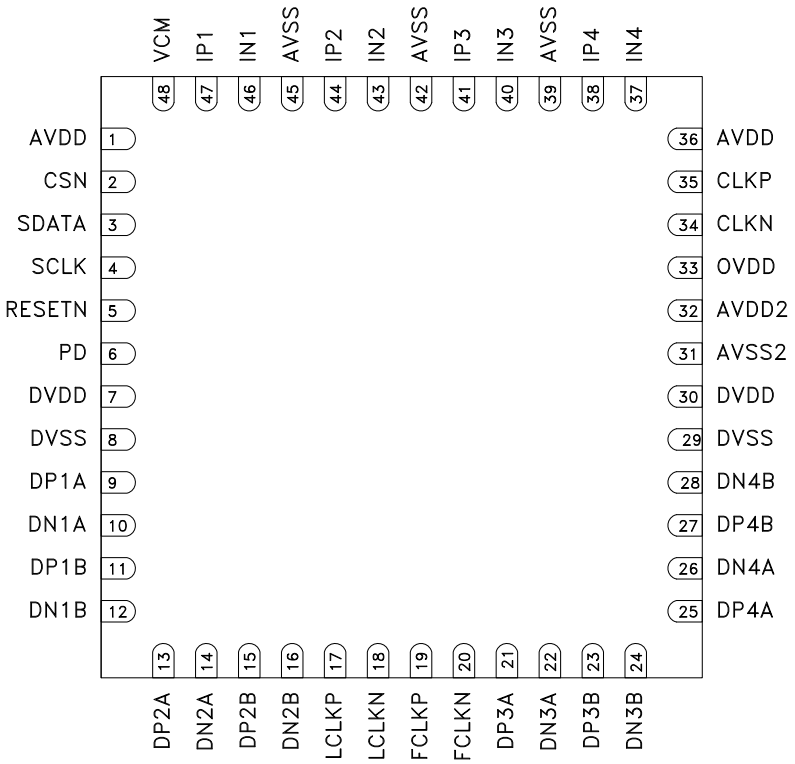


Figure 1: Pin Diagram

Table 3: Pin Descriptions

Pin name	Description	Pin Number	# of Pins
AVDD	Analog power supply, 1.8V	1, 36	2
CSN	Chip select enable. Active low	2	1
SDATA	Serial data input	3	1
SCLK	Serial clock input	4	1
RESETN	Reset SPI interface. Active low	5	1
PD	Power-down input. Activate after applying power in order to initialize the ADC correctly. Alternatively use the SPI power down feature	6	1
DVDD	Digital and I/O power supply, 1.8V	7, 30	2
DVSS	Digital ground	8, 29	2
DP1A	LVDS channel 1A, positive output	9	1
DN1A	LVDS channel 1A, negative output	10	1
DP1B	LVDS channel 1B, positive output	11	1
DN1B	LVDS channel 1B, negative output	12	1
DP2A	LVDS channel 2A, positive output	13	1
DN2A	LVDS channel 2A, negative output	14	1
DP2B	LVDS channel 2B, positive output	15	1
DN2B	LVDS channel 2B, negative output	16	1

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Table 3: Pin Descriptions

Pin name	Description	Pin Number	# of Pins
LCLKP	LVDS bit clock, positive output	17	1
LCLKN	LVDS bit clock, negative output	18	1
FCLKP	LVDS frame clock (1X), positive output	19	1
FCLKN	LVDS frame clock (1X), negative output	20	1
DP3A	LVDS channel 3A, positive output	21	1
DN3A	LVDS channel 3A, negative output	22	1
DP3B	LVDS channel 3B, positive output	23	1
DN3B	LVDS channel 3B, negative output	24	1
DP4A	LVDS channel 4A, positive output	25	1
DN4A	LVDS channel 4A, negative output	26	1
DP4B	LVDS channel 4B, positive output	27	1
DN4B	LVDS channel 4B, negative output	28	1
AVSS2	Analog ground domain 2	31	1
AVDD2	Analog power supply domain 2, 1.8V	32	1
OVDD	Digital CMOS Inputs supply voltage	33	1
CLKN	Negative differential input clock.	34	1
CLKP	Positive differential input clock	35	1
IN4	Negative differential input signal, channel 4	37	1
IP4	Positive differential input signal, channel 4	38	1
AVSS	Analog ground	39, 42, 45	3
IN3	Negative differential input signal, channel 3	40	1
IP3	Positive differential input signal, channel 3	41	1
IN2	Negative differential input signal, channel 2	43	1
IP2	Positive differential input signal, channel 2	44	1
IN1	Negative differential input signal, channel 1	46	1
IP1	Positive differential input signal, channel 1	47	1
VCM	Common mode output pin, 0.5*AVDD	48	1

Start up Initialization

As part of the HMCAD1520 power-on sequence both a reset and a power down cycle have to be applied to ensure correct start-up initialization. Reset can be done in one of two ways:

1. By applying a low-going pulse (minimum 20 ns) on the RESETN pin (asynchronous).
2. By using the serial interface to set the ‘rst’ bit high. Internal registers are reset to default values when this bit is set. The ‘rst’ bit is self-reset to zero. When using this method, do not apply any low-going pulse on the RESETN pin.

Power down cycling can be done in one of two ways:

1. By applying a high-going pulse (minimum 20 ns) on the PD pin (asynchronous).
2. By cycling the ‘pd’ bit in register 0Fhex to high (reg value ‘0200’hex) and then low (reg value ‘0000’hex).

Register Initialization

To set the HMCAD1520 in Precision Mode, the following registers must be changed from the default value. Suggested values are:

Address	Data	Function
0x31	0x0008	Sets HMCAD1520 in precision mode, Clock divider to 1
0x53	0x0004	Sets the LVDS output in dual 8 bit mode

Serial Interface

The HMCAD1520 configuration registers can be accessed through a serial interface formed by the pins SDATA (serial interface data), SCLK (serial interface clock) and CSN (chip select, active low). The following occurs when CSN is set low:

- Serial data are shifted into the chip
- At every rising edge of SCLK, the value present at SDATA is latched
- SDATA is loaded into the register every 24th rising edge of SCLK

Multiples of 24-bit words data can be loaded within a single active CSN pulse. If more than 24 bits are loaded into SDATA during one active CSN pulse, only the first 24 bits are kept. The excess bits are ignored. Every 24-bit word is divided into two parts:

- The first eight bits form the register address
- The remaining 16 bits form the register data

Acceptable SCLK frequencies are from 20MHz down to a few hertz. Duty-cycle does not have to be tightly controlled.

Timing Diagram

Figure 2 shows the timing of the serial port interface. Table 4 explains the timing variables used in figure 2.

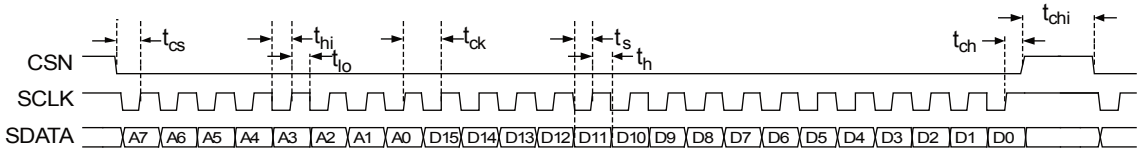


Figure 2: Serial Port Interface timing

Table 4: Serial Port Interface Timing Definitions

Parameter	Description	Minimum value	Unit
t_{cs}	Setup time between CSN and SCLK	8	ns
t_{ch}	Hold time between CSN and SCLK	8	ns
t_{hi}	SCLK high time	20	ns
t_{lo}	SCLK low time	20	ns
t_{ck}	SCLK period	50	ns
t_{s}	Data setup time	5	ns
t_{h}	Data hold time	5	ns

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Timing Diagrams

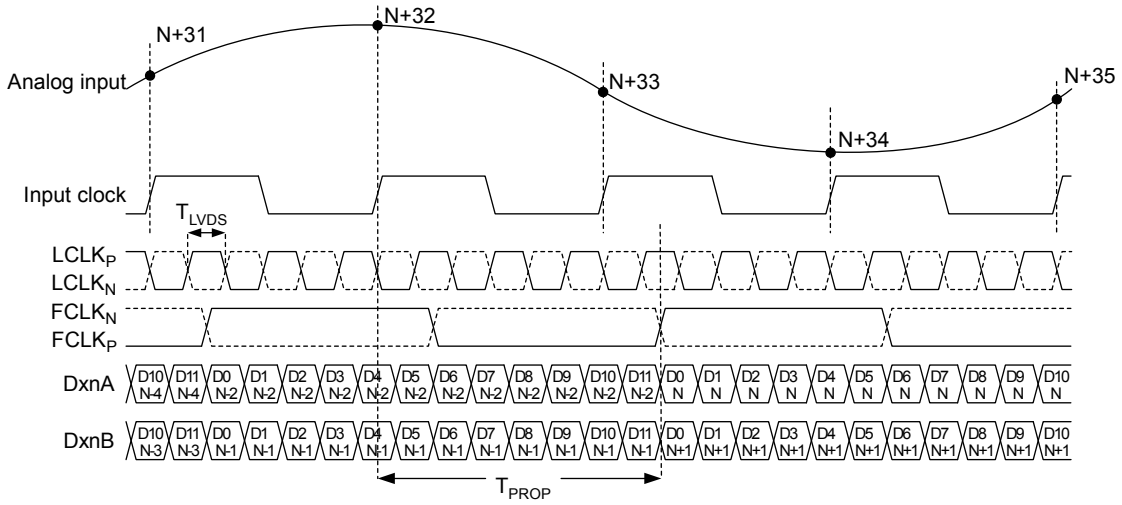


Figure 3: Quad channel - LVDS timing 12-bit output

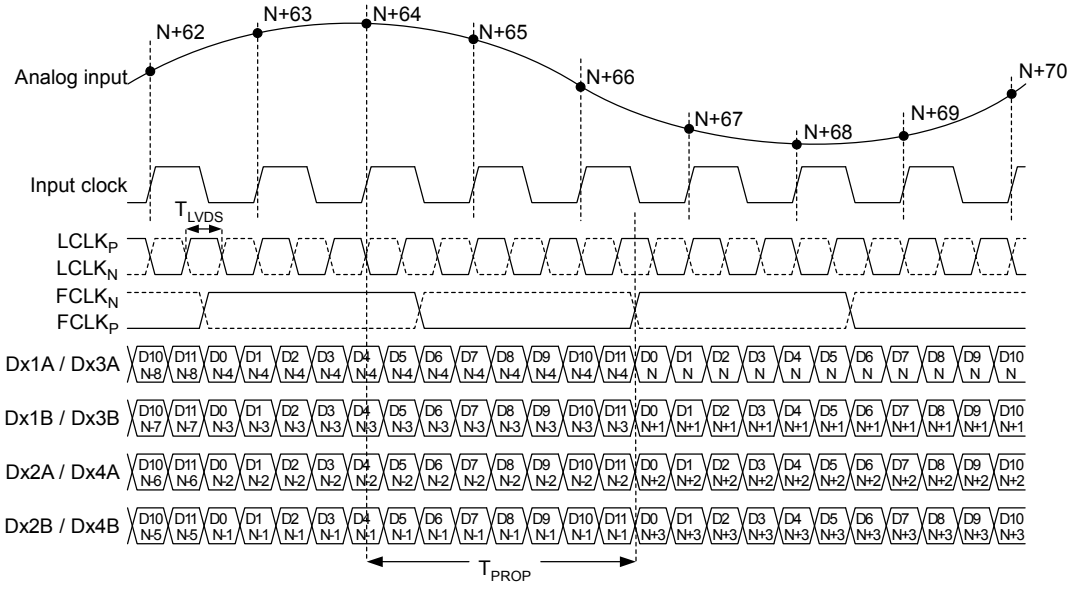


Figure 4: Dual channel - LVDS timing 12-bit output

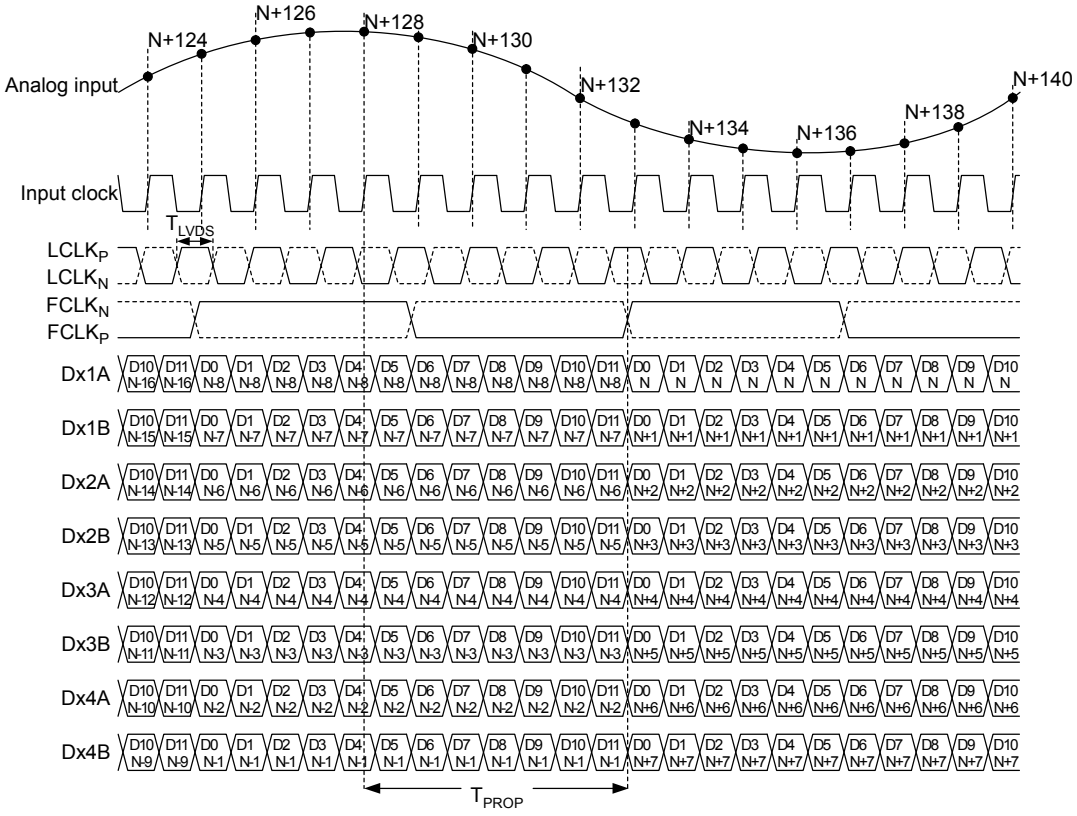


Figure 5: Single channel - LVDS timing 12-bit output

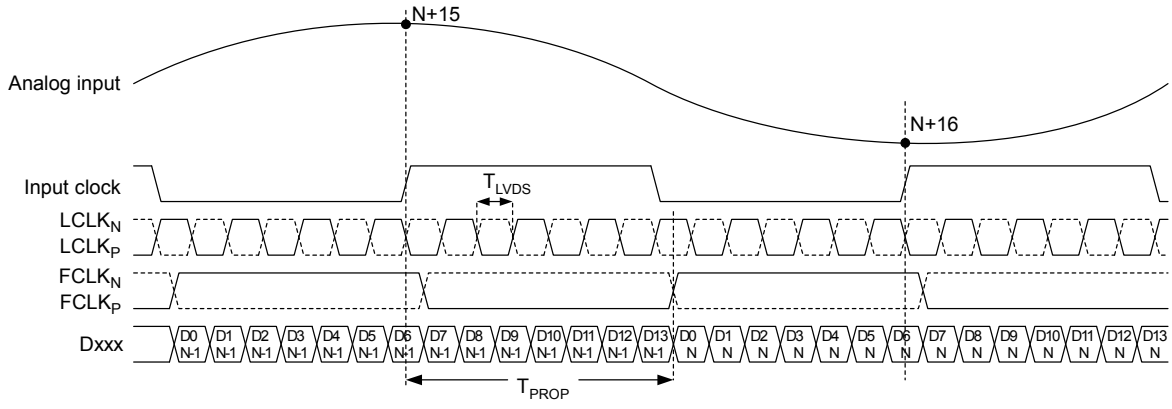


Figure 6: Precision - LVDS timing 14-bit output

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

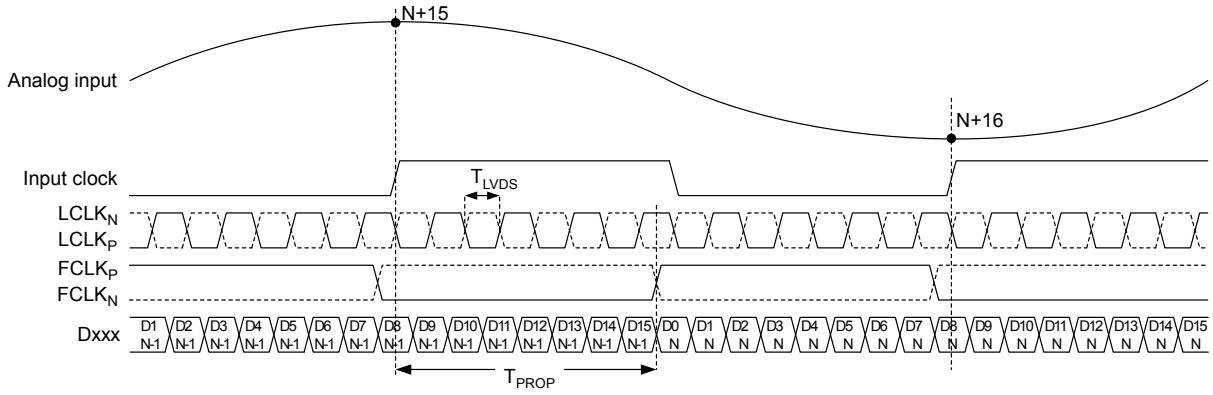


Figure 7: Precision - LVDS timing 16-bit output

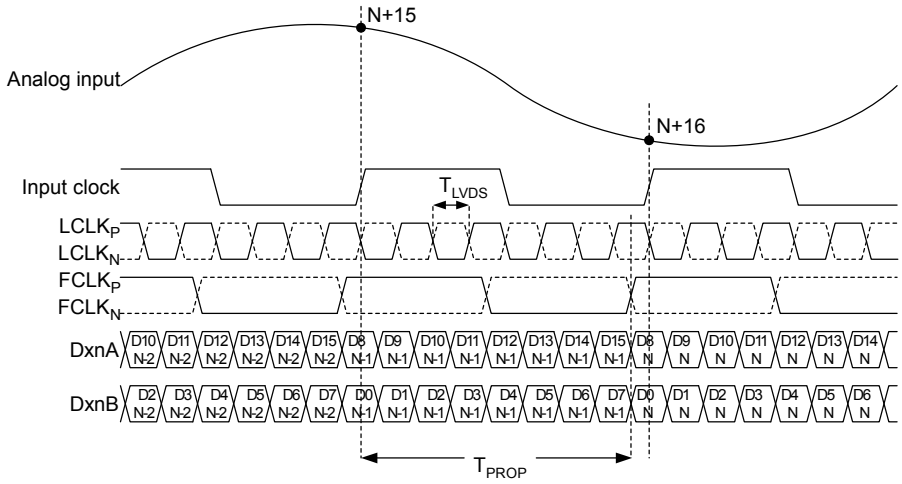


Figure 8: Precision - LVDS timing Dual 8-bit output

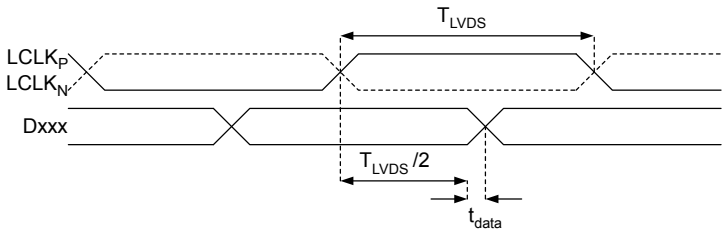


Figure 9: LVDS data timing

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Table 5: Register Map

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
rst *	Self-clearing software reset.	Inactive																X	0x00
sleep4_ch <4:1>	Channel-specific sleep mode for a Quad Channel setup.	Inactive													X	X	X	X	
sleep2_ch <2:1>	Channel-specific sleep mode for a Dual Channel setup.	Inactive											X	X					
sleep1_ch1	Channel-specific sleep mode for a Single Channel setup.	Inactive										X							0x0F
sleep	Go to sleep-mode.	Inactive								X									
pd	Go to power-down.	Inactive							X										
pd_pin_cfg <1:0>	Configures the PD pin function.	PD pin configured for power-down mode					X	X											
ilvds_lclk <2:0>	LVDS current drive programmability for LCLKP and LCLKN pins.	3.5 mA drive														X	X	X	
ilvds_frame <2:0>	LVDS current drive programmability for FCLKP and FCLKN pins.	3.5 mA drive										X	X	X					0x11
ilvds_dat <2:0>	LVDS current drive programmability for output data pins.	3.5 mA drive						X	X	X									
en_lvds_ term	Enables internal termination for LVDS buffers.	Termination disabled		X															
term_lclk <2:0>	Programmable termination for LCLKN and LCLKP buffers.	Termination disabled		1												X	X	X	
term_frame <2:0>	Programmable termination for FCLKN and FCLKP buffers.	Termination disabled		1								X	X	X					0x12
term_dat <2:0>	Programmable termination for output data buffers.	Termination disabled		1				X	X	X									
invert4_ch <4:1>	Channel specific swapping of the analog input signal for a Quad Channel setup.	IPx is positive input													X	X	X	X	
invert2_ch <2:1>	Channel specific swapping of the analog input signal for a Dual Channel setup.	IPx is positive input											X	X					0x24
invert1_ch1	Channel specific swapping of the analog input signal for a Single Channel setup.	IPx is positive input										X							
en_ramp	Enables a repeating full-scale ramp pattern on the outputs.	Inactive										X	0	0					
dual_ custom_pat	Enable the mode wherein the output toggles between two defined codes.	Inactive										0	X	0					0x25
single_ custom_pat	Enables the mode wherein the output is a constant specified code.	Inactive										0	0	X					
bits_custom1 <15:0>	Bits for the single custom pattern and for the first code of the dual custom pattern. <0> is the LSB.	0x0000	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0x26

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Table 5: Register Map

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
bits_custom2 <15:0>	Bits for the second code of the dual custom pattern.	0x0000	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0x27
cgain4_ch1 <3:0>	Programmable coarse gain channel 1 in a Quad Channel setup.	1x gain													X	X	X	X	0x2A
cgain4_ch2 <3:0>	Programmable coarse gain channel 2 in a Quad Channel setup.	1x gain									X	X	X	X					
cgain4_ch3 <3:0>	Programmable coarse gain channel 3 in a Quad Channel setup.	1x gain					X	X	X	X									
cgain4_ch4 <3:0>	Programmable coarse gain channel 4 in a Quad Channel setup.	1x gain	X	X	X	X													
cgain2_ch1 <3:0>	Programmable coarse gain channel 1 in a Dual Channel setup.	1x gain													X	X	X	X	0x2B
cgain2_ch2 <3:0>	Programmable coarse gain channel 2 in a Dual Channel setup.	1x gain									X	X	X	X					
cgain1_ch1 <3:0>	Programmable coarse gain channel 1 in a Single Channel setup.	1x gain					X	X	X	X									
jitter_ctrl <7:0>	Clock jitter adjustment.	160 fsrms									X	X	X	X	X	X	X	X	0x30
precision_ mode *	Enable Quad Channel 14 bits precision mode.	Inactive													X				0x31
high_speed_ mode * <2:0>	Enable high speed mode, Single, Dual or Quad channel.	High speed mode – Quad Channel														X	X	X	
clk_divide <1:0> *	Define clock divider factor: 1, 2, 4 or 8	Divide by 1							X	X									
coarse_ gain_cfg	Configures the coarse gain setting	x-gain enabled																X	0x33
fine_gain_en	Enable use of fine gain.	Disabled															X		
fgain_ branch1 <6:0>	Programmable fine gain for branch1.	1x / 0dB gain										X	X	X	X	X	X	X	0x34
fgain_ branch2 <6:0>	Programmable fine gain for branch 2.	1x / 0dB gain		X	X	X	X	X	X	X									
fgain_ branch3 <6:0>	Programmable fine gain for branch 3.	1x / 0dB gain										X	X	X	X	X	X	X	0x35
fgain_ branch4 <6:0>	Programmable fine gain for branch 4.	1x / 0dB gain		X	X	X	X	X	X	X									
fgain_ branch5 <6:0>	Programmable fine gain for branch 5.	1x / 0dB gain										X	X	X	X	X	X	X	0x36
fgain_ branch6 <6:0>	Programmable fine gain for branch 6.	1x / 0dB gain		X	X	X	X	X	X	X									
fgain_ branch7 <6:0>	Programmable fine gain for branch 7.	1x / 0dB gain										X	X	X	X	X	X	X	0x37
fgain_ branch8 <6:0>	Programmable fine gain for branch 8.	1x / 0dB gain		X	X	X	X	X	X	X									
inp_sel_adc1 <4:0>	Input select for adc 1.	Signal input: IP1/ IN1												X	X	X	X	X	0x3A
inp_sel_adc2 <4:0>	Input select for adc 2.	Signal input: IP2/ IN2				X	X	X	X	X									

Table 5: Register Map

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
inp_sel_adc3 <4:0>	Input select for adc 3.	Signal input: IP3/ IN3												X	X	X	X	X	0x3B
inp_sel_adc4 <4:0>	Input select for adc 4.	Signal input: IP4/ IN4				X	X	X	X	X									
phase_ddr <1:0>	Controls the phase of the LCLK output relative to data.	90 degrees										X	X						0x42
pat_deskew	Enable deskew pattern mode.	Inactive															0	X	0x45
pat_sync	Enable sync pattern mode.	Inactive															X	0	
btc_mode	Binary two's complement format for ADC output data.	Straight offset binary														X			0x46
msb_first	Serialized ADC output data comes out with MSB first.	LSB first													X				
adc_curr <2:0>	ADC current scaling.	Nominal														X	X	X	0x50
ext_vcm_bc <1:0>	VCM buffer driving strength control.	Nominal											X	X					
lvds_pd_ mode	Controls LVDS power down mode	High z-mode																X	0x52
lvds_output_ mode <2:0> *	Sets the number of LVDS output bits.	12 bit														X	X	X	0x53
low_clk_ freq *	Low clock frequency used.	Inactive													X				
lvds_ advance	Advance LVDS data bits and frame clock by one clock cycle	Inactive											0	X					
lvds_delay	Delay LVDS data bits and frame clock by one clock cycle	Inactive											X	0					
fs_cntrl <5:0>	Fine adjust ADC full scale range	0% change											X	X	X	X	X	X	0x55
startup_ctrl <2:0> *	Controls start-up time.	'000'														X	X	X	0x56

Undefined register addresses must not be written to; incorrect behavior may be the result.

Unused register bits (blank table cells) must be set to '0' when programming the registers.

All registers can be written to while the chip is in power down.

* These registers requires a power down cycle when written to (See Start up Initialization).

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Register Description

Software Reset

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
rst	Self-clearing software reset.	Inactive																X	0x00

Setting the rst register bit to '1', restores the default value of all the internal registers including the rst register bit itself.

Modes of Operation

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
precision_mode	Enable Quad Channel 14 bits precision mode.	Inactive													X				0x31
high_speed_ mode <2:0>	Enable high speed mode, Single, Dual or Quad channel.	High speed mode – Quad Channel														X	X	X	
clk_divide<1:0>	Define clock divider factor: 1, 2, 4 or 8	Divide by 1							X	X									

The HMCAD1520 has four main operating modes controlled by the register bits precision_mode and high_speed_ mode as defined in table 6. Power down mode, as described in section 'Startup Initialization', must be activated after or during a change of operating mode to ensure correct operation. The high speed modes all utilize interleaving to achieve high sampling speed. Quad channel mode interleaves 2 ADC branches, dual channel mode interleaves 4 ADC branches, while single channel mode interleave all 8 ADC branches. In precision mode interleaving is not required and each ADC channel uses one ADC branch only.

Table 6: Modes of Operation

precision_ mode	high_speed_mode <2:0>			Mode of operation	Description
0	0	0	1	Single channel 12-bit high speed mode	Single channel by interleaving ADC1to ADC4
0	0	1	0	Dual channel 12-bit high speed mode	Dual channel where channel 1 is made by interleaving ADC1 and ADC2, channel 2 by interleaving ADC3 and ADC4
0	1	0	0	Quad channel 12-bit high speed mode	Quad channel where channel 1 corresponds to ADC1, chan-nel2 to ADC2, channel3 to ADC3 and channel 4 to ADC4
1	0	0	0	Quad channel 14-bit precision mode	Quad channel where channel 1 corresponds to ADC1, chan-nel2 to ADC2, channel3 to ADC3 and channel 4 to ADC4

Only one of the 4 bits should be activated at the same time.

clk_divide<1:0> allows the user to apply an input clock frequency higher than the sampling rate. The clock divider will divide the input clock frequency by a factor of 1, 2, 4, or 8, defined by the *clk_divide<1:0>* register. By setting the *clk_divide<1:0>* value relative to the *channel_num<2:0>* value, the same input clock frequency can be used for all settings on number of channels. e.g: When increasing the number of channels from 1 to 4, the maximum sampling rate is reduced by a factor of 4. By letting *clk_divide<1:0>* follow the *channel_num<2:0>* value, and change it from 1 to 4, the internal clock divider will provide the reduction of the sampling rate without changing the input clock frequency.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Table 7: Clock Divider Factor

clk_divide<1:0>	Clock Divider Factor	Sampling rate (FS)
00 (default)	1	Input clock frequency / 1
01	2	Input clock frequency / 2
10	4	Input clock frequency / 4
11	8	Input clock frequency / 8

Input Select

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
inp_sel_adc1 <4:0>	Input select for adc 1.	Signal input: IP1/IN1												X	X	X	X	0	0x3A
inp_sel_adc2 <4:0>	Input select for adc 2.	Signal input: IP2/IN2				X	X	X	X	0									
inp_sel_adc3 <4:0>	Input select for adc 3.	Signal input: IP3/IN3												X	X	X	X	0	0x3B
inp_sel_adc4 <4:0>	Input select for adc 4.	Signal input: IP4/IN4				X	X	X	X	0									

Each ADC is connected to the four input signals via a full flexible cross point switch, set up by inp_sel_adcx. In single channel mode, any one of the four inputs can be selected as valid input to the single ADC channel. In dual channel mode, any two of the four inputs can be selected to each ADC channel. In quad channel mode and precision mode, any input can be assigned to any ADC channel. The switching of inputs can be done during normal operation, and no additional actions are needed. The switching will occur instantaneously at the end of each SPI command.

Table 8: ADC Input Select

inp_sel_adcx<4:0>	Selected input
0001 0	IP1/IN1
0010 0	IP2/IN2
0100 0	IP3/IN3
1000 0	IP4/IN4
other	Do not use

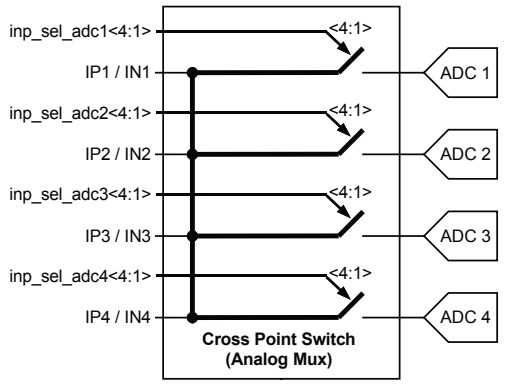


Figure 10: ADC input signals through Cross Point Switch

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Full-Scale Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
fs_cntrl <5:0>	Fine adjust ADC full scale range	0% change											X	X	X	X	X	X	0x55

The full-scale voltage range of HMCAD1520 can be adjusted using an internal 6-bit DAC controlled by the fs_cntrl register. Changing the value in the register by one step, adjusts the full-scale range by approximately 0.3%. This leads to a maximum range of ±10% adjustment. Table 9 shows how the register settings correspond to the full-scale range. Note that the values for full-scale range adjustment are approximate. The DAC is, however, guaranteed to be monotonous.

The full-scale control and the programmable gain features differ in two major ways:

1. The full-scale control function is an analog, whereas the programmable gain is a digital function.
2. The programmable gain function has much coarser gain steps and larger range compared to the full-scale control function.

Table 9: Register Values with Corresponding Change in Full-Scale Range

fs_cntrl<5:0>	Full-scale range adjustment
111111	9.7 %
111110	9.4 %
100001	0.3 %
100000	0%
011111	-0.3 %
000001	–9,7%
000000	–10,0%

Current Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
adc_curr <2:0>	ADC current scaling.	Nominal														X	X	X	0x50
ext_vcm_bc <1:0>	VCM buffer driving strength control	Nominal											X	X					

There are two registers that impact performance and power dissipation.

The *adc_curr* register scales the current consumption in the ADC core. The performance is guaranteed at the nominal setting. Lower power consumption can be achieved by reducing the adc_curr value, see table 10. The impact on performance will depend on the ADC sampling rate.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Table 10: ADC Current Control Settings

adc_curr<2:0>	ADC core current
100	-40%
101	-30%
110	-20%
111	-10%
000 (default)	Nominal
001	Do not use
010	Do not use
011	Do not use

The ext_vcm_bc register controls the driving strength in the buffer supplying the voltage on the VCM pin. If this pin is not in use, the buffer can be switched off. If current is drawn from the VCM pin, the driving strength can be increased to keep the voltage on this pin at the correct level.

Table 11: External Common Mode Voltage Buffer Driving Strength

ext_vcm_bc<1:0>	VCM buffer driving strength [µA] Max current sinked/sourced from VCM pin with < 20 mV voltage change.
00	Off (VCM floating)
01 (default)	±20
10	±400
11	±700

Start-up and Clock Jitter Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
startup_ctrl <2:0>	Controls start-up time	'000'														X	X	X	0x56
jitter_ctrl <7:0>	Clock jitter adjustment	160 fsrms									X	X	X	X	X	X	X	X	0x30

To optimize start up time, a register is provided where the start-up time in clock cycles can be set. Some internal circuitry have start up times that are clock frequency independent. Default counter values are set to accommodate these start up times at the maximum clock frequency (sampling rate). This will lead to increased start up times at low clock frequencies. Setting the value of this register to the nearest higher clock frequency will reduce the count values of the internal counters, to better fit the actual start up time, such that the start up time will be reduced. The start up times from power down and sleep modes are changed by this register setting. If the clock divider is used (set to other than 1), the input clock frequency must be divided by the divider factor to find the correct clock frequency range (see table 7).

Table 12: Start-Up Time Control Settings

Precision mode			
startup_ ctrl<2:0>	Clock frequency range [MSPS]	Startup delay [clock cycles]	Startup delay [µs]
100	80 - 125	1536	12.3 - 19.2
000	50 - 80	992	12.4 - 19.8
001	32,5 - 50	640	12.8 - 19.7
010	20 - 32,5	420	12.9 - 21
011	15 - 20	260	13 - 17.3
other	Do not use	-	-

Quad channel – High speed			
startup_ ctrl<2:0>	Clock frequency range [MSPS]	Startup delay [clock cycles]	Startup delay [µs]
100	160 - 250	3072	12.3 – 19.2
000	100 - 160	1984	12.4 - 19.8
001	65 - 100	1280	12.8 - 19.7
010	40 - 65	840	12.9 - 21
011	30 - 40	520	13 - 17.3
other	Do not use	-	-

Dual channel – High speed			
startup_ ctrl<2:0>	Clock frequency range [MSPS]	Startup delay [clock cycles]	Startup delay [µs]
100	320 - 500	6144	12.3 – 19.2
000	200 - 320	3968	12.4 - 19.8
001	130 – 200	2560	12.8 - 19.7
010	80 - 130	1680	12.9 - 21
011	60 – 80	1040	13 - 17.3
other	Do not use	-	-

Single channel – High speed			
startup_ ctrl<2:0>	Clock frequency range [MSPS]	Startup delay [clock cycles]	Startup delay [µs]
100	640 - 1000	12288	12.3 – 19.2
000	400 - 640	7936	12.4 - 19.8
001	260 - 400	5120	12.8 - 19.7
010	160 - 260	3360	12.9 - 21
011	120 - 160	2080	13 - 17.3
other	Do not use	-	-

jitter_ctrl<7:0> allows the user to set a trade-off between power consumption and clock jitter. If all bits in the register is set low, the clock signal is stopped. The clock jitter depends on the number of bits set to '1' in the *jitter_ctrl<7:0>* register. which bits are set high does not affect the result.

Table 13: Clock Jitter Performance

Number of bits to '1' in jitter_ctrl<7:0>	Clock jitter performance Precision mode [fsrms]	Clock jitter performance High speed modes [fsrms]	Module current consumption [mA]
1	130	160	1
2	100	150	2
3	92	136	3
4	85	130	4
5	82	126	5
6	80	124	6
7	77	122	7
8	75	120	8
0	Clock stopped	Clock stopped	

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

LVDS Output Configuration and Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
lvds_output_mode <2:0>	Sets the number of LVDS output bits.	12 bit														X	X	X	0x53
low_clk_freq	Low clock frequency used.	Inactive													X				
lvds_advance	Advance LVDS data bits and frame clock by one clock cycle	Inactive											0	X					
lvds_delay	Delay LVDS data bits and frame clock by one clock cycle	Inactive											X	0					
phase_ddr<1:0>	Controls the phase of the LCLK output relative to data.	90 degrees										X	X						0x42
btc_mode	Binary two's complement format for ADC output data.	Straight offset binary														X			0x46
msb_first	Serialized ADC output data comes out with MSB first.	LSB first													X				

The HMCAD1520 serial LVDS output has four different modes selected by the register lvds_output_mode as defined in table 14. Power down mode, as described in section 'Startup Initialization', must be activated after or during a change in the number of output bits to ensure correct behavior.

Table 14: Number of Bits in LVDS Output

lvds_output_mode <2:0>	Number of Bits	Comment
000	8 bit	8 bit mode, up to 1 GSPS (See HMCAD1511 datasheet)
001	12 bit	Recommended setting for High Speed Modes (Default)
101	14 bit	Recommended setting up to 70 MSPS (Precision mode)
011	16 bit	
100	Dual 8 bit	Recommended setting above 70 MSPS (Precision mode)
Other	Do not use	

12-bit LVDS mode is default for all operational modes. If another LVDS mode is to be used, the *lvds_output_mode* register setting must be changed accordingly.

When 8-bit LVDS mode is used, the LSBs are truncated and the data output will have 8-bit resolution. See HMCAD1511 and HMCAD1510 for detailed description.

When 14 or 16 bit LVDS output mode is selected the output data will be a 13 bit left justified word filled up with '0's on the LSB side. The different high speed modes uses the LVDS outputs as defined by table 15.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Table 15: High Speed Modes and Use of LVDS Outputs

High speed modes/ channels	LVDS outputs used
Single channel	D1A, D1B, D2A, D2B, D3A, D3B, D4A, D4B
Dual channel, channel 1	D1A, D1B, D2A, D2B
Dual channel, channel 2	D3A, D3B, D4A, D4B
Quad channel, channel 1	D1A, D1B
Quad channel, channel 2	D2A, D2B
Quad channel, channel 3	D3A, D3B
Quad channel, channel 4	D4A, D4B

For the 14-bit precision mode 14, 16 or dual 8-bit LVDS mode should be used. If the default 12-bit LVDS mode is used, the data output will be truncated to 12 bit. If the 16-bit LVDS mode is used the data output will be a 14-bit left justified word filled up with '00' on the LSB side. If the dual 8-bit output mode is used the 8 most significant bit of the 14 bit data word will be available on the LVDS 'A' output and the remaining 6 bit will be left justified and filled up with '00' on the LVDS 'B' output, see table 16.

Table 16: Precision Mode and Use of LVDS Outputs

Precision mode	LVDS outputs used
Channel 1 - 12, 14, 16-bit output	D1A (D1B will be in power down – high Z)
Channel 1 - Dual 8-bit output	D1A, D1B
Channel 2 - 12, 14, 16-bit output	D2A (D2B will be in power down – high Z)
Channel 2 - Dual 8-bit output	D2A, D2B
Channel 3 - 12, 14, 16-bit output	D3A (D3B will be in power down – high Z)
Channel 3 - Dual 8-bit output	D3A, D3B
Channel 4 - 12, 14, 16-bit output	D4A (D4B will be in power down – high Z)
Channel 4 - Dual 8-bit output	D4A, D4B

Maximum data output bit-rate for the HMCAD1520 is 1 Gb/s. The maximum sampling rate for the different configurations is given by table 17. The sampling rate is set by the frequency of the input clock (FS). The frame-rate, i.e. the frequency of the FCLK signal on the LVDS outputs, depends on the selected mode and the sampling frequency (FS) as defined in table 18.

Table 17: Maximum Sampling Rate vs Number of Output Bits for Different HMCAD1520 Configurations

Number of bits	Single Channel High Speed [MSPS]	Dual Channel High Speed [MSPS]	Quad Channel High Speed [MSPS]	Quad Channel Precision [MSPS]
8	1000	500	250	-
12	660	330	165	82.5
14	560	280	140	70
16	500	250	125	62.5
Dual 8	-	-	-	125

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

Table 18: Output Data Frame Rate

Mode of operation	Frame-rate (FCLK frequency)
High speed, single channel	F_S / 8
High speed, dual channel	F_S / 4
High speed, quad channel	F_S / 2
Precision mode	F_S

If the HMCAD1520 device is used at a low sampling rate the register bit low_clk_freq has to be set to '1'. See table 19 for when to use this register bit for the different modes of operation.

Table 19: Use of Register Bit low_clk_freq

Mode of operation	Limit when low_clk_freq should be activated
High speed, single channel	F_S < 240 MHz
High speed, dual channel	F_S < 120 MHz
High speed, quad channel	F_S < 60 MHz
Precision mode	F_S < 30 MHz

To ease timing in the receiver when using multiple HMCAD1520, the device has the option to adjust the timing of the output data and the frame clock. The propagation delay with respect to the ADC input clock can be moved one LVDS clock cycle forward or backward, by using *lvds_delay* and *lvds_advance*, respectively. See figure 11 for details. Note that LCLK is not affected by *lvds_delay* or *lvds_advance* settings.

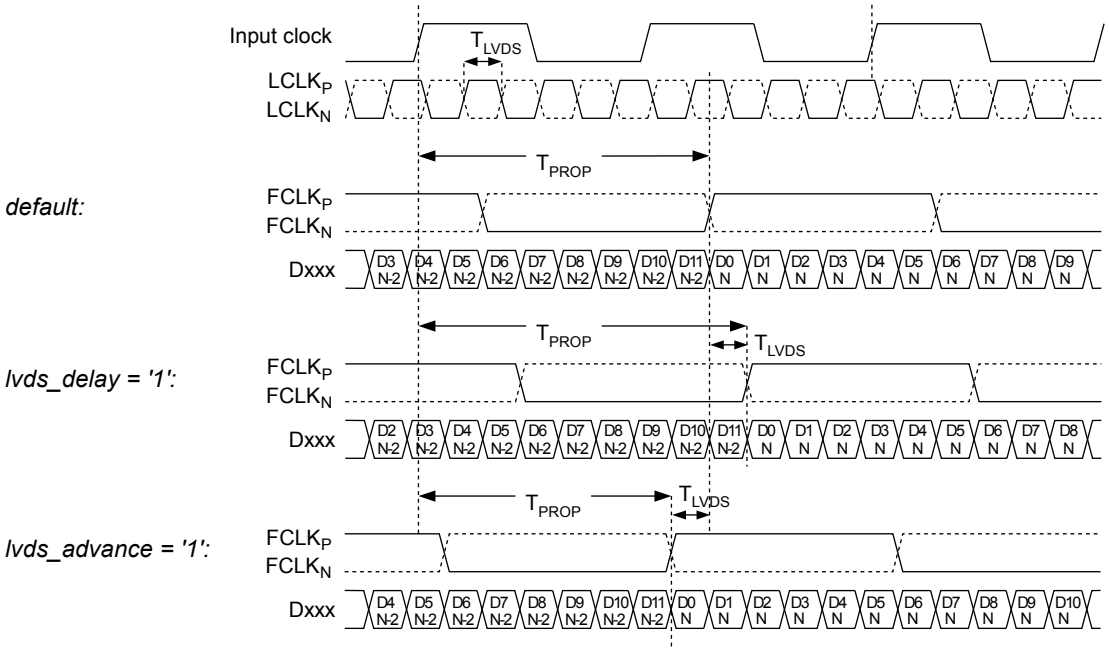


Figure 11: LVDS output timing adjustment

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D