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January 31, 2005

FN7376.2

6-Channel Clock Driver

The EL5001 is a 6-channel level shifting driver designed primarily for use as a clock driver in LTPS LCD displays. The EL5001 buffers and level shifts six logic level input signals. The six channels are grouped in to two sets, one of two channels and one of four channels. Each set can be configured in the inverting or non-inverting modes. Operating from 3.3V input logic, the output swing is set using two reference input pins. These pins can be up to 18V differential and are not buffered, so should therefore be bypassed effectively.

The EL5001 is designed to drive capacitive loads of 500pF with rise and fall times of just 20ns. A three-state pin is provided to set all outputs in to a high impedance mode. The ENABLE pin can be used to put the device in to a power save mode where the power consumption drops to just 3µA.

The EL5001 is available in 20-pin QFN (4mm x 4mm) and HTSSOP packages. Both are specified for operation over the -40°C to +85°C temperature range.

Features

- · SIx inverting/non-inverting channels
- · 3.3V input logic
- 18V output
- 250µA typical supply current
- Drives up to 500pF
- $T_R/T_F = 35$ ns max
- · Disable function
- 20-pin QFN (4mm x 4mm) and HTSSOP packages
- · Pb-free available (RoHS compliant)

Applications

- · LTPS LCD clock drivers
- · CCD driving
- · Level shifters

Ordering Information

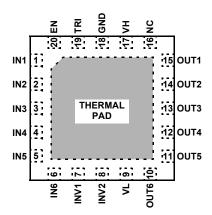
PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL5001IL	20-Pin QFN (4mm x 4mm)	-	MDP0046
EL5001IL-T7	20-Pin QFN (4mm x 4mm)	7"	MDP0046
EL5001IL-T13	20-Pin QFN (4mm x 4mm)	13"	MDP0046
EL5001ILZ (See Note)	20-Pin QFN (4mm x 4mm) (Pb-Free)	-	MDP0046
EL5001ILZ-T7 (See Note)	20-Pin QFN (4mm x 4mm) (Pb-Free)	7"	MDP0046
EL5001ILZ-T13 (See Note)	20-Pin QFN (4mm x 4mm) (Pb-Free)	13"	MDP0046

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL5001IRE	20-Pin HTSSOP	-	MDP0048
EL5001IRE-T7	20-Pin HTSSOP	7"	MDP0048
EL5001IRE-T13	20-Pin HTSSOP	13"	MDP0048
EL5001IREZ (See Note)	20-Pin HTSSOP (Pb-Free)	-	MDP0048
EL5001IREZ-T7 (See Note)	20-Pin HTSSOP (Pb-Free)	7"	MDP0048
EL5001IREZ-T13 (See Note)	20-Pin HTSSOP (Pb-Free)	13"	MDP0048

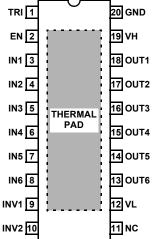
NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Pinouts

EL5001 [20-PIN QFN (4MM X 4MM)] TOP VIEW







Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Supply Voltage between V _{SD} and GND	Maximum Die Temperature
Maximum Continuous Output Current 50mA	Storage Temperature
Ambient Operating Temperature40°C to +85°C	Power Dissipation See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications V_H = 10V, V_L = -5V, EN = 3V, unless otherwise specified.

EN = 3V, IN _X = 3V 250 500 μA I _{S_DIS} Supply Current - Disabled EN = 0V, IN _X = 0V 3 μA V _{LR} V _L Range	PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
EN = 3V, IN _X = 3V 250 500 μA IS_DIS Supply Current - Disabled EN = 0V, IN _X = 0V 3 μA VLR VLR Range	POWER SUPPL	Y					
Is_DIS Supply Current - Disabled EN = 0V, INX = 0V 3 μA VLR VL Range -13 0 V VHR VH Range 5 18 V VH-VL Maximum VH - VL Range 0 18 V INPUT INPUT VIH Logic '1' Input Voltage 2.0 V IlH Logic '0' Input Current 0.1 10 μA VIL Logic '0' Input Voltage 0.8 V IlL Logic '0' Input Current 0.1 10 μA VIL Logic '0' Input Current 0.1 10 μA VIL Logic '0' Input Current 0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1 <td>I_S</td> <td>Supply Current</td> <td>EN = 3V, IN_X = 0V</td> <td></td> <td>750</td> <td>1200</td> <td>μA</td>	I _S	Supply Current	EN = 3V, IN _X = 0V		750	1200	μA
VLR VL Range -13 0 V VHR VH Range 5 18 V VH-VL Maximum VH - VL Range 0 18 V INPUT VIH Logic '1' Input Voltage 2.0 V V IlH Logic '1' Input Voltage 2.0 0.1 10 μA VIL Logic '0' Input Voltage 0.8 V IlL Logic '0' Input Current 0.1 10 μA CIN Input Capacitance 3.5 pF Rin Input Resistance 3.5 pF Rin Input Resistance 50 MΩ OUTPUT VOH VOUTL High INX = 10V, IL = 10mA 9.80 9.88 V VOL VOUTL Low INX = 0V, IL = 10mA 9.80 9.88 V VOL VOUTL Low INX = 0V, IL = 10mA 9.80 9.88 V ROH On Resistance VL to OUT IL = 50mA 11 15			EN = 3V, IN _X = 3V		250	500	μΑ
VHR VH Range 5 18 V VH-VL Maximum VH - VL Range 0 18 V INPUT VINPUT VIINPUT VIINPUT VIINPUT VIINPUT VIINPUT VIINPUT VIIINPUT Current 0.1 10 µA VIIINPUT Current 0.1 10 µA VIIINPUT Current 0.8 V VIIINPUT Current 0.1 10 µA VIINPUT CURRENT 0.0 <td>I_{S_DIS}</td> <td>Supply Current - Disabled</td> <td>EN = 0V, IN_X = 0V</td> <td></td> <td>3</td> <td></td> <td>μΑ</td>	I _{S_DIS}	Supply Current - Disabled	EN = 0V, IN _X = 0V		3		μΑ
V _H -V _L Maximum V _H - V _L Range 0 18 V INPUT Vi _H Logic '1' Input Voltage 2.0 V I _{IH} Logic '0' Input Current 0.1 10 μA V _{IL} Logic '0' Input Voltage 0.8 V I _{IL} Logic '0' Input Current 0.1 10 μA C _{IN} Input Capacitance 3.5 pF R _{IN} Input Resistance 50 MΩ OUTPUT VOH VOUTL High INX = 10V, I _L = 10mA 9.80 9.88 V VOL VOUT, Low INX = 0V, I _L = -10mA 9.80 9.8 V ROH On Resistance V _H to OUT I _L = 50mA 11 15 Ω ROL On Resistance V _L to OUT I _L = 50mA 11 15 Ω IPEAK Peak Output Current 500 mA I _L Out Leakage Current 500 mA SWITCHING CHARACTERISTICS 20 35 ns <td>V_{LR}</td> <td>V_L Range</td> <td></td> <td>-13</td> <td></td> <td>0</td> <td>V</td>	V _{LR}	V _L Range		-13		0	V
NPUT	V_{HR}	V _H Range		5		18	V
Vi	V _H -V _L	Maximum V _H - V _L Range		0		18	V
	INPUT						
VIL Logic '0' Input Voltage 0.8 V IIL Logic '0' Input Current 0.1 10 μA CIN Input Capacitance 3.5 pF RIN Input Resistance 50 MΩ OUTPUT VOH VOUTL High INx = 10V, IL = 10mA 9.80 9.88 V VOL VOUTL Low INx = 0V, IL = -10mA -4.90 -4.88 V ROH On Resistance V _H to OUT IL = 50mA 11 15 Ω ROL On Resistance V _L to OUT IL = 50mA 11 15 Ω IPEAK Peak Output Current 500 mA IL Out Leakage Current 0.1 0.5 μA SWITCHING CHARACTERISTICS Ite Fall Time CL = 500pF 20 35 ns Ite Fall Time CL = 500pF 5 ns Ite Turn On Delay CL = 500pF 55 ns Ite Turn Off Delay </td <td>V_{IH}</td> <td>Logic '1' Input Voltage</td> <td></td> <td>2.0</td> <td></td> <td></td> <td>V</td>	V _{IH}	Logic '1' Input Voltage		2.0			V
IIL Logic '0' Input Current 0.1 10 μA CIN Input Capacitance 3.5 pF RIN Input Resistance 50 MΩ OUTPUT VOH VOUTL High INX = 10V, IL = 10mA 9.80 9.88 V VOL VOUTL Low INX = 0V, IL = -10mA -4.90 -4.88 V ROH On Resistance V _H to OUT IL = 50mA 11 15 Ω ROL On Resistance V _L to OUT IL = 50mA 11 15 Ω IPEAK Peak Output Current 500 mA IL Out Leakage Current 0.1 0.5 μA SWITCHING CHARACTERISTICS I'R R ise Time CL = 500pF 20 35 ns ItF Fall Time CL = 500pF 5 ns ItPED TR, TF Matching CL = 500pF 55 ns ItPED Turn Off Delay CL = 500pF 55 ns ItPED	lін	Logic '1' Input Current			0.1	10	μΑ
CIN Input Capacitance 3.5 pF RIN Input Resistance 50 MΩ OUTPUT VOH VOUTL High INX = 10V, IL = 10mA 9.80 9.88 V VOL VOUTL Low INX = 0V, IL = -10mA -4.90 -4.88 V ROH On Resistance V _L to OUT IL = 50mA 11 15 Ω ROL On Resistance V _L to OUT IL = 50mA 11 15 Ω IPEAK Peak Output Current 500 mA IL Out Leakage Current 500 mA SWITCHING CHARACTERISTICS tR Rise Time CL = 500pF 20 35 ns tr- Fall Time CL = 500pF 20 35 ns tr- Fall Time CL = 500pF 55 ns tp- Turn On Delay CL = 500pF 55 ns tp- Turn Off Delay CL = 500pF 55 ns tp- Turn Off Delay CL =	V _{IL}	Logic '0' Input Voltage				0.8	V
RIN Input Resistance 50 MΩ OUTPUT VOH VOUTL High INX = 10V, IL = 10mA 9.80 9.88 V VOL VOUTL Low INX = 0V, IL = -10mA -4.90 -4.88 V ROH On Resistance VH to OUT IL = 50mA 11 15 Ω ROL On Resistance VL to OUT IL = 50mA 11 15 Ω IPEAK Peak Output Current 500 mA IL Out Leakage Current 500 mA SWITCHING CHARACTERISTICS TR Rise Time CL = 500pF 20 35 ns tF Fall Time CL = 500pF 20 35 ns tRFD TR. TF Matching CL = 500pF 5 ns tD+ Turn On Delay CL = 500pF 55 ns tD- Turn Off Delay CL = 500pF 55 ns tDD tD+, tD-, Matching CL = 500pF 5 ns tEN Enable T	I _{IL}	Logic '0' Input Current			0.1	10	μΑ
OUTPUT VOH VOUTL High INX = 10V, IL = 10mA 9.80 9.88 V VOL VOUTL LOW INX = 0V, IL = -10mA -4.90 -4.88 V ROH On Resistance VH to OUT IL = 50mA 11 15 Ω ROL On Resistance VL to OUT IL = 50mA 11 15 Ω IPEAK Peak Output Current 500 mA IL Out Leakage Current 0.1 0.5 µA SWITCHING CHARACTERISTICS 1 20 35 ns tR Rise Time CL = 500pF 20 35 ns tF Fall Time CL = 500pF 5 ns tRFD TR, TF Matching CL = 500pF 5 ns tD+ Turn Off Delay CL = 500pF 55 ns tD- Turn Off Delay CL = 500pF 55 ns tDD tD+, tD-, Matching CL = 500pF 5 ns tEN Enable Time	C _{IN}	Input Capacitance			3.5		pF
VOH VOUTL High INχ = 10V, IL = 10mA 9.80 9.88 V VOL VOUTL Low INχ = 0V, IL = -10mA -4.90 -4.88 V ROH On Resistance V _L to OUT IL = 50mA 11 15 Ω ROL On Resistance V _L to OUT IL = 50mA 11 15 Ω IPEAK Peak Output Current 500 mA IL Out Leakage Current 0.1 0.5 μA SWITCHING CHARACTERISTICS tR Rise Time CL = 500pF 20 35 ns tF Fall Time CL = 500pF 20 35 ns tRFD TR, TF Matching CL = 500pF 5 ns tD+ Turn On Delay CL = 500pF 55 ns tD- Turn Off Delay CL = 500pF 55 ns tDD tD+, tD-, Matching CL = 500pF 5 ns tEN Enable Time CL = 500pF 5 ns	R _{IN}	Input Resistance			50		MΩ
VOL VOLTL Low IN _X = 0V, I _L = -10mA -4.90 -4.88 V ROH On Resistance V _L to OUT I _L = 50mA 11 15 Ω ROL On Resistance V _L to OUT I _L = 50mA 11 15 Ω I _{PEAK} Peak Output Current 500 mA I _L Out Leakage Current 0.1 0.5 μA SWITCHING CHARACTERISTICS t _R Rise Time C _L = 500pF 20 35 ns t _F Fall Time C _L = 500pF 20 35 ns t _{RFD} T _R , T _F Matching C _L = 500pF 5 ns t _D + Turn On Delay C _L = 500pF 55 ns t _D - Turn Off Delay C _L = 500pF 55 ns t _D - T _D -, Matching C _L = 500pF 5 ns t _D - Enable Time C _L = 500pF 9.8 μs	OUTPUT						
ROH On Resistance V _H to OUT I _L = 50mA 11 15 Ω ROL On Resistance V _L to OUT I _L = 50mA 11 15 Ω I _{PEAK} Peak Output Current 500 mA I _L Out Leakage Current 0.1 0.5 μ A SWITCHING CHARACTERISTICS t _R Rise Time C _L = 500pF 20 35 ns t _F Fall Time C _L = 500pF 20 35 ns t _{RFD} T _R , T _F Matching C _L = 500pF 5 ns t _D + Turn On Delay C _L = 500pF 55 ns t _D - Turn Off Delay C _L = 500pF 55 ns t _D - Turn Off Delay C _L = 500pF 55 ns t _D - T _D -, Matching C _L = 500pF 5 ns t _{EN} Enable Time 9.8 μ s	V _{OH}	V _{OUTL} High	IN _X = 10V, I _L = 10mA	9.80	9.88		V
ROL On Resistance V _L to OUT I _L = 50mA 11 15 Ω I _{PEAK} Peak Output Current 500 mA I _L Out Leakage Current 0.1 0.5 μA SWITCHING CHARACTERISTICS t _R Rise Time $C_L = 500pF$ 20 35 ns t _F Fall Time $C_L = 500pF$ 20 35 ns t _{RFD} T _R , T _F Matching $C_L = 500pF$ 5 ns t _D + Turn On Delay $C_L = 500pF$ 55 ns t _D - Turn Off Delay $C_L = 500pF$ 55 ns t _D - t _D +, t _D -, Matching $C_L = 500pF$ 5 ns t _{EN} Enable Time 9.8 μs	V _{OL}	V _{OUTL} Low	$IN_X = 0V$, $I_L = -10mA$		-4.90	-4.88	V
IPEAK Peak Output Current 500 mA IL Out Leakage Current 0.1 0.5 μA SWITCHING CHARACTERISTICS t_R Rise Time $C_L = 500pF$ 20 35 ns t_F Fall Time $C_L = 500pF$ 20 35 ns t_{RFD} T_R , T_F Matching $C_L = 500pF$ 5 ns t_D + Turn On Delay $C_L = 500pF$ 55 ns t_D - Turn Off Delay $C_L = 500pF$ 55 ns t_D - t_D +, t_D -, Matching $C_L = 500pF$ 5 ns t_{EN} Enable Time 9.8 μ s	R _{OH}	On Resistance V _H to OUT	I _L = 50mA		11	15	Ω
IL Out Leakage Current 0.1 0.5 μA SWITCHING CHARACTERISTICS t_R Rise Time $C_L = 500pF$ 20 35 ns t_F Fall Time $C_L = 500pF$ 20 35 ns t_{RFD} T_{R} , T_{F} Matching $C_L = 500pF$ 5 ns t_D + Turn On Delay $C_L = 500pF$ 55 ns t_{DD} t_{D^+} , t_{D^-} , Matching $C_L = 500pF$ 55 ns t_{DN} Enable Time $C_L = 500pF$ 9.8 μ_S	R _{OL}	On Resistance V _L to OUT	I _L = 50mA		11	15	Ω
SWITCHING CHARACTERISTICS t_R Rise Time $C_L = 500pF$ 20 35 ns t_F Fall Time $C_L = 500pF$ 20 35 ns t_{RFD} T_R , T_F Matching $C_L = 500pF$ 5 ns t_D + Turn On Delay $C_L = 500pF$ 55 ns t_D - Turn Off Delay $C_L = 500pF$ 55 ns t_D - t_D +, t_D -, Matching $C_L = 500pF$ 5 ns t_{EN} Enable Time 9.8 μ s	I _{PEAK}	Peak Output Current			500		mA
t_R Rise Time $C_L = 500pF$ 20 35 ns t_F Fall Time $C_L = 500pF$ 20 35 ns t_{RFD} T_R , T_F Matching $C_L = 500pF$ 5 ns t_D + Turn On Delay $C_L = 500pF$ 55 ns t_D - Turn Off Delay $C_L = 500pF$ 55 ns t_D - t_D +, t_D -, Matching $C_L = 500pF$ 5 ns t_{EN} Enable Time 9.8 μ_S	IL	Out Leakage Current			0.1	0.5	μΑ
t_F Fall Time C_L = 500pF 20 35 ns t_{RFD} T_R , T_F Matching C_L = 500pF 5 ns t_D + Turn On Delay C_L = 500pF 55 ns t_D - Turn Off Delay C_L = 500pF 55 ns t_D D t_D +, t_D -, Matching C_L = 500pF 5 ns t_{EN} Enable Time 9.8 μ_S	SWITCHING CH	IARACTERISTICS					
t_{RFD} T_{R} , T_{F} Matching C_{L} = 500pF 5 ns t_{D} Turn On Delay C_{L} = 500pF 55 ns t_{D} Turn Off Delay C_{L} = 500pF 55 ns t_{DD} t_{D} +, t_{D} -, Matching C_{L} = 500pF 5 ns t_{EN} Enable Time 9.8 μ_{S}	t _R	Rise Time	C _L = 500pF		20	35	ns
t_D^+ Turn On Delay $C_L = 500pF$ 55 ns t_D^- Turn Off Delay $C_L = 500pF$ 55 ns t_{DD} t_D^+ , t_{D^-} , Matching $C_L = 500pF$ 5 ns t_{EN} Enable Time 9.8 μs	t _F	Fall Time	C _L = 500pF		20	35	ns
t_{D^-} Turn Off Delay C_L = 500pF 55 ns t_{DD} t_{D^+} , t_{D^-} , Matching C_L = 500pF 5 ns t_{EN} Enable Time 9.8 μs	t _{RFD}	T _R , T _F Matching	C _L = 500pF		5		ns
t_{DD} $t_{D}+$, $t_{D}-$, Matching $C_{L}=500 pF$ 5 ns t_{EN} Enable Time 9.8 μs	t _D +	Turn On Delay	C _L = 500pF		55		ns
t _{EN} Enable Time 9.8 μs	t _D -	Turn Off Delay	C _L = 500pF		55		ns
Liv I	t _{DD}	t _D +, t _D -, Matching	C _L = 500pF		5		ns
t _{DIS} Disable Time 2.2 μs	t _{EN}	Enable Time		9.8			μs
	t _{DIS}	Disable Time		2.2			μs

intersil FN7376.2 January 31, 2005

Typical Performance Curves

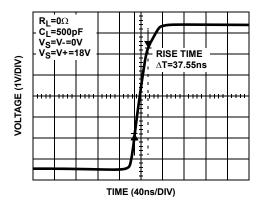


FIGURE 1. RISE TIME OUTPUT $6V_{P-P}$

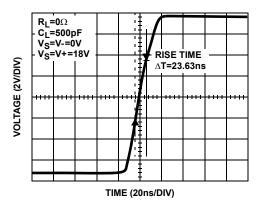


FIGURE 3. RISE TIME OUTPUT 12VP-P

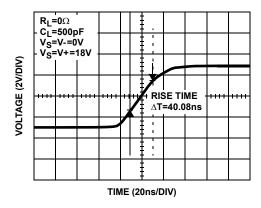


FIGURE 5. RISE TIME OUTPUT 5VP-P

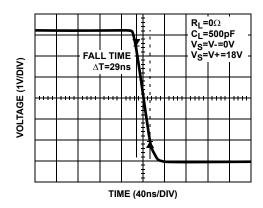


FIGURE 2. FALL TIME OUTPUT 6VP-P

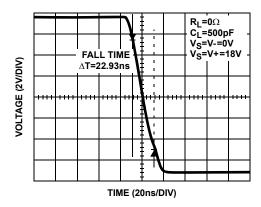


FIGURE 4. FALL TIME OUTPUT 12VP-P

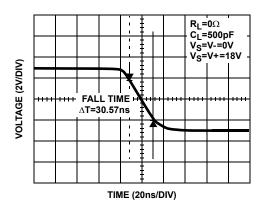


FIGURE 6. FALL TIME OUTPUT 5VP-P

Typical Performance Curves (Continued)

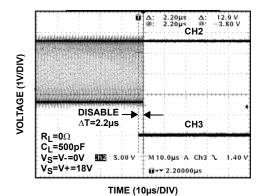


FIGURE 7. DISABLE RESPONSE

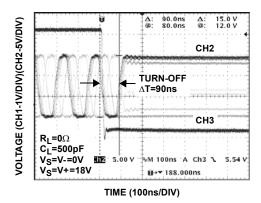


FIGURE 9. TURN-OFF (TRI)

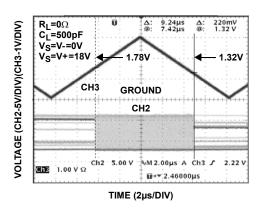


FIGURE 11. ENABLE/DISABLE THRESHOLD

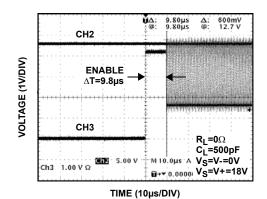


FIGURE 8. ENABLE RESPONSE

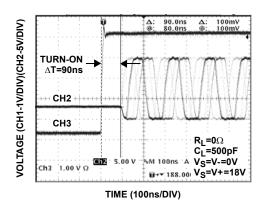


FIGURE 10. TURN-ON (TRI)

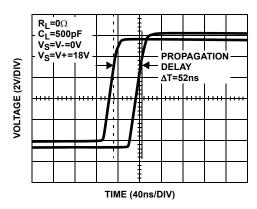


FIGURE 12. PROPAGATION DELAY

Typical Performance Curves (Continued)

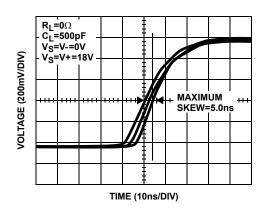


FIGURE 13. SKEW

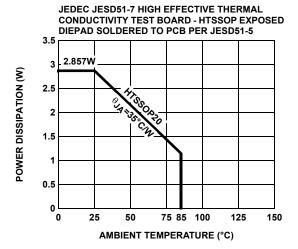


FIGURE 15. PACKAGE POWER DISSIPATION VS AMBIENT TEMPERATURE

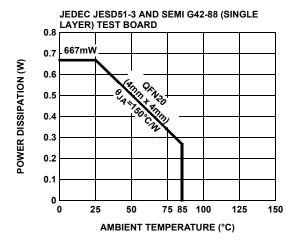


FIGURE 17. PACKAGE POWER DISSIPATION VS AMBIENT TEMPERATURE

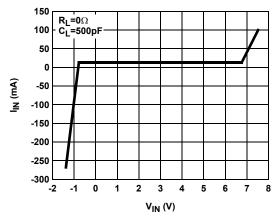


FIGURE 14. INPUT CURRENT vs VOLTAGE

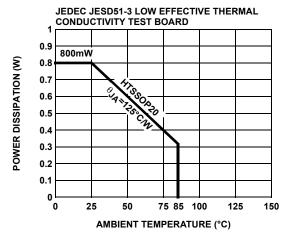


FIGURE 16. PACKAGE POWER DISSIPATION VS AMBIENT TEMPERATURE

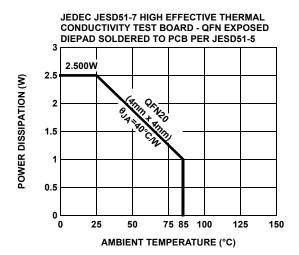
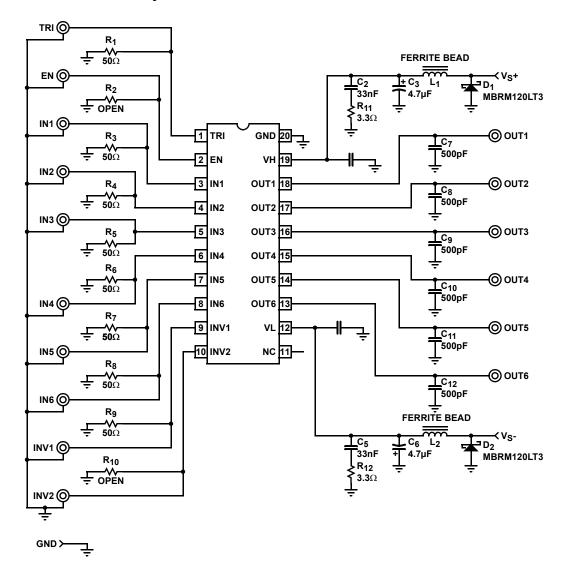


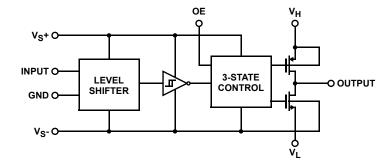
FIGURE 18. PACKAGE POWER DISSIPATION VS AMBIENT TEMPERATURE

6

EL5001 Test Board Circuit Layout



Block Diagram



Applications Information

The EL5001, a six channel high performance buffer, is directed primarily as a clock driver to LPTS LCD display applications. The six input channels are grouped into one group of four inputs and one group of two inputs each with a single pin (INV1 or INV2) to toggle the polarity from inverting to non-inverting. Each channel consists of a single N-channel low side driver and single P-channel high side driver. These 11 Ω devices pull the output to either the high or low voltage on $V_{\mbox{\scriptsize H}}$ and $V_{\mbox{\scriptsize L}}$ respectively, depending on the logic input signal.

A common 3-state pin is available that when activated will pull all 6-channel outputs to the high impedance state. Enable and disable pins turn shutdown both inputs and outputs. Timing plots for 3-state, enable, and disable functions are included in the characterization documentation.

The EL5001 is available in either a 20-pin HTSSOP or QFN (4mm x 4mm) packages to provide a choice for power dissipation considerations.

Supply Voltage and Input Compatibility

The EL5001 is designed to operate at a maximum potential range from 0V to 18V. Because the EL5001 does not contain a true analog switch, the positive supply must always be 4V higher than the negative supply.

All input pins are compatible with both 3V and 5V CMOS signals. With the positive supply set to V_S = 5V the EL5001 is compatible with TTL inputs.

Power Supply Bypassing

Due to the high switching currents generated by the EL5001 power supply bypassing is very important on both the positive and negative supplies. A 4.7 μF tantalum capacitor can be used in parallel with a 0.1 μF low-inductance ceramic MLC capacitor. As with all bypass components, these should be placed as close as possible to the supply pins. We also recommend the V_L and V_H pins have some level of bypassing especially when the device is driving highly capacitive loads.

Power Dissipation Calculation

When switching at high speeds, or driving heavy loads, the EL5001 drive capability is limited by the rise in die temperature brought about by internal power dissipation. For reliable operation die temperature must be kept below $T_{\mbox{\scriptsize JMAX}}$ (125°C). It is necessary to calculate the power dissipation for a given application prior to selecting package type.

Power dissipation may be calculated:

$$PD = (V_S \times I_S) + \sum_{f} (C_{INT} \times V_S^2 \times f) + (C_L \times V_{OUT}^2 \times f)$$

where:

 V_S = Total power supply to the EL5001 (from V_S + to V_S -)

 V_{OUT} = Swing on the output ($V_H - V_I$)

C_L = Load capacitance

C_{INT} = Internal load capacitance (80pF max)

I_S = Quiescent supply current (3mA max)

f = Frequency

Having obtained the application's power dissipation, the maximum junction temperature can be calculated:

$$T_{JMAX} = T_{MAX} + \Theta_{JA} \times PD$$

where:

T_{JMAX} = Maximum junction temperature (125°C)

T_{MAX} = Maximum ambient operating temperature

PD = Power dissipation calculated above

 θ_{JA} = Thermal resistance, junction to ambient, of the application (package + PCB combination)

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