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Data Sheet May 13, 2005 FN7430.1

Multi-Channel Buffers

The EL5129 and EL5329 integrate multiple gamma buffers and a single V_{COM} buffer for use in large panel LCD displays of 10” and greater. The EL5129 integrates 6 gamma channels and the EL5329 integrates 10 gamma channels. Half of the gamma channels in each device are designed to swing to the upper supply rail, with the other half designed to swing to the lower rail. The output capability of each channel is 10mA continuous, with 120mA peak. The gamma buffers feature a 10MHz 3dB bandwidth specification and a 9V/µs slew rate.

The V_{COM} amplifier is designed to swing from rail to rail. The output current capability of the V_{COM} in the EL5129 and EL5329 is 30mA continuous, 150mA peak and a slew rate of 10V/µs.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG DWG. #
EL5129IRE	20-Pin HTSSOP	-	MDP0048
EL5129IRE-T7	20-Pin HTSSOP	7”	MDP0048
EL5129IRE-T13	20-Pin HTSSOP	13”	MDP0048
EL5129IREZ (See Note)	20-Pin HTSSOP (Pb-free)	-	MDP0048
EL5129IREZ-T7 (See Note)	20-Pin HTSSOP (Pb-free)	7”	MDP0048
EL5129IREZ-T13 (See Note)	20-Pin HTSSOP (Pb-free)	13”	MDP0048
EL5129IRZ (See Note)	20-Pin TSSOP (Pb-free)	-	MDP0044
EL5129IRZ-T7 (See Note)	20-Pin TSSOP (Pb-free)	7”	MDP0044
EL5129IRZ-T13 (See Note)	20-Pin TSSOP (Pb-free)	13”	MDP0044
EL5329IREZ (See Note)	28-Pin HTSSOP (Pb-free)	-	MDP0048
EL5329IREZ-T7 (See Note)	28-Pin HTSSOP (Pb-free)	7”	MDP0048
EL5329IREZ-T13 (See Note)	28-Pin HTSSOP (Pb-free)	13”	MDP0048
EL5329IRZ (See Note)	28-Pin TSSOP (Pb-free)	-	MDP0044
EL5329IRZ-T7 (See Note)	28-Pin TSSOP (Pb-free)	7”	MDP0044
EL5329IRZ-T13 (See Note)	28-Pin TSSOP (Pb-free)	13”	MDP0044

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

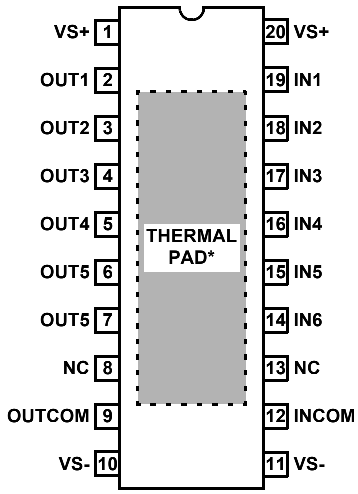
- Multiple gamma buffers
  - 6 channels (EL5129)
  - 10 channels (EL5329)
- Single V_{COM} amplifier
- Low supply current
  - 3.5mA (EL5129)
  - 5.5mA (EL5329)
- For higher speed or higher output power, see the EL5x24 family
- Pb-free available (RoHS compliant)

Applications

- TFT-LCD monitors
- LCD televisions
- Industrial flat panel displays

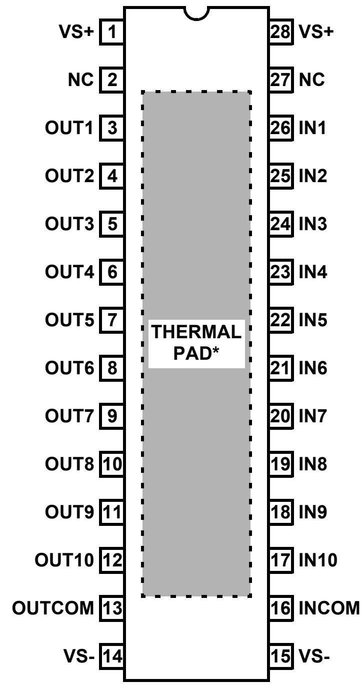
Pinouts

EL5129
(20-PIN TSSOP, HTSSOP)
TOP VIEW



* THERMAL PAD CONNECTED TO PIN 10 OR 11 (V_S-)

EL5329
(28-PIN TSSOP, HTSSOP)
TOP VIEW



* THERMAL PAD CONNECTED TO PIN 14 OR 15 (V_S-)

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S+ and V_S- . . . .+18V
Input Voltage . . . . V_S- -0.5V, V_S+ +0.5V
Maximum Continuous Output Current (V_{OUT0-9}) 15mA
Maximum Continuous Output Current (V_{OUTA}). 100mA

Power Dissipation . . . . See Curves
Maximum Die Temperature . . . . +125°C
Storage Temperature . . . . -65°C to +150°C
Ambient Operating Temperature . . . . -40°C to +85°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +15V, V_S- = 0, R_L = 10kΩ, C_L = 10pF to 0V, T_A = 25°C unless otherwise specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		2	20	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			10		MΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	1V ≤ V_{OUT} ≤ 14V	0.992		1.008	V/V
CMIR	Input Voltage Range	EL5129, IN1 to IN3	1.5		V_S+	V
		EL5329, IN1 to IN5	1.5		V_S+	V
		EL5129, IN4 to IN6	0		V_S+ -1.5	V
		EL5329, IN6 to IN10	0		V_S+ -1.5	V
INPUT CHARACTERISTICS (V_{COM} BUFFER)						
V_{OS}	Input Offset Voltage	V_{CM} = 7.5V		1	20	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		3		µV/°C
I_B	Input Bias Current	V_{CM} = 7.5V		2	50	nA
R_{IN}	Input Impedance			10		MΩ
C_{IN}	Input Capacitance			1.35		pF
V_{REG}	Load Regulation	V_{COM} = 7.5V, -60mA < I_L < 60mA	-20		+20	mV
$CMIR_{COM}$	Input Voltage Range V_{COM}		0		V_S+	V
OUTPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V_{OH}	High Output Voltage - EL5129 & EL5329 (Output 1)	V_{IN} = 15V, I_O = 5mA	14.85	14.9		V
	High Output Voltage - EL5129 (Output 2, 3), EL5329 (Output 2-5)		14.8	14.85		V
	High Output Voltage - EL5129 (Output 4-6), EL5329 (Output 6-10)	V_{IN} = 13.5V, I_O = 5mA	13.45	13.5		V
V_{OL}	Low Output Voltage - EL5129 (Output 1-3), EL5329 (Output 1-5)	V_{IN} = 1.5V, I_O = 5mA		1.5	1.55	V
	Low Output Voltage - EL5129 (Output 4-5), EL5329 (Output 6-9)	V_{IN} = 0V, I_O = 5mA		150	200	mV
	Low Output Voltage - EL5129 (Output 6), EL5329 (Output 10)			100	150	mV
I_{SC}	Short Circuit Current		100	120		mA

Electrical Specifications $V_S+ = +15V$, $V_S- = 0$, $R_L = 10k\Omega$, $C_L = 10pF$ to 0V, $T_A = 25°C$ unless otherwise specified **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS (V_{COM} BUFFER)						
V_{OH}	High Level Saturated Output Voltage	$V_S+ = 15V$, $I_O = -5mA$, $V_I = 15V$	14.85	14.9		V
V_{OL}	Low Level Saturated Output Voltage	$V_S+ = 15V$, $I_O = -5mA$, $V_I = 0V$		0.1	0.15	V
I_{SC}	Short Circuit Current		150	170		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	Reference buffer V_S from 5V to 15V	50	80		dB
		V_{COM} buffer, V_S from 5V to 15V	55	80		dB
I_S	Total Supply Current	EL5129		3.5	4.5	mA
		EL5329		5.5	7	mA
DYNAMIC PERFORMANCE (BUFFER AMPLIFIERS)						
SR	Slew Rate (Note 2)		5	9		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 10pF$		10		MHz
CS	Channel Separation	f = 5MHz		75		dB
EL5129 & EL5329 DYNAMIC PERFORMANCE (V_{COM} AMPLIFIERS)						
SR	Slew Rate (Note 2)	$-4V \le V_{OUT} \le 4V$, 20% to 80%	7	10		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		350		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 10pF$		15		MHz
CS	Channel Separation	f = 5MHz		75		dB

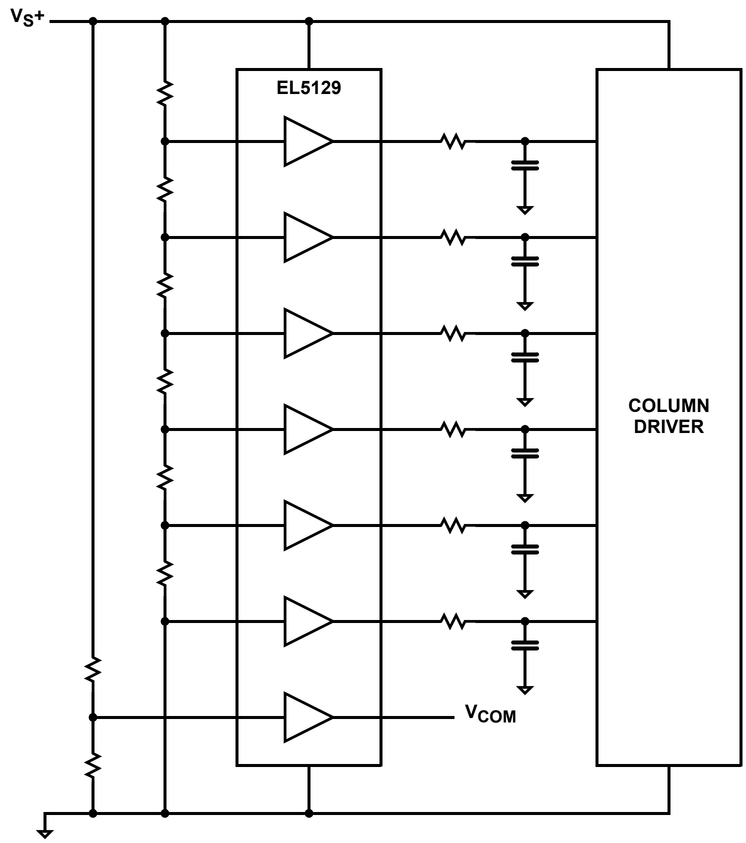
NOTES:

1. Measured over operating temperature range
2. Slew rate is measured on rising and falling edges

Pin Descriptions

EL5129	EL5329	PIN NAME	PIN FUNCTION
1, 20	1, 28	VS+	Positive supply voltage
2	3	OUT1	Output gamma channel 1
3	4	OUT2	Output gamma channel 2
4	5	OUT3	Output gamma channel 3
5	6	OUT4	Output gamma channel 4
6	7	OUT5	Output gamma channel 5
7	8	OUT6	Output gamma channel 6
8, 13	2, 27	NC	No connect
9	13	OUTCOM	Output, V_{COM}
10, 11	14, 15	VS-	Negative supply
12	16	INCOM	Input, V_{COM}
14	21	IN6	Input gamma channel 6
15	22	IN5	Input gamma channel 5
16	23	IN4	Input gamma channel 4
17	24	IN3	Input gamma channel 3
18	25	IN2	Input gamma channel 2
19	26	IN1	Input gamma channel 1
	9	OUT7	Output gamma channel 7
	10	OUT8	Output gamma channel 8
	11	OUT9	Output gamma channel 9
	12	OUT10	Output gamma channel 10
	17	IN10	Input gamma channel 10
	18	IN9	Input gamma channel 9
	19	IN8	Input gamma channel 8
	20	IN7	Input gamma channel 7

Block Diagram



Typical Performance Curves

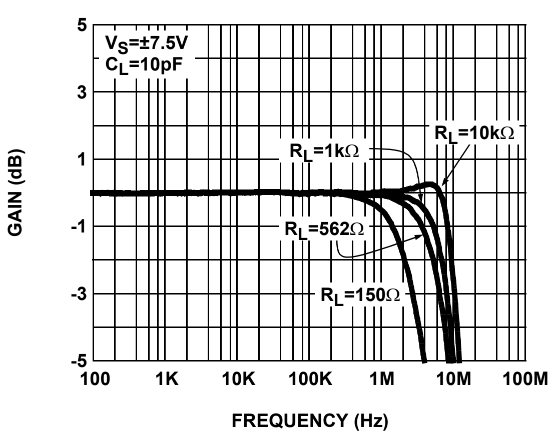


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS R_{LOAD} (BUFFER)

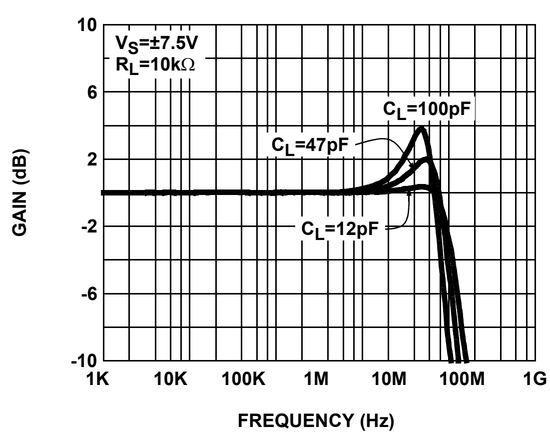


FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS C_{LOAD} (BUFFER)

Typical Performance Curves (Continued)

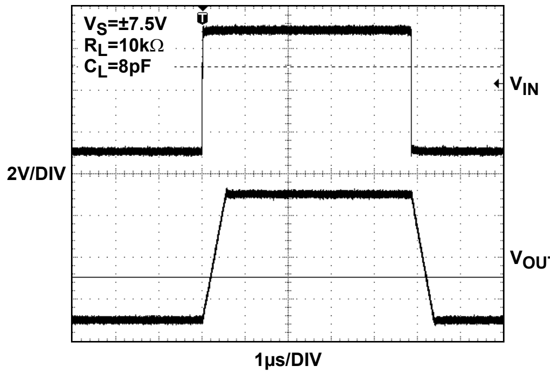


FIGURE 3. LARGE SIGNAL TRANSIENT RESPONSE (BUFFER)

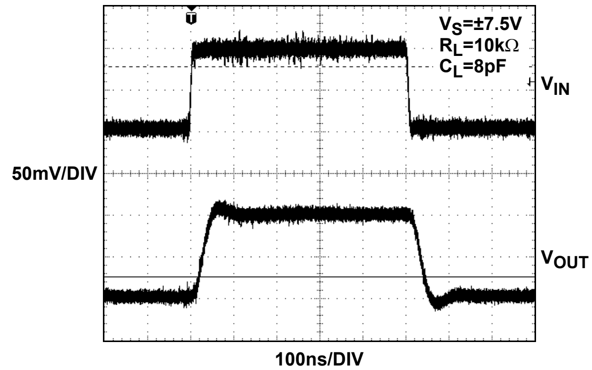


FIGURE 4. SMALL SIGNAL TRANSIENT RESPONSE (BUFFER)

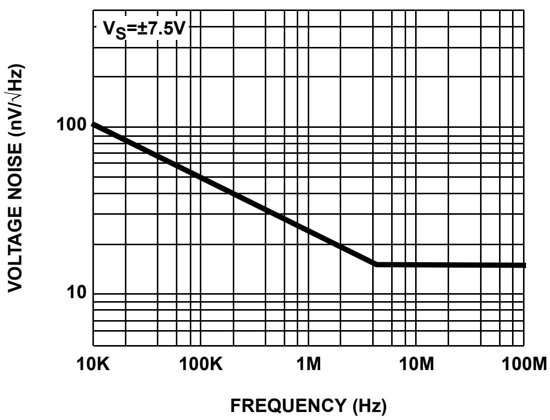


FIGURE 5. INPUT NOISE SPECIAL DENSITY vs FREQUENCY (BUFFER)

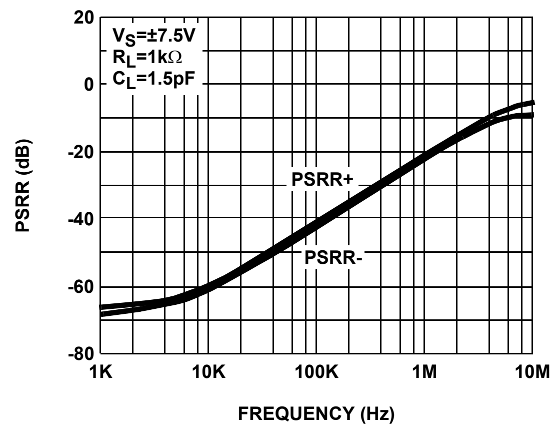


FIGURE 6. PSRR vs FREQUENCY (BUFFER)

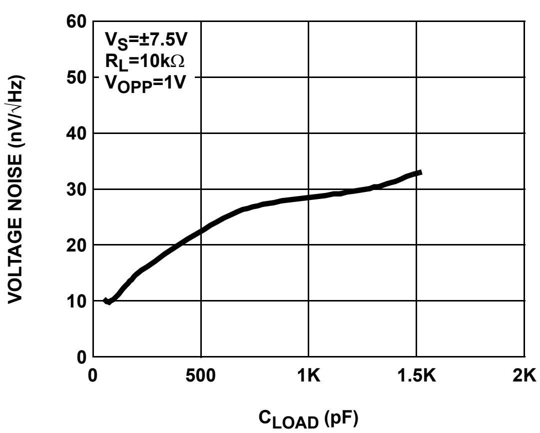


FIGURE 7. OVERSHOOT vs CAPACITANCE LOAD (BUFFER)

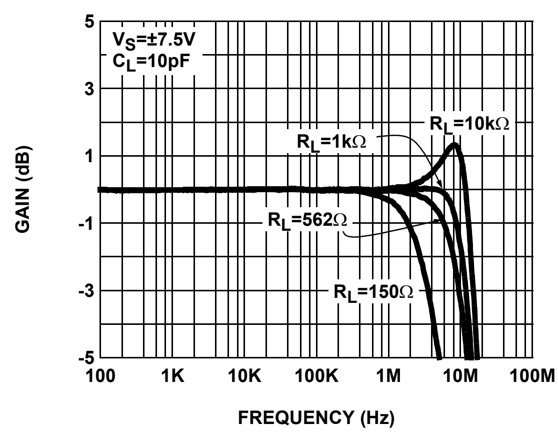


FIGURE 8. FREQUENCY RESPONSE FOR VARIOUS R_{LOAD} (V_{COM})

Typical Performance Curves (Continued)

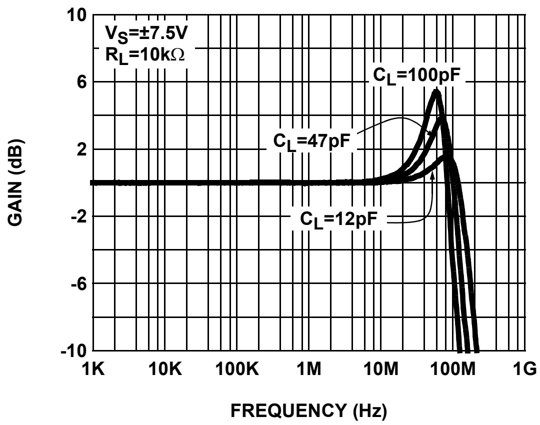


FIGURE 9. FREQUENCY RESPONSE FOR VARIOUS C_{LOAD} (V_{COM})

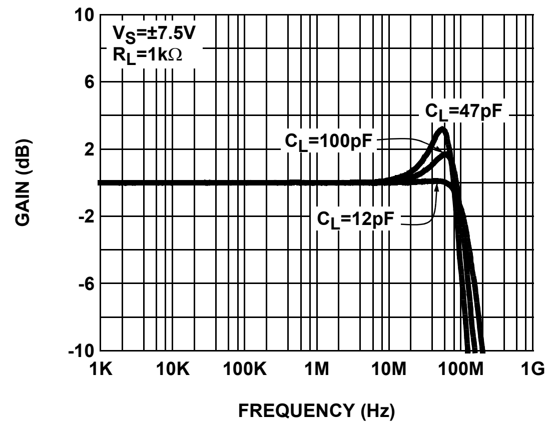


FIGURE 10. FREQUENCY RESPONSE FOR VARIOUS C_{LOAD} (V_{COM})

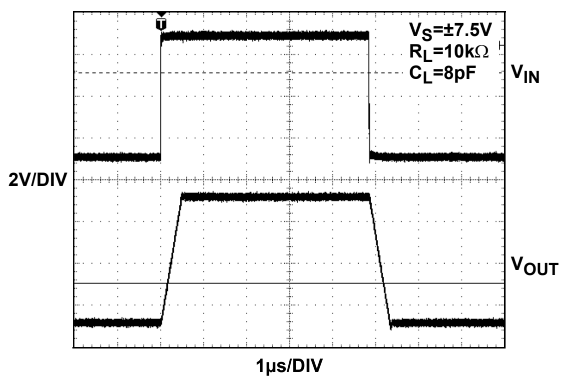


FIGURE 11. LARGE SIGNAL TRANSIENT RESPONSE (V_{COM})

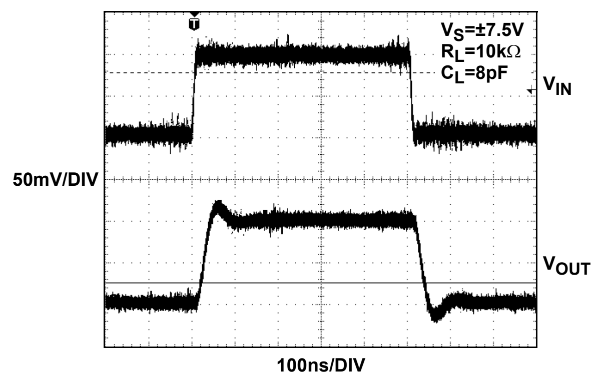


FIGURE 12. SMALL SIGNAL TRANSIENT RESPONSE (V_{COM})

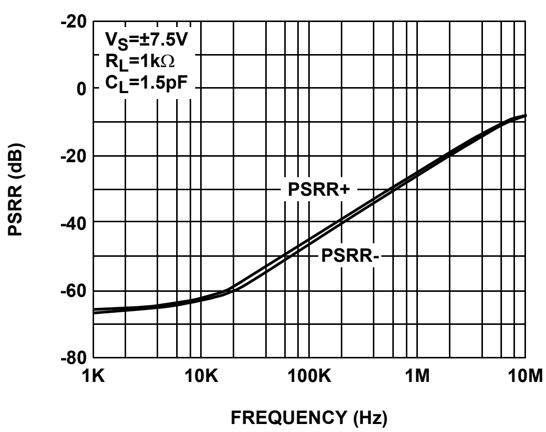


FIGURE 13. PSRR vs FREQUENCY (V_{COM})

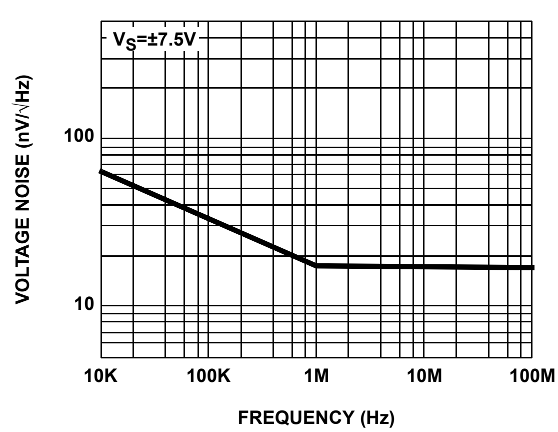


FIGURE 14. INPUT NOISE SPECIAL DENSITY vs FREQUENCY (V_{COM})

Typical Performance Curves (Continued)

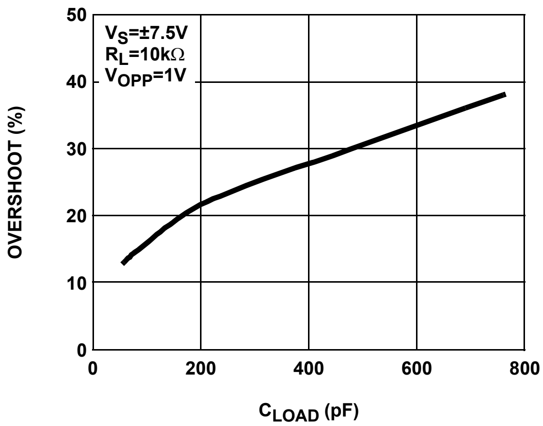


FIGURE 15. OVERSHOOT vs CAPACITANCE LOAD (V_{COM})

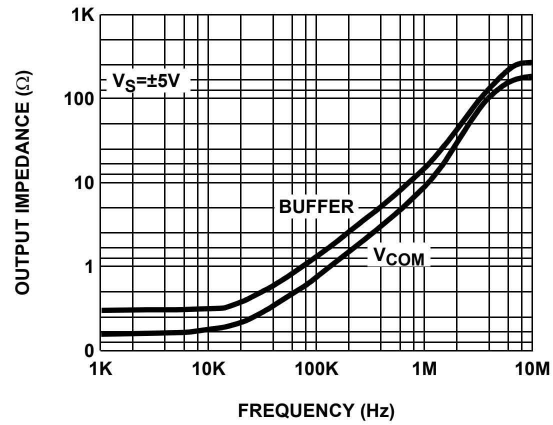


FIGURE 16. OUTPUT IMPEDANCE vs FREQUENCY

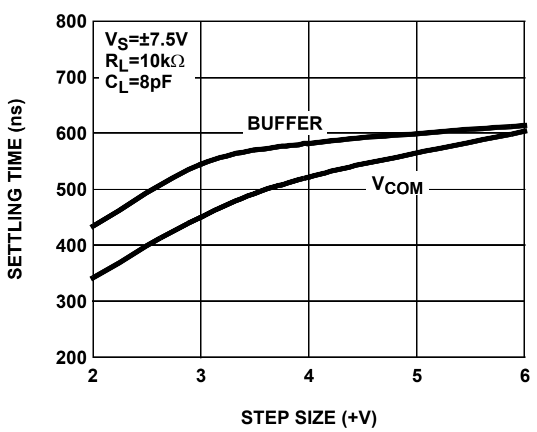


FIGURE 17. SETTLING TIME vs STEP SIZE

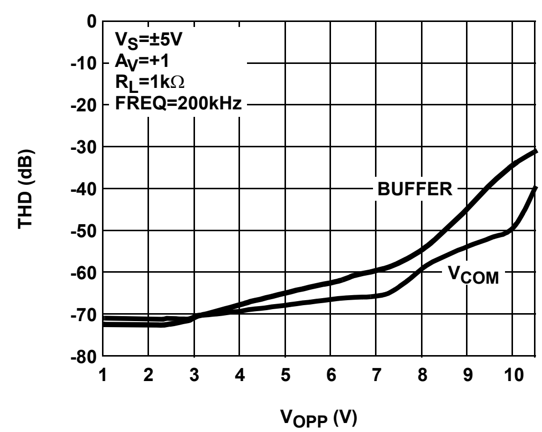


FIGURE 18. TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE

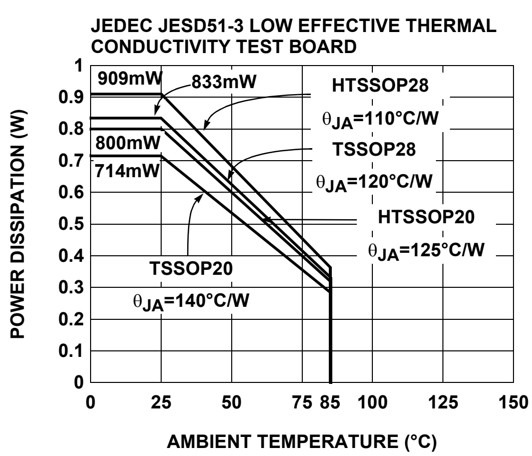


FIGURE 19. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

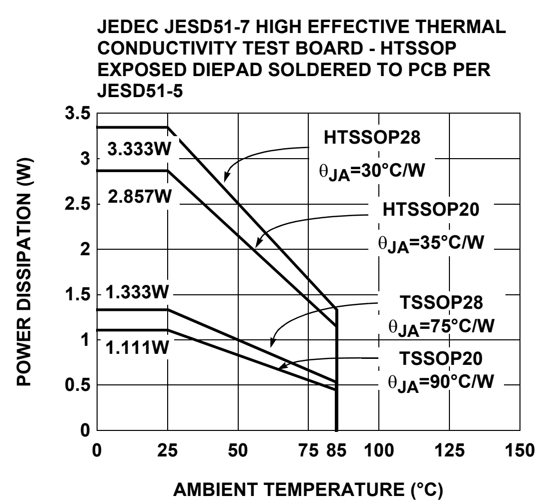


FIGURE 20. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Description of Operation and Application Information

Product Description

The EL5129 and EL5329 are fabricated using a high voltage CMOS process. They exhibit rail to rail input and output capability and have very low power consumption. When driving a load of 10K and 12pF, the buffers have a -3dB bandwidth of 10MHz and exhibit 9V/µs slew rate. The V_{COM} amplifier has a -3dB bandwidth of 12MHz and exhibit 10V/µs slew rate.

Input, Output, and Supply Voltage Range

The EL5129 and EL5329 are specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range from 4.5V to 16.5V.

The input common-mode voltage range of the EL5129 and EL5329 within 500mV beyond the supply rails. The output swings of the buffers and V_{COM} amplifier typically extend to within 100mV of the positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage even closer to each supply rails.

Output Phase Reversal

The EL5129 and EL5329 are immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Although the device's output will not change phase, the input's over-voltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diode placed in the input stage of the device begin to conduct and over-voltage damage could occur.

Output Drive Capability

The EL5129 and EL5329 do not have internal short-circuit protection circuitry. The buffers will limit the short circuit current to ±120mA and the V_{COM} amplifier will limit the short circuit current to ±170mA if the outputs are directly shorted to the positive or the negative supply. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output continuous current never exceeds ±15mA for the buffers and ±100mA for the V_{COM} amplifier. These limits are set by the design of the internal metal interconnections.

The Unused Buffers

It is recommended that any unused buffers should have their inputs tied to ground plane.

Power Dissipation

With the high-output drive capability of the EL5129 and EL5329, it is possible to exceed the 125°C "absolute-maximum junction temperature" under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the buffer to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = V_S \times I_S + \Sigma i \times [(V_S + - V_{OUT}i) \times I_{LOAD}i] + (V_S + - V_{OUT}) \times I_{LA}$$

when sourcing, and:

$$P_{DMAX} = V_S \times I_S + \Sigma i \times [(V_{OUT}i - V_S -) \times I_{LOAD}i] + (V_{OUT} - V_S -) \times I_{LA}$$

when sinking.

where:

- i = 1 to total number of buffers
- V_S = Total supply voltage of buffer and V_{COM}
- I_{SMAX} = Total quiescent current
- $V_{OUT}i$ = Maximum output voltage of the application
- V_{OUT} = Maximum output voltage of V_{COM}
- $I_{LOAD}i$ = Load current of buffer
- I_{LA} = Load current of V_{COM}

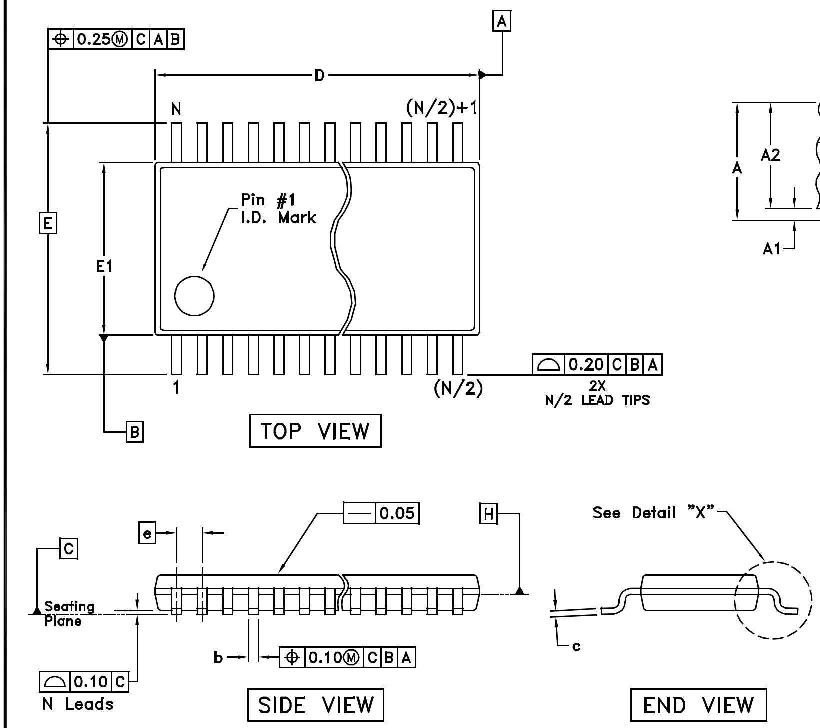
If we set the two P_{DMAX} equations equal to each other, we can solve for the R_{LOAD}'s to avoid device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves.

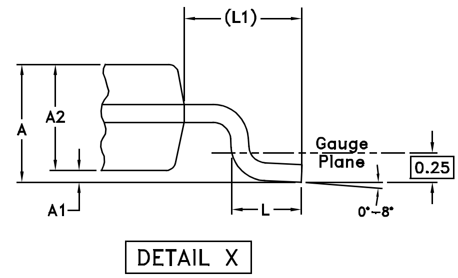
Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, one 0.1µF ceramic capacitor should be placed from the V_S+ pin to ground. A 4.7µF tantalum capacitor should then be connected from the V_S+ pin to ground. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Important Note: The metal plane used for heat sinking of the device is electrically connected to the negative supply potential (V_S-). If V_S- is tied to ground, the thermal pad can be connected to ground. Otherwise, the thermal pad must be isolated from any other power planes.

TSSOP Package Outline Drawing





DIMENSION TABLE						
Symbol	14 Lead	16 Lead	20 Lead	24 Lead	28 Lead	Tolerance
A	1.20	1.20	1.20	1.20	1.20	MAX.
A1	0.10	0.10	0.10	0.10	0.10	+/− 0.05
A2	0.90	0.90	0.90	0.90	0.90	+/− 0.05
D	5.00	5.00	6.50	7.80	9.70	+/− 0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	+/− 0.10
L	0.60	0.60	0.60	0.60	0.60	+/− 0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
b	0.25	0.25	0.25	0.25	0.25	+0.05/−0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/−0.06
e	0.65	0.65	0.65	0.65	0.65	Basic

Drawing #: MDP0044	PACKAGE OUTLINE DRAWING TSSOP (Thin−Shrink Small Outline Package) Family
Rev: E	
Date: 12/11/02	
Units: mm	intersil SOLUTIONS IN SILICON
JEDEC Reg: MO−153	

Notes:

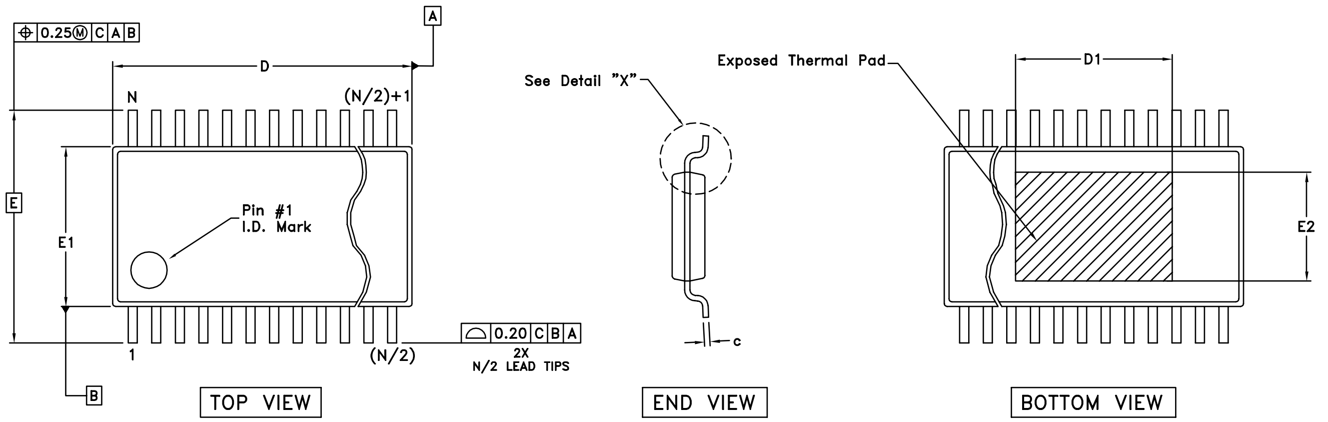
(1) Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.

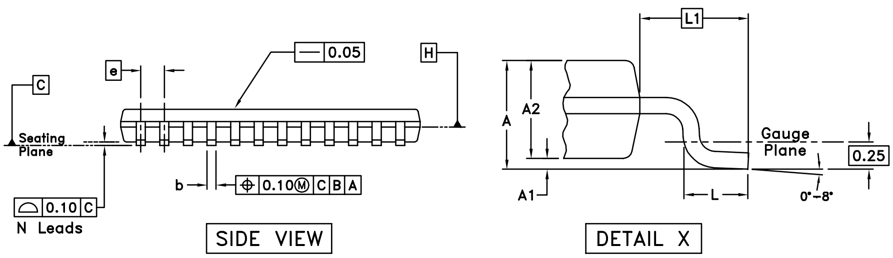
(2) Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.

(3) Dimensions "D" and "E1" are measured at datum plane H.

(4) Dimensioning and tolerancing per ASME Y14.5M−1994.

HTSSOP Package Outline Drawing





DIMENSION TABLE						
Symbol	14L	20L	24L	28L	38L	Tolerance
A	1.20	1.20	1.20	1.20	1.20	MAX.
A1	0.075	0.075	0.075	0.075	0.075	+/- 0.075
A2	0.90	0.90	0.90	0.90	0.90	+0.15/-0.10
D	5.00	6.50	7.80	9.70	9.70	+/- 0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	+/- 0.10
L	0.60	0.60	0.60	0.60	0.60	+/- 0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
b	0.25	0.25	0.25	0.25	0.22	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
e	0.65	0.65	0.65	0.65	0.50	Basic
D1	3.2	4.2	4.3	5.0	7.25	Reference
E2	3.0	3.0	3.0	3.0	3.0	Reference
N	14	20	24	28	38	Reference

Notes:
(1) Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
(2) Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
(3) Dimensions "D" and "E1" are measured at datum plane H.
(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

Drawing #: MDP0048	PACKAGE OUTLINE DRAWING HTSSOP (Heat-Sink TSSOP) Family
Rev: 2	
Date: 12/4/03	
Units: mm	intersil SOLUTIONS IN SILICON
JEDEC Reg: MO-153	

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>