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Multi-Channel Buffer

The EL5623 integrates six channels of gamma buffers into a single device. The top three gamma channels in each device are designed to swing to the upper supply rail, with the other three designed to swing to the lower rail. The output capability of each channel is 10mA continuous, with 120mA peak. The gamma buffers feature a 10MHz -3dB bandwidth specification and a 9V/µs slew rate.

Packaged in the 16-pin TSSOP package, the EL5623 is specified for operation over the -40°C to +85°C temperature range.

Ordering Information

PART NUMBER (See Note)	PACKAGE (Pb-Free)	TAPE & REEL	PKG DWG. #
EL5623IRZ	16-Pin TSSOP	-	MDP0048
EL5623IRZ-T7	16-Pin TSSOP	7”	MDP0048
EL5623IRZ-T13	16-Pin TSSOP	13”	MDP0048

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

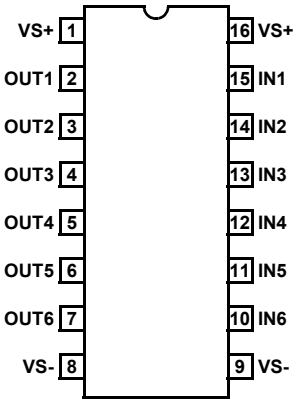
- Six gamma buffers
  - 10MHz BW
  - 9V/µs SR
  - 120mA peak I_{OUT}
  - 3 high side drivers
  - 3 low side drivers
- 3.5mA supply current
- Pb-free available (RoHS compliant)

Applications

- TFT-LCD monitors
- LCD televisions
- Industrial flat panel displays

Pinout

EL5623
(16-PIN TSSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S+ and V_S- . . . . . +18V
Input Voltage . . . . . V_S- -0.5V, V_S+ +0.5V
Maximum Continuous Output Current (V_{OUT1-6}) 15mA

Power Dissipation . . . . . See Curves
Maximum Die Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +15V, V_S- = 0, R_L = 10kΩ, C_L = 10pF to 0V, and T_A = 25°C Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		2	20	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			10		MΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	1V ≤ V_{OUT} ≤ 14V	0.992		1.008	V/V
CMIR	Input Voltage Range	IN1 to IN3	1.5		V_S+	V
		IN4 to IN6	0		V_S+ -1.5	V
OUTPUT CHARACTERISTICS (REFERENCE BUFFERS)						
V_{OH}	High Level Output Voltage - (OUT1)	V_S+ = 15V, I_O = 5mA, V_I = 15V, T_O = 25°C	14.85	14.9		V
	High Level Output Voltage - (OUT2-OUT3)		14.8	14.85		V
	High Level Output Voltage - (OUT4-OUT6)	V_S+ = 15V, I_O = 5mA, V_I = 13.5V, T_O = 25°C	13.45	13.5		V
V_{OL}	Low Level Output Voltage - (OUT1-OUT3)	V_S+ = 15V, I_O = 5mA, V_I = 1.5V, T_O = 25°C		1.5	1.55	V
	Low Level Output Voltage - (OUT4-OUT5)	V_S+ = 15V, I_O = 5mA, V_I = 0V, T_O = 25°C		0.15	.2	V
	Low Level Output Voltage - (OUT6)			0.1	0.15	V
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	Reference buffer V_S from 5V to 15V	50	80		dB
I_S	Total Supply Current			3.5	4.5	mA
DYNAMIC PERFORMANCE (BUFFER AMPLIFIERS)						
SR	Slew Rate (Note 2)		5	9		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		500		ns
BW	-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF		10		MHz
GBWP	Gain-Bandwidth Product	R_L = 10kΩ, C_L = 10pF		6		MHz
PM	Phase Margin	R_L = 10kΩ, C_L = 10pF		50		°
CS	Channel Separation	f = 5MHz		75		dB

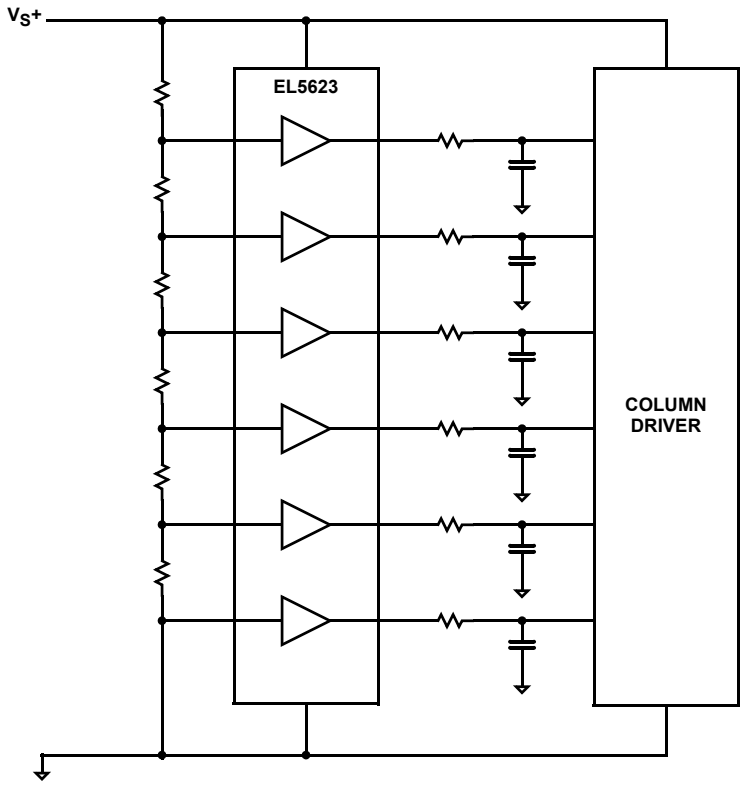
NOTES:

1. Measured over operating temperature range.
2. Slew rate is measured on rising and falling edges.

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1, 16	VS+	Positive supply voltage
2	OUT1	Output gamma channel 1
3	OUT2	Output gamma channel 2
4	OUT3	Output gamma channel 3
5	OUT4	Output gamma channel 4
6	OUT5	Output gamma channel 5
7	OUT6	Output gamma channel 6
8, 9	VS-	Negative supply
10	IN6	Input gamma channel 6
11	IN5	Input gamma channel 5
12	IN4	Input gamma channel 4
13	IN3	Input gamma channel 3
14	IN2	Input gamma channel 2
15	IN1	Input gamma channel 1

Block Diagram



Typical Performance Curves

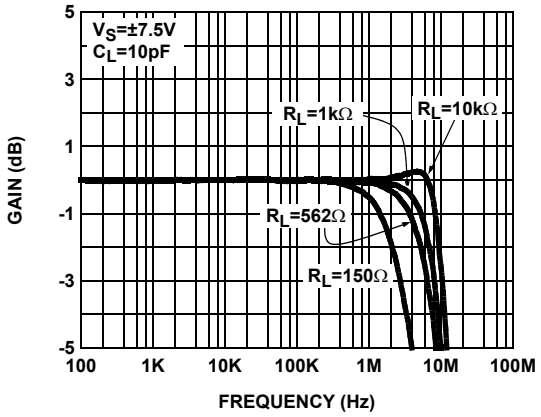


FIGURE 1. FREQUENCY RESPONSE FOR VARIOUS R_{LOAD}

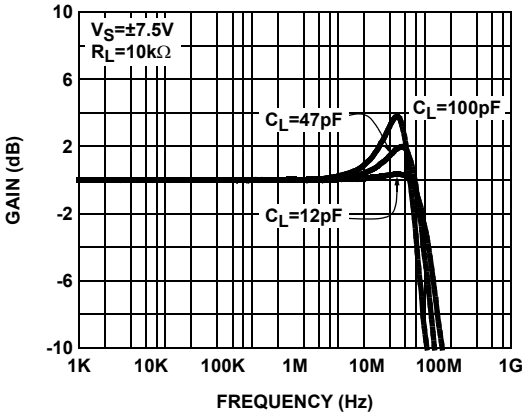


FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS C_{LOAD}

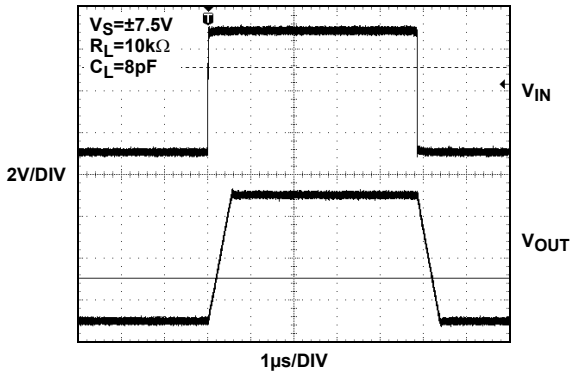


FIGURE 3. LARGE SIGNAL TRANSIENT RESPONSE

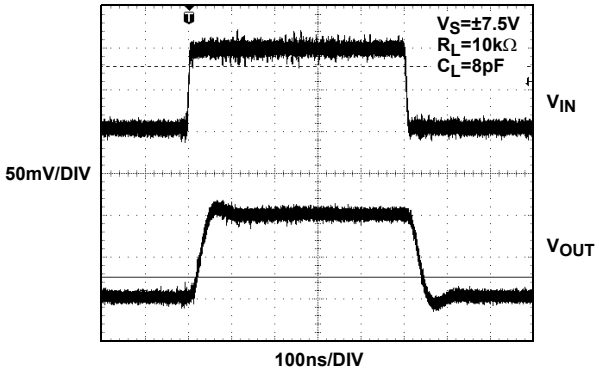


FIGURE 4. SMALL SIGNAL TRANSIENT RESPONSE

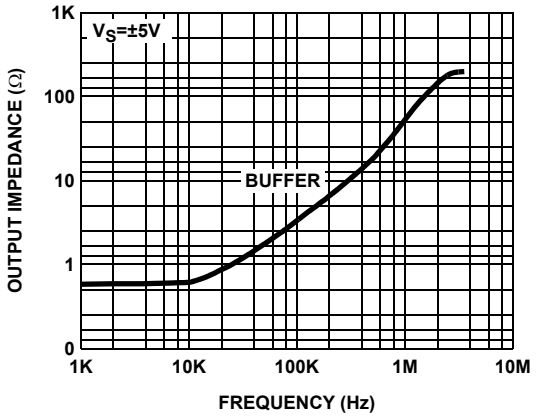


FIGURE 5. OUTPUT IMPEDANCE vs FREQUENCY

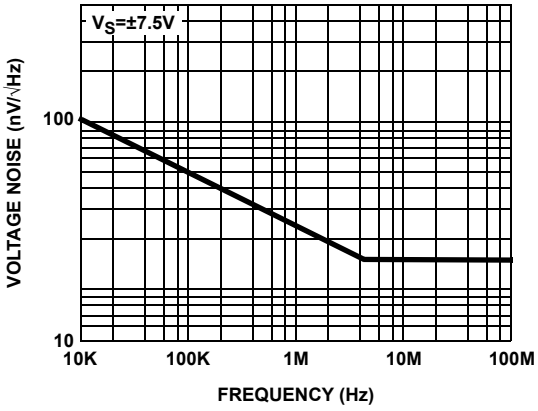


FIGURE 6. INPUT NOISE SPECTRAL DENSITY vs FREQUENCY

Typical Performance Curves

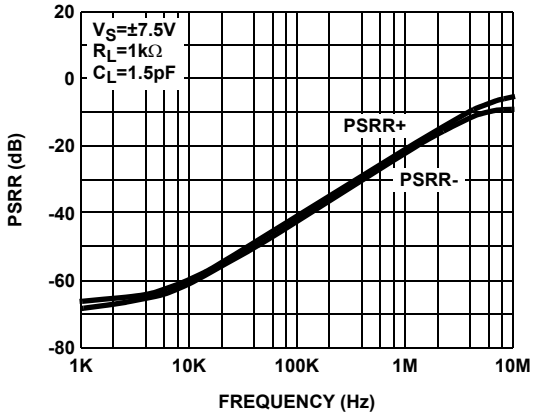


FIGURE 7. PSRR vs FREQUENCY

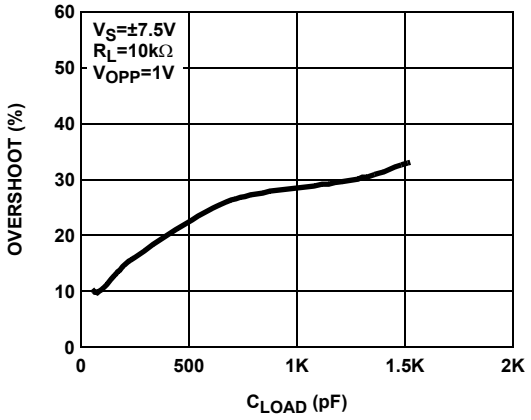


FIGURE 8. OVERSHOOT vs CAPACITANCE LOAD

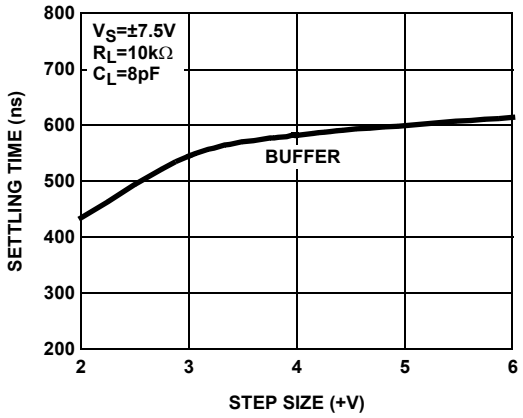


FIGURE 9. SETTLING TIME vs STEP SIZE

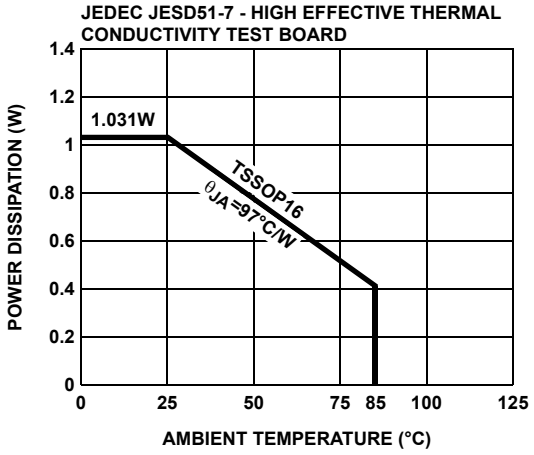


FIGURE 10. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

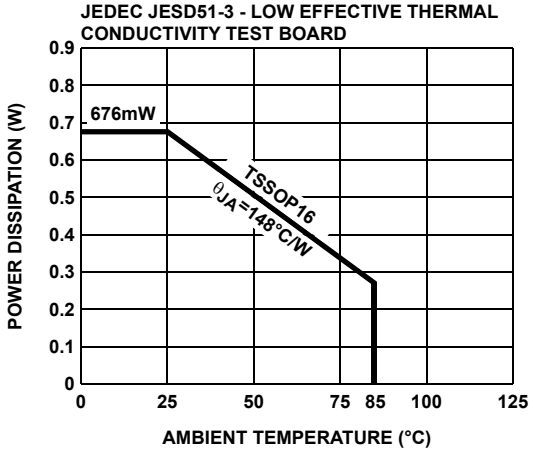


FIGURE 11. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Description of Operation and Application Information

Product Description

The EL5623 is fabricated using a high voltage CMOS process. It exhibits rail to rail input and output capability and has very low power consumption. When driving a load of 10K and 12pF, the buffers have a -3dB bandwidth of 10MHz and exhibit 9V/µs slew rate.

Input, Output, and Supply Voltage Range

The EL5623 is specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range from 4.5V to 16.5V.

The input common-mode voltage range of the EL5623 is within 500mV beyond the supply rails. The output swings of the buffers typically extend to within 100mV of the positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage even closer to each supply rails.

Output Phase Reversal

The EL5623 is immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Although the device's output will not change phase, the input's over-voltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diode placed in the input stage of the device begin to conduct and over-voltage damage could occur.

Output Drive Capability

The EL5623 does not have internal short-circuit protection circuitry. The buffers will limit the short circuit current to ±120mA if the outputs are directly shorted to the positive or the negative supply. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output continuous current never exceeds ±30mA, a limit is set by the design of the internal metal interconnections.

The Unused Buffers

It is recommended that any unused buffers should have their inputs tied to ground plane.

Power Dissipation

With the high-output drive capability of the EL5623, it is possible to exceed the 125°C “absolute-maximum junction temperature” under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the buffer to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = V_S \times I_S + \Sigma i \times [(V_S+ - V_{OUT}i) \times I_{LOAD}i]$$

when sourcing, and:

$$P_{DMAX} = V_S \times I_S + \Sigma i \times [(V_{OUT}i - V_S-) \times I_{LOAD}i]$$

when sinking.

where:

i = 1 to total number of buffers

V_S = Total supply voltage of buffer and V_{COM}

I_{SMAX} = Total quiescent current

$V_{OUT}i$ = Maximum output voltage of the application

$I_{LOAD}i$ = Load current of buffer

If we set the two P_{DMAX} equations equal to each other, we can solve for the R_{LOAD}'s to avoid device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, one 0.1µF ceramic capacitor should be placed from the V_S+ pin to ground. A 4.7µF tantalum capacitor should then be connected from the V_S+ pin to ground. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.