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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



### High Performance Pin Driver

The EL7156 high performance pin driver with three-state is suited to many ATE and level-shifting applications. The 3.5A peak drive capability makes this part an excellent choice when driving high capacitance loads.

The output pin OUT is connected to input pins VH or VL respectively, depending on the status of the IN pin. When the OE pin is active low, the output is placed in the three-state mode. The isolation of the output FETs from the power supplies enables VH and VL to be set independently, enabling level-shifting to be implemented. Related to the EL7155, the EL7156 adds a lower supply pin VS- and makes VL an isolated and independent input. This feature adds applications flexibility and improves switching response due to the increased enhancement of the output FETs.

This pin driver has improved performance over existing pin drivers. It is specifically designed to operate at voltages down to 0V across the switch elements while maintaining good speed and ON-resistance characteristics.

Available in the 8 Ld SOIC and 8 Ld PDIP packages, the EL7156 is specified for operation over the full -40°C to +85°C temperature range.

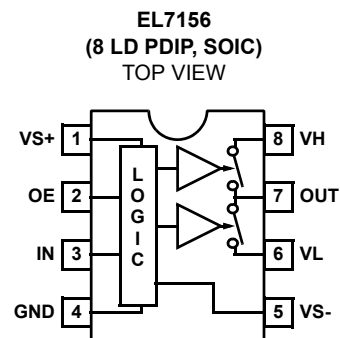
### Features

- Clocking speeds up to 40MHz
- 15ns  $t_R/t_F$  at 2000pF  $C_{LOAD}$
- 0.5ns rise and fall times mismatch
- 0.5ns  $t_{ON}$ - $t_{OFF}$  prop delay mismatch
- 3.5pF typical input capacitance
- 3.5A peak drive
- Low ON-resistance of 3.5Ω
- High capacitive drive capability
- Operates from 4.5V to 16.5V
- Pb-free plus anneal available (RoHS compliant)

### Applications

- ATE/burn-in testers
- Level shifting
- IGBT drivers
- CCD drivers

### Pinout



### Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PKG	PKG. DWG. #
EL7156CNZ (Note) <b>(No longer available, recommended replacement: EL7156CSZ)</b>	EL7156CN Z	-	8 Ld PDIP* (Pb-free)	MDP0031
EL7156CSZ (Note)	7156CSZ	-	8 Ld SOIC (Pb-free)	MDP0027
EL7156CSZ-T7 (Note)	7156CSZ	7"	8 Ld SOIC (Pb-free)	MDP0027
EL7156CSZ-T13 (Note)	7156CSZ	13"	8 Ld SOIC (Pb-free)	MDP0027

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

Supply Voltage ( $V_{S+}$ to $V_{S-}$ )	.....+18V
Input Voltage	..... $V_{S-} -0.3\text{V}$ , $V_{S+} +0.3\text{V}$
Continuous Output Current	..... 200mA
Storage Temperature Range	..... $-65^\circ\text{C}$ to $+150^\circ\text{C}$

**Thermal Information**

Ambient Operating Temperature	..... $-40^\circ\text{C}$ to $+85^\circ\text{C}$
Operating Junction Temperature	..... $+125^\circ\text{C}$
Power Dissipation	..... see curves
Pb-free reflow profile	.....see link below <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>

\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$*

**Electrical Specifications**  $V_{S+} = +15\text{V}$ ,  $V_H = +15\text{V}$ ,  $V_L = 0\text{V}$ ,  $V_{S-} = 0\text{V}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
<b>INPUT</b>						
$V_{IH}$	Logic '1' Input Voltage		2.4			V
$I_{IH}$	Logic '1' Input Current	$V_{IH} = V_{S+}$		0.1	10	$\mu\text{A}$
$V_{IL}$	Logic '0' Input Voltage				0.8	V
$I_{IL}$	Logic '0' Input Current	$V_{IL} = 0\text{V}$		0.1	10	$\mu\text{A}$
$C_{IN}$	Input Capacitance			3.5		pF
$R_{IN}$	Input Resistance			50		M $\Omega$
<b>OUTPUT</b>						
$R_{OVH}$	ON-Resistance $V_H$ to OUT	$I_{OUT} = -200\text{ mA}$		2.7	4.5	$\Omega$
$R_{OVL}$	ON-Resistance $V_L$ to OUT	$I_{OUT} = +200\text{ mA}$		3.5	5.5	$\Omega$
$I_{OUT}$	Output Leakage Current	OE = 0V, OUT = $V_H/V_L$		0.1	10	$\mu\text{A}$
$I_{PK}$	Peak Output Current (linear resistive operation)	Source		3.5		A
		Sink		3.5		A
$I_{DC}$	Continuous Output Current	Source/Sink	200			mA
<b>POWER SUPPLY</b>						
$I_S$	Power Supply Current	Inputs = $V_{S+}$		1.3	3	mA
$I_{VH}$	Off Leakage at $V_H$ and $V_L$	$V_H, V_L = 0\text{V}$		4	10	$\mu\text{A}$
<b>SWITCHING CHARACTERISTICS</b>						
$t_R$	Rise Time	$C_L = 2000\text{pF}$		14.5		ns
$t_F$	Fall Time	$C_L = 2000\text{pF}$		15		ns
$t_{RF\Delta}$	$t_R, t_F$ Mismatch	$C_L = 2000\text{pF}$		0.5		ns
$t_{d-1}$	Turn-Off Delay Time	$C_L = 2000\text{pF}$		9.5		ns
$t_{d-2}$	Turn-On Delay Time	$C_L = 2000\text{pF}$		10		ns
$t_{d\Delta}$	$t_{d-1}-t_{d-2}$ Mismatch	$C_L = 2000\text{pF}$		0.5		ns
$t_{d-3}$	Three-state Delay Enable			10		ns
$t_{d-4}$	Three-state Delay Disable			10		ns



# EL7156

## Electrical Specifications $V_{S+} = +5V, V_H = +5V, V_L = -5V, V_{S-} = -5V, T_A = +25^\circ C$ , unless otherwise specified. (Continued)

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
<b>INPUT</b>						
$V_{IH}$	Logic '1' Input Voltage		2.0			V
$I_{IH}$	Logic '1' Input Current	$V_{IH} = V_{S+}$		0.1	10	$\mu A$
$V_{IL}$	Logic '0' Input Voltage				0.8	V
$I_{IL}$	Logic '0' Input Current	$V_{IL} = 0V$		0.1	10	$\mu A$
$C_{IN}$	Input Capacitance			3.5		pF
$R_{IN}$	Input Resistance			50		M $\Omega$
<b>OUTPUT</b>						
$R_{OVH}$	ON-Resistance $V_H$ to OUT	$I_{OUT} = -200mA$		3.4	5	$\Omega$
$R_{OVL}$	ON-Resistance $V_L$ to OUT	$I_{OUT} = +200mA$		4	6	$\Omega$
$I_{OUT}$	Output Leakage Current	$OE = 0V, OUT = V_H/V_L$		0.1	10	$\mu A$
$I_{PK}$	Peak Output Current (linear resistive operation)	Source		3.5		A
		Sink		3.5		A
$I_{DC}$	Continuous Output Current	Source/Sink	200			mA
<b>POWER SUPPLY</b>						
$I_S$	Power Supply Current	Inputs = $V_{S+}$		1	2.5	mA
$V_H$	Off Leakage at $V_H$ and $V_L$	$V_H, V_L = 0V$		4	10	$\mu A$
<b>SWITCHING CHARACTERISTICS</b>						
$t_R$	Rise Time	$C_L = 2000pF$		17		ns
$t_F$	Fall Time	$C_L = 2000pF$		17		ns
$t_{RF\Delta}$	$t_R, t_F$ Mismatch	$C_L = 2000pF$		0		ns
$t_{d-1}$	Turn-Off Delay Time	$C_L = 2000pF$		11.5		ns
$t_{d-2}$	Turn-On Delay Time	$C_L = 2000pF$		12		ns
$t_{d\Delta}$	$t_{d-1}-t_{d-2}$ Mismatch	$C_L = 2000pF$		0.5		ns
$t_{d-3}$	Three-state Delay Enable			10		ns
$t_{d-4}$	Three-state Delay Disable			10		ns

Typical Performance Curves

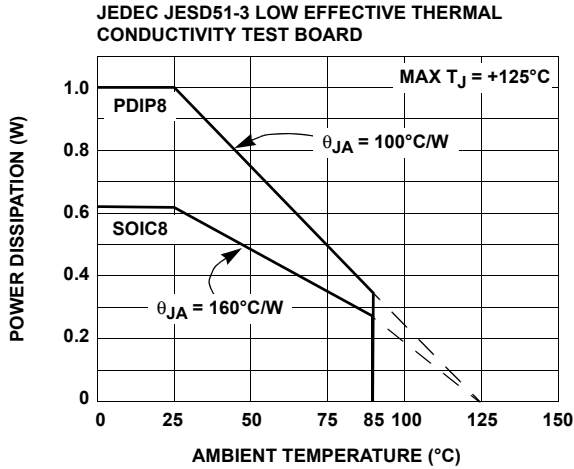


FIGURE 1. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

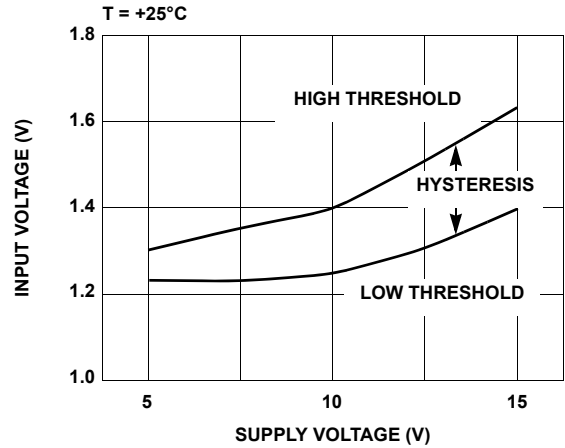


FIGURE 2. INPUT THRESHOLD vs SUPPLY VOLTAGE

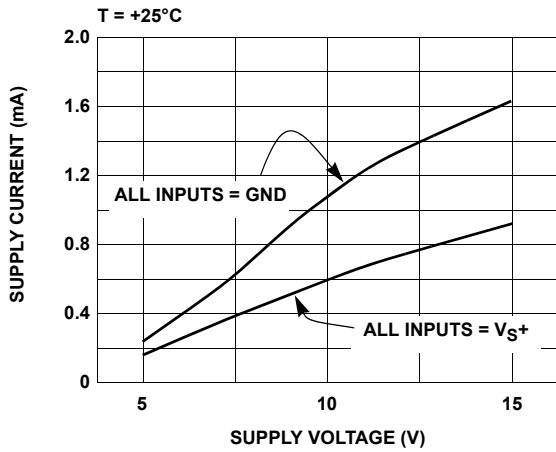


FIGURE 3. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

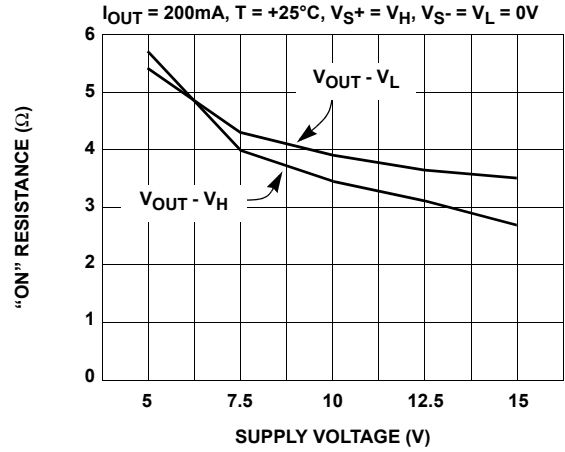


FIGURE 4. "ON"-RESISTANCE vs SUPPLY VOLTAGE

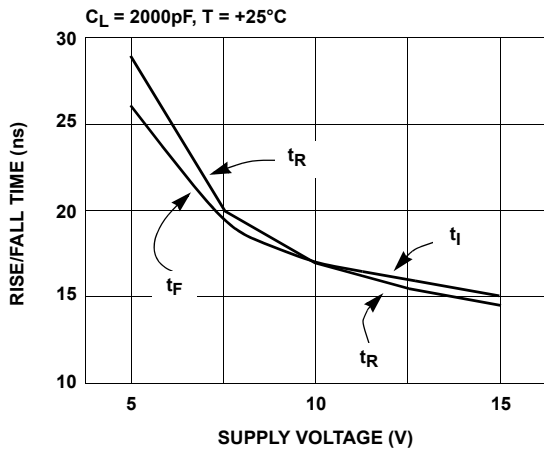


FIGURE 5. RISE/FALL TIME vs SUPPLY VOLTAGE

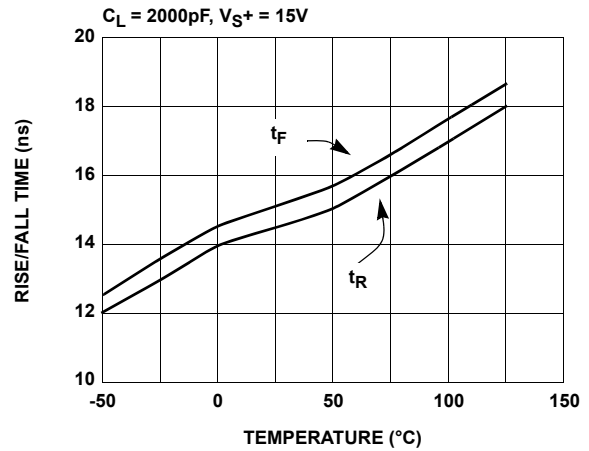


FIGURE 6. RISE/FALL TIME vs TEMPERATURE

Typical Performance Curves (Continued)

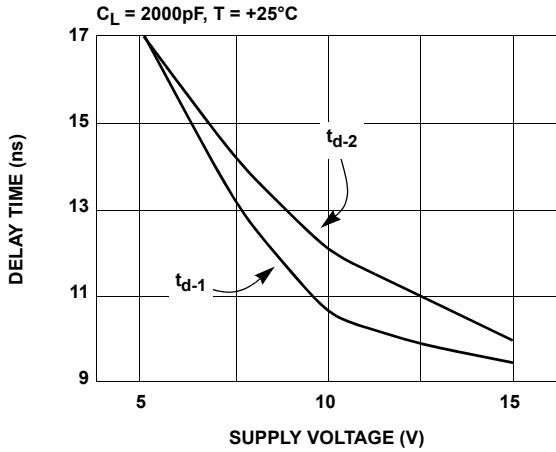


FIGURE 7. PROPAGATION DELAY vs SUPPLY VOLTAGE

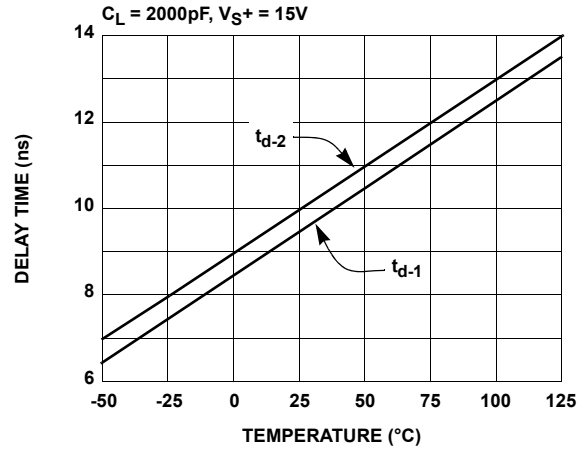


FIGURE 8. PROPAGATION DELAY vs TEMPERATURE

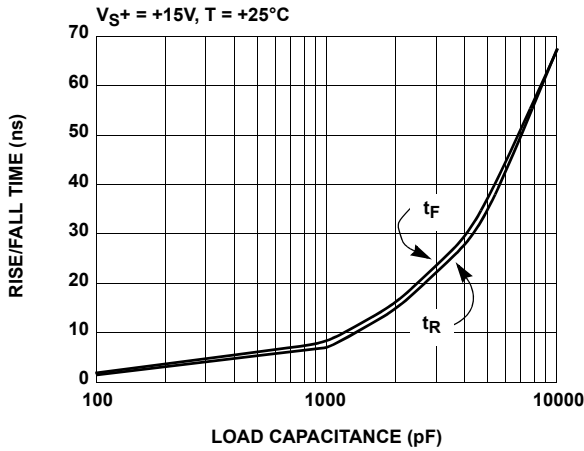


FIGURE 9. RISE/FALL TIME vs LOAD CAPACITANCE

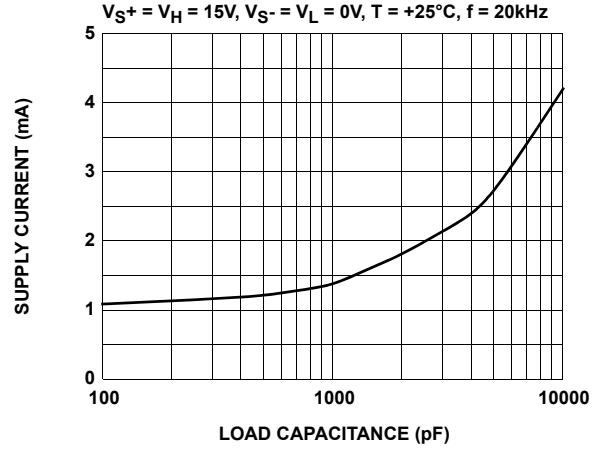


FIGURE 10. SUPPLY CURRENT vs LOAD CAPACITANCE

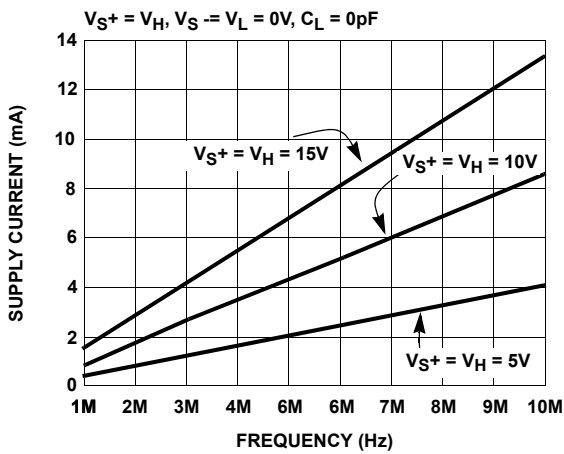


FIGURE 11. SUPPLY CURRENT vs FREQUENCY

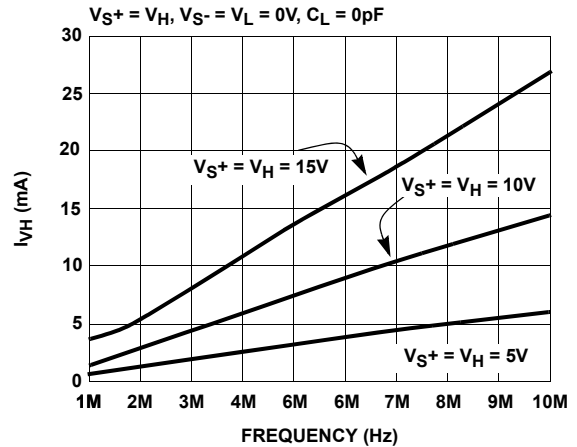


FIGURE 12.  $V_H$  SUPPLY CURRENT vs FREQUENCY

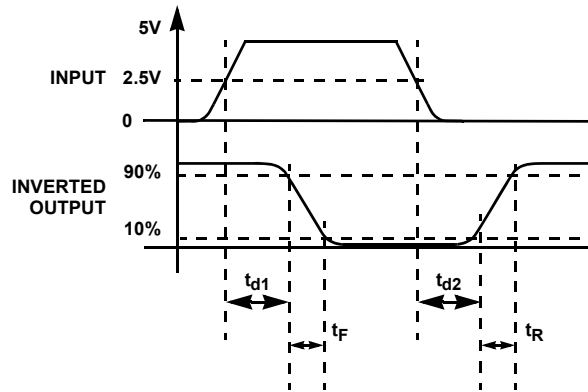
**Truth Table**

OE	IN	OUT
0	0	Three-state
0	1	Three-state
1	0	V <sub>H</sub>
1	1	V <sub>L</sub>

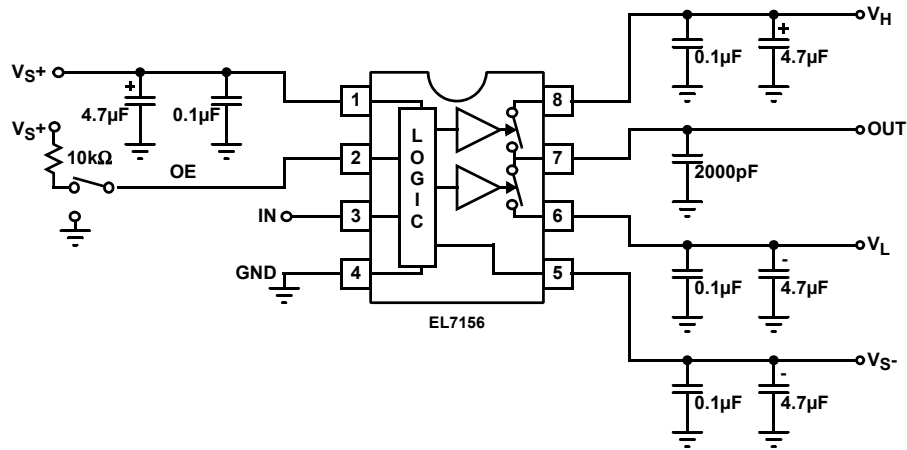
**Operating Voltage Range**

PIN	MIN	MAX
V <sub>S-</sub> to GND	-5	0
V <sub>S+</sub> to V <sub>S-</sub>	5	16.5
V <sub>H</sub> to V <sub>L</sub>	0	16.5
V <sub>S+</sub> to V <sub>H</sub>	0	16.5
V <sub>S+</sub> to GND	5	16.5
V <sub>L</sub> to V <sub>S-</sub>	0	16.5
Three-state Output	V <sub>L</sub>	V <sub>H</sub>

**Timing Diagram**



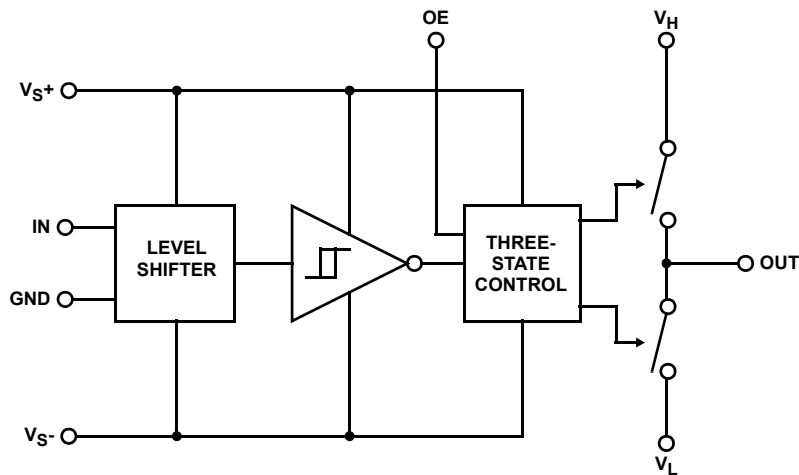
**Standard Test Configuration**



**Pin Descriptions**

PIN	NAME	FUNCTION	EQUIVALENT CIRCUIT
1	VS+	Positive Supply Voltage	
2	OE	Output Enable	<p>CIRCUIT 1</p>
3	IN	Input	Reference Circuit 1
4	GND	Ground	
5	VS-	Negative Supply Voltage	
6	VL	Lower Output Voltage	
7	OUT	Output	<p>CIRCUIT 2</p>
8	VH	High Output Voltage	

**Block Diagram**





**Applications Information**

**Product Description**

The EL7156 is a high performance 40MHz pin driver. It contains two analog switches connecting VH and VL to OUT. Depending on the value of the IN pin, one of the two switches will be closed and the other switch open. An output enable (OE) is also supplied which opens both switches simultaneously.

Due to the topology of the EL7156, both the VH and VL pins can be connected to any voltage between the VS+ and VS- pins, but VH must be greater than VL in order to prevent turning on the body diode at the output stage.

The EL7156 is available in both the 8 Ld SOIC and the 8 Ld PDIP packages. The relevant package should be chosen depending on the calculated power dissipation.

**Three-state Operation**

When the OE pin is low, the output is three-state (floating). The output voltage is the parasitic capacitance’s voltage. It can be any voltage between VH and VL, depending on the previous state. At three-state, the output voltage can be pushed to any voltage between VH and VL. The output voltage can’t be pushed higher than VH or lower than VL since the body diode at the output stage will turn on.

**Supply Voltage Range and Input Compatibility**

The EL7156 is designed for operation on supplies from 5V to 15V (4.5V to 16.5V maximum). “Operating Voltage Range” on page 6 shows the specifications for the relationship between the VS+, VS-, VH, VL, and GND pins.

All input pins are compatible with both 3V and 5V CMOS signals. With a positive supply (VS+) of 5V, the EL7156 is also compatible with TTL inputs.

**Power Supply Bypassing**

When using the EL7156, it is very important to use adequate power supply bypassing. The high switching currents developed by the EL7156 necessitate the use of a bypass capacitor between the supplies (VS+ and VS-) and GND pins. It is recommended that a 2.2µF tantalum capacitor be used in parallel with a 0.1µF low-inductance ceramic MLC capacitor. These should be placed as close to the supply pins as possible. It is also recommended that the VH and VL pins have some level of bypassing, especially if the EL7156 is driving highly capacitive loads.

**Power Dissipation Calculation**

When switching at high speeds, or driving heavy loads, the EL7156 drive capability is limited by the rise in die temperature brought about by internal power dissipation. For reliable operation, die temperature must be kept below T<sub>JMAX</sub> (+125°C). It is necessary to calculate the power dissipation for a given application prior to selecting the package type.

Power dissipation may be calculated:

$$PD = (V_S \times I_S) + (C_{VS} \times V_S^2 \times f) + [(C_{INT} + C_L) \times V_{OUT}^2 \times f] \tag{EQ. 1}$$

where:

- V<sub>S</sub> is the total power supply to the EL7156 (from VS+ to GND)
- V<sub>OUT</sub> is the swing on the output (V<sub>H</sub> to V<sub>L</sub>)
- C<sub>VS</sub> is the integral capacitance due to VS+
- C<sub>INT</sub> is the integral load capacitance due to V<sub>H</sub>
- I<sub>S</sub> is the quiescent supply current (3mA max)
- f is frequency

**TABLE 1. INTEGRAL CAPACITANCE**

V <sub>S+</sub> = V <sub>H</sub> (V)	C <sub>VS</sub> (pF)	C <sub>INT</sub> (pF)
5	80	120
10	85	145
15	90	180

Having obtained the application’s power dissipation, a maximum package thermal coefficient may be determined, to maintain the internal die temperature below T<sub>JMAX</sub>:

$$\theta_{JA} = \frac{T_{JMAX} - T_{MAX}}{PD} \tag{EQ. 2}$$

where:

- T<sub>JMAX</sub> is the maximum junction temperature (+125°C)
- T<sub>MAX</sub> is the maximum operating temperature
- PD is the power dissipation calculated above
- θ<sub>JA</sub> thermal resistance on junction to ambient

θ<sub>JA</sub> is 160°C/W for the SOIC8 package and 100°C/W for the PDIP8 package when using a standard JEDEC JESD51-3 single-layer test board. If T<sub>JMAX</sub> is greater than +125°C when calculated using Equation 2, then one of the following actions must be taken:

- Reduce θ<sub>JA</sub> the system by designing more heat-sinking into the PCB (as compared to the standard JEDEC JESD51-3).
- Use the PDIP8 instead of the SOIC8 package.
- De-rate the application either by reducing the switching frequency, the capacitive load, or the maximum operating (ambient) temperature (T<sub>MAX</sub>).

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 1, 2015	FN7280.4	Updated Ordering Information Table on page 1. Added Revision History and About Intersil sections.

## About Intersil

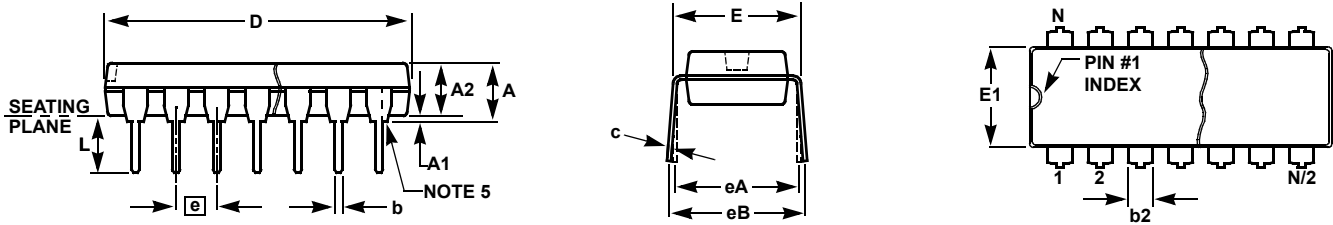
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at [www.intersil.com](http://www.intersil.com).

You may report errors or suggestions for improving this datasheet by visiting [www.intersil.com/ask](http://www.intersil.com/ask).

Reliability reports are also available from our website at [www.intersil.com/support](http://www.intersil.com/support)

**Plastic Dual-In-Line Packages (PDIP)**



**MDP0031**

**PLASTIC DUAL-IN-LINE PACKAGE**

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

**NOTES:**

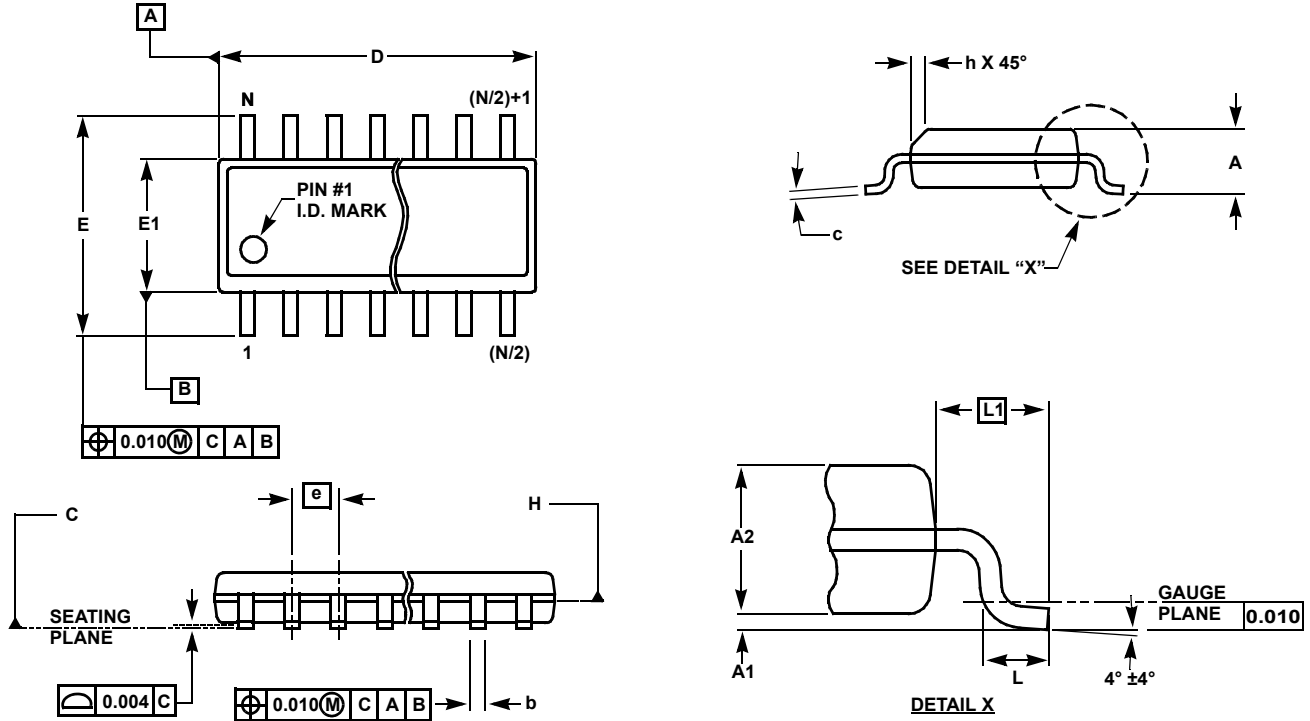
1. Plastic or metal protrusions of 0.010" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9001 quality systems.  
Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

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**Small Outline Package Family (SO)**



**MDP0027**

**SMALL OUTLINE PACKAGE FAMILY (SO)**

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

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**NOTES:**

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994